Self-Aligned Single-Electron Memories

SASEM Project (IST-2001-32674)

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(1) Introduction

Single-electron memory, which consists of a narrow channel MOSFET with a nano floating gate embedded in the gate oxide, is much attractive due to its high density, low power consumption and compatibility with conventional MOS technology. The key technological issue is to fabricate a nano floating gate and align it with the channel in a controlled manner. The goal of SASEM project is to realize a self-aligned single-electron memory operating at room temperature and investigate technology transfer. This project includes three main workpackages concerning device fabrication, process simulation and optimization and electrical characterization. A selection of results is briefly presented.

(2) Device fabrication

Based on arsenic-assisted etching and oxidation effects, we fabricated single-electron memory devices, as well as arrays of memory cells, in which the floating gate is self-aligned with the MOS channel. A SEM image of a few devices is shown in Fig. 1, where the floating gate with a size of 20nm can be seen in the gate oxide. The triangular channel has a height and a base of 100nm and 125nm, respectively. By combining optical lithography with e-beam lithography, large throughput has been reached. The critical technology step, i.e. channel and dot formation, has been tested successfully by the industrial partner (ST electronics) with current optical tools (see Fig. 2). Finally, scaled down devices (10 nm quantum dot) with single electron behavior have been fabricated. Their behavior is discussed hereafter.

(3) Process simulation and optimization

To control well the formation and the size of the floating gate, the full process of the SASEM device has been simulated by the simulator of TSUPREM-4 and DIOS from ISE-TCAD. A monitoring tool under MATLAB has been developed to extract device parameters vs. process parameters. Critical process parameters such as oxidation temperature and time have be optimized. A simulation result is shown in Fig. 3, consistent with the observed cross section of the device in Fig.1.

(4) Electrical characterization

Figure 4 gives electrical characteristics of a fabricated memory device. The device behaves like a p-channel MOSFET and is normally-off. A clear hysteresis of $Id(Vg)$ curve is observed. The threshold voltage V_{th} can be expressed approximately by $nx\Delta V_{th}$, where n is integer and $\Delta V_{th} \cong 0.09V$. This quantized V_{th} shift indicates that the Coulomb blockade effect occurs, with a single hole tunneling to the floating gate at room temperature. Therefore, the hysteresis of $Id(Vg)$ curve and quantized threshold voltage shift are evidence of single-electron memory effect.

To observe the single-electron charging behavior, the Coulomb blockade theory sets the temperature limitation: $T=q^2/2k_BC_\Sigma$. C_Σ is the total capacitance. For our device, the existence of Coulomb blockade effect at room temperature implies that the total capacitance is smaller than 3 aF. The maximum size of the floating gate is estimated to be about 14nm from $C_\Sigma=4\pi\varepsilon_{ox}r$. This is consistent with the observed cross section of the fabricated quantum dot (10 nm).

In order to realize the final circuit, the distribution of the threshold voltage shift must be investigated. Figure 5 shows the threshold voltage shift distribution for 70 devices fabricated on the same SOI wafer. It is found that the threshold voltage shift varied from 0.04V to 0.56V. The lithography tool was recognized as the source of variations.

(5) Conclusion

Compared with other single-electron memory devices proposed in the literature, the SASEM device operating at room temperature has three main advantages: (1) it does not require very fine pattern formation technology to obtain a nano floating gate (thinnest pattern is 100 nm), (2) the nano floating gate and a high quality, thermally formed, tunnel oxide are performed simultaneously in a simple process step, and (3) the floating gate and the channel are self-aligned. Our device is mentioned in the ITRS 2003 (page 20). The reproducibility, compatibility with MOS processes and large throughput in our process implies that this technology is a good potential candidate to realize single electron memory circuit in a near future.

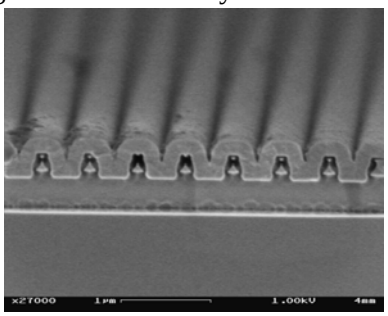

Fig. 1: SEM cross-section for a few cells in the fabricated array.

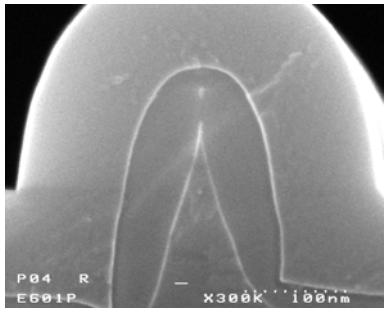

Fig. 2: SEM cross-section for a cell fabricated by optical

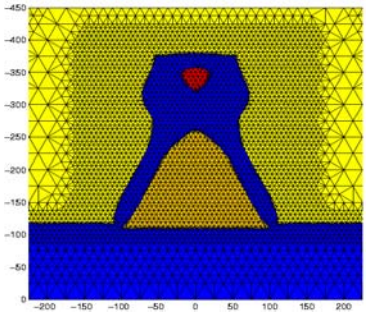

Fig. 3: Simulated cross-section for a cell shown in Fig. 1.

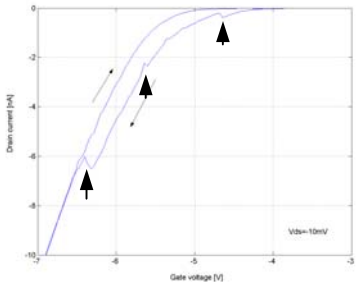

Fig. 4: Hysteresis characteristics of the memory devics at room temperature. The arrows represent Id(Vg) curve with one, two, three … holes injected into the

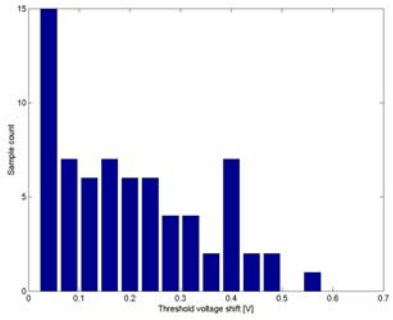

Fig.5: The distribution of threshold voltage shift for 70 memory devices.