nanoICT
STRATEGIC RESEARCH AGENDA

nanoICT coordination action

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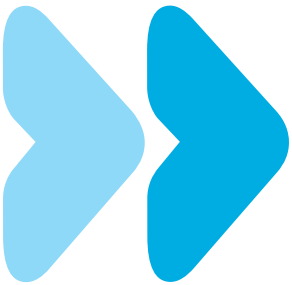
Version 1.0

Index



At this stage, it is impossible to predict the exact course the nanotechnology revolution will take and, therefore, its effect on our daily lives. We can, however, be reasonably sure that nanotechnology will have a profound impact on the future development of many commercial sectors. The impact will likely be greatest in the strategic nanoelectronics (ICT nanoscale devices - nanoICT) sector, currently one of the key enabling technologies for sustainable and competitive growth in Europe, where the demand for technologies permitting faster processing of data at lower costs will remain undiminished.

Considering the fast and continuous evolvements in the inter-disciplinary field of Nanotechnology and in particular of "ICT nanoscale devices", initiatives such as the nanoICT Coordination Action[1] should identify and monitor the new emerging fields research drivers of interest for this Community and put in place instruments/measures to address them.

One of the main challenges is the timely identification and substantiation of new directions for the physical realisation of ICT beyond CMOS that have a high potential for significant breakthrough and that may become the foundations of the information and communication technologies and innovations of tomorrow.

Therefore, the first version of the nanoICT research agenda provides focus and accelerate progress in identified R&D directions and priorities for the "nanoscale ICT devices and systems" FET proactive program and guide public research institutions, keeping Europe at the forefront in research. In addition, it aims to be a valid source of guidance, not only for the nanoICT scientific community but also for the industry (roadmapping issues), providing the latest developments in the field of emerging nano-devices that appear promising for future take up by the industry.

This first version of the research agenda is an open document to comments and/or suggestions and covers a very wide range of interdisciplinary areas of research and development, such as Mono-Molecular electronics, Bioelectronics, NEMS, Nanotubes, Modelling, etc. providing insights in these areas, currently very active worldwide.

Expected impact of initiatives such as this nanoICT strategic research agenda is to enhance visibility, communication and networking between specialists in several fields, facilitate rapid information flow, look for areas of common ground between different technologies and therefore shape and consolidate the European research community.

I hope you will enjoy reading this document and look forward to the next edition beginning of 2011 which will explore some new nanoICT related research areas such as Spintronics, Nanophotonics and Nanophononics. Please contact coordinators of the working groups if you are interested in providing a comment or would like to see your research featured in future editions.

The editor

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[1] www.nanoICT.org

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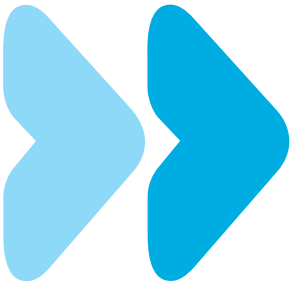
Introduction



1. Introduction

Robert Baptist (CEA, France)

This introduction does not pretend to be an historical description of developments in nanoscience or nanotechnology over the last 20 years. It is only a guide through various domains that will influence Future Emerging Technologies (FET) and will definitely inspire or master our future.

First, the text introduces the context of nanoelectronics and 7 reports written by experts of the Nano-ICT project on well defined topics. It then tries to indicate some (new) perspectives that the author think should be important in the upcoming times.

In order to give some freedom to the reader and enrich the next version of this first draft, this document is voluntarily not split, nor well organized, into chapters, paragraphs, historical development, tables, etc. This absence of structure should enable to point out missing but important issues and generate debates about the respective importance of different fields. Feel free to signal corrections and suggest comments/disagreements to enrich this first version and prepare the next one, we have to set up during the fourth year of the nanoICT Coordination Action.

Since their discovery by Iijima in 1991, carbon nanotubes have been the subject of intensive research and development activity. Indeed, they combine a very broad range of exceptional intrinsic properties, which have caused interest in many fields of science and technology such photonics and nanoelectronics. The same occurs with semiconducting nanowires which, for example, benefit from the fourth dimension in microelectronics, with nanostructure-based NEMS reaching the quantum world, or with nanotubes, graphene and organic based spintronics research, which are new challenging areas of research, with great promise for novel types of information processing and storage.

All these aspects of research achieved during the last 20 years for information and communication technologies (ICT), as well as the challenges for their use in the field of electronics and ICT are presented in the following chapters, together with the strategic research agenda and their respective position papers. This research is developed in the world and in many cases specific technologies have been developed for integration into standard microelectronics. Applications will be short or medium term depending on the maturity of the domain. The following chapters, written by experts, give an insight into their time schedules.

However, apart from the domains of investigation that we briefly present below, various possible outlined scenarios could transform in a different manner the "convergence" between (bio) nanomaterials and ICT; consequently our vision on the future of electronics (in a broad sense) can be enlarged. Here, in this preface we propose to give an overview of leading trends which are not directly covered presently by the nanoICT actions but which could have a real impact in the future of nanoelectronics and its relation to ICT. Naturally many subjects are indeed treated in other European programs and when appropriate we will refer to them.

This overview is not intended to describe things accurately or to present recent published literature but rather to provide a possible guidance towards the 2020-2030 time frames. All information and points of view are not expressed in this first draft but will be complemented by the data in the next editions.

Introduction

Classical Microelectronics

Microelectronics follows technical changes and evolutions suggested or required by the International Technology Roadmap for Semiconductors (ITRS, www.itrs.net) to keep on track with the so-called Moore's law, and it also follows worldwide economical and societal parameters. These developments reflect also national or international technical programs (such as those from ENIAC www.eniac.eu, or EPOSS www.smart-systems-integration.org/public in Europe) and of course the strategies of industrial or research clusters and their alliances in this field, for example the recent IBM alliance www-03.ibm.com/press/us/en/pressrelease/27222.wss. Any future non CMOS devices already studied in laboratories which could replace the CMOS FET as logic switches shall present significant advantages over these ultimate classical FETs in terms of density, power performances and cost.

Considering Moore's law and its scale reduction, to which future devices coming from other technologies should be compared, it is enough to mention the various devices sizes and the date of their possible production to see the difficulties in front of any new device willing to enter this field; if we take the case of logic devices, we get the following table:

Generation	45 nm	32 nm	22 nm	16 nm	11 nm	8 nm
ITRS 2009	In production	2010	2012	2015	2018	2020-2021

Table 1. Roadmap (according to the ITRS) for the introduction of next technology generations (logic circuits, including microprocessors). R&D activities will be carried out by microelectronics companies before introduction into production. When physical fundamental limits will be reached (~ 2020) either these limits will be overcome or the economic and societal interest will focus on alternative science. Note that for flash memories, the agenda is even more aggressive.

To solve future problems such as variability between devices or energy dissipation, new materials listed in the ITRS could be used (for example Ge and III-V materials integrated in the transistor channel or high-k dielectrics for the gate stacking or ionic compounds for memories) and advantages of pursuing Moore's law strategy are manifest: pushing technology to its limits will result in a reduced number (<5) players in the world.

These industrials will fabricate all advanced microelectronics microprocessors and hyper dense memories to be used in the world and this is thanks to the huge investments needed to produce nano CMOS on large 300 or 450 mm wafers. Probably, all performances will get better (by a factor of 1000-1000000) during the next decades.

This mainstream semiconductor technology is today different from what it was 20 years ago before internet, gaming and mobile phones existed. In particular from that time, conventional technology has integrated new functions such as RF functions, switches, sensors, etc (which are often fabricated using semiconductor and nanoelectronics technologies in particular CMOS technology). All these instruments get progressively ubiquitous. These orientations are connected to the "More Moore" and "More than Moore" approaches which respectively lead to fabrication of devices at the nano scale and devices with added functions extending Moore's Law. Today, it seems consequently more difficult to keep only such a simplified presentation of "classical" electronics in terms of an industrial sector working only on "memories and logic for computing" even if the huge investments characteristic of the microelectronics industry give to this sector a particular importance. The diversity of applications listed in the recent call of ENIAC, focusing on "Nanoelectronics for Health & Wellness", "Nanoelectronics for Transport & Mobility", Nanoelectronics for Security & Safety", "Nanoelectronics for Energy & Environment", "Nanoelectronics for Communication", "Nanoelectronics for E-Society", show that microelectronics has been much expanded and is now infiltrating all human activities.

A consequence of this is that the components are no longer limited to information processing and dissemination/ communication (telecom) but also include actuators, transducers, restorers of senses (displays, electronic noose), "caregiver for defects" (prostheses, artificial retinas...), "stokers" of energy (micro-batteries, fuel cells...), and high power (smart) devices... Integration as described by "EPoSS, the European Technology Platform on Smart Systems Integration" www.smart-systems-integration.org/public gives an idea of R&D and innovation needs as well as policy requirements related to Smart Systems Integration and integrated Micro and Nanosystems.

Moreover, like in the car industry, where devices for engine control systems, headlight, ABS, car camera recorder, anticollision radar, climate control units, comfort, have invaded the automobile and increased its norms for security, it appears that these applications, able to connect continuously and universally, will be present everywhere, with secured connectivity: they will modify our ways of life and also shape the future of electronics.

These technical evolutions in microelectronics and in integration of systems accompany the evolution in ICT where the notion of information is today much more connected to gaming, energy aspects, environmental context, health and neuroscience, and their respective research areas than some years ago. Its future is continuously reshaped in particular by research done in laboratories. This is what we will try to present briefly after the introduction of the various conclusions of the different working groups in nanoICT.

Strategic agenda from nanoICT groups

Returning to **carbon nanotubes**, the SRA and position paper written by W. Milne and co-workers shows their huge potential even if their integration into CMOS technologies either for vias or for transistors still seems to be problematic. A plethora of scientific and technical results are described covering many applications. In the next version of the position paper, due next year, the working group will incorporate a state of the art description of the physics of graphene. Graphene and carbon nanotubes are indeed major players in the so-called "Carbon-based nanoelectronics" in the ITRS roadmap.

Semiconducting nanowires (NW) are treated by Lars Samuelson and co-workers in a large report integrating the latest results from the integrated project "NODE" (www.node-project.com). We also reproduce the introduction provided by L. Samuelson in its report, which presents other aspects of development of this technology.

Other central areas of nanowire research and applications deal with fundamental studies of nanowire growth, as very actively pursued through the arrangements of a series of four European Workshops on Growth on nanowires, most recently the 4th arranged in Paris in October 2009. We include as an appendix a summary of the status as revealed from this workshop (written by J-C Harmand and F. Glas).

Incorporated in this article is also a status of the field description provided by J. Johansson and P. Caroff. In order to provide a more detailed description of the level of understanding and control of physical properties of nanowires, a special chapter has been provided for this by L. P. Kouwenhoven and V. Zwiller. This chapter also deals in more detail with the opportunities for opto-electronic devices based on NW technology. Another important area of NW research relates to their application for Energy harvesting as implemented in solar cells and thermoelectrics. For the use of NWs in photo-voltaics was recently started an EU-project called AMON-RA (www.amonra.eu). We enclose two short descriptions of nanowires for energy, provided by K. Deppert.

An increasingly important aspect of nanowire research deals with their use in biology and in medical applications. We include here also a description of the state of the art as provided by C. Prinz and J. Tegenfeldt.

Finally, for this NW activity is also included an insight on this domain written by Jean-Christophe Harmand and his colleagues from the French GDR on nanowires (http://iemn.univ-lille1.fr/GDRNanofil/accueil_fr. html) and from the Steering Committee, of the Growth Workshop 2009 (NWG2009).

NEMS. The situation, here is paradoxical. Huge progress has been made both from the scientific and technical points of view but neither reaching quantum limits for vibrations nor the possibility of detecting one molecule, nor the possibility of fabricating millions of identical NEMS is opening the door to clearly defined consumer applications (except maybe mass spectrometers for environmental or medical applications?). However Juergen Brugger and co-workers see a large potential for Nano-electro Mechanical Switches owing to the possibility of producing chips which will include a huge number of NEMS.

Spintronics, Collective Spin Devices, Spin Torque Transfer Devices and memories. Spinelectronics merges magnetism with electronics. It already find applications in magnetic disk drives and non-volatile memories (MRAM) and all electronic

designers are dreaming of a universal memory which would combine non-volatility, high speed, high density, infinite cyclability. New MRAM designs may allow achieving this combination of qualities. Apart of this, new applications are emerging for sensing, storing, processing, transmitting information. New architectures mixing functions such as logic and memories in a delocalised geometry are appearing. The position paper written under the direction of Claude Chappert will present us all these directions.

Resistive switches (or: Resistive Random Access Memories, RRAM, or: memristive devices) based on two-terminal nanometre size cells using oxides or higher chalcogenides as active material represents an emerging concept in nanoelectronics. Similar to spintronic concepts, it reaches far beyond the conventional CMOS technology and still can be merged with the technology of today in order to provide a migration path. There are three main variants of memristive systems all of which are utilizing internal redox processes and a related change in the conductance to store the information: Electrochemical metallization cells (ECM, also called PMC or CBRAM) are build from an electrochemically active electrode such as Ag or Cu, a very thin ion conductor, and an inert counter electrode. The anodic dissolution and cathodic recrystallization of the active electrode material leads to the formation of nanofilaments. The electrochemical formation and dissolution of these filaments by bipolar voltage pulses controls the resistance state of the cell.

The valence change mechanism (VCM) uses redox processes in transition metal oxides such as TiO_2 and WO_3 controlled by the local movement of oxygen vacancies - again triggered by bipolar voltage pulses. The thermo-chemical mechanism (TCM) is based on a thermal formation and dissolution of conductive filament in transition metal oxides using unipolar pulses.

Finally, the phase change memories (PCM) represent another unipolar, thermally driven switching mechanism. It is based on the formation of amorphous and crystalline selenides and tellurides which show very different resistivities. The objective EMMA project (www.imec.be/EMMA) in the 6th Framework Program has been the investigation of new solutions for massive non-volatile data storage solid-state memories, based on resistive switching systems. The achievement of this objective was assumed to represent a complete breakthrough in the field of memory devices and related production technologies. The final objectives of the project were (i) the understanding of the memory switching effect and of the electrode materials impact, (ii) the demonstration of the cell functionality with the proposed active material, (iii) the assessment of the manufacturability of the new proposed active materials and electrodes, (iv) the identification of the array architectures, programming and reading conditions, and (v) the reliability issues and scalability of the proposed approach for mass-storage applications beyond the 32nm technological node.

The team - IMEC (Belgium), STMicroelectronics/ Numonyx, Consiglio Nazionale delle Ricerche/MDM, Consorzio Nazionale Interuniversitario per la Nanoelettronica (Italy), and Centre National de la Recherche Scientifique/ IM2NP (France), RWTH Aachen University (Germany) - focused the activities on high-density resistive switching non-volatile memories based on binary resistive switching oxides and CuTCNQ. Among the other topics, special attention was drawn on the physical mechanisms, modeling and scaling of the memory switching process, leading to a physical modeling and enabling evaluating basic scaling potential.

The SRA and position paper on **Mono Molecular Electronics** are presented by C. Joachim and co-workers whereas **Nanophotonics** (Clivia Sotomayor) will be presented together with the last results from the European Technology Platform PHOTONICS 21 Photonics21 (see the PHOTONICS 21 Strategic Research Agenda at www.photonics21.org). Another FP6 programme, MOLOC (www.moloc.ulg.ac.be) - Molecular Logic Circuits - aims at the design and demonstration of the basic principles, feasibility and significant advantages of logic circuits, which emphasize the internal states of a single molecule (or of assemblies of atoms or molecules) as the basic element.

Rather than being used for a mere switching operation, the molecule is designed to act in itself as an entire logic circuit. Molecules (or nano-structures, dopants in bulk material, etc.) exhibit multiple (quasi) stationary states by virtue of their confined size. The consortium, therefore, makes an advantage of the nanoscale, which is imposed by the cardinal technological need to reduce

the size of the circuit. Beyond this, MOLOC further reduces the scale by implementing logic operations directly at the hardware level and by designing circuits in which the logic goes beyond two-valued Boolean algorithms, i.e. the variables are not restricted to be either true (≡ 1) or false (≡ 0). A notable feature of the MOLOC project is the close collaboration between experiment and theory.

During the 2009 meeting of the Theory and Modelling working group the current status of modelling for nanoscale information processing and storage devices has been discussed and the main issues on which collaboration within the modelling community is needed have been pointed out (see also the European initiative http://vonbiber.iet.unipi.it).

An analysis of the current situation in Europe in comparison with that in the rest of the world has been performed, too. The previous version of the present report (resulting from the 2008 meeting) has been updated reflecting the new issues that have been recognized as relevant and of significant current interest. An extended Position paper for the Theory and Modelling Working Group is presented by M. Macucci and co-workers.

Biology applied to information. Over the last decades, tremendous progresses have been achieved in our capability to do work at the nm scale. Design and fabrication of new nano-objects, ingenious and sophisticated experimental set up dedicated to characterize, manipulate and organize matter at nanoscale. Nanosystems and nanoobjects open new area with a dominant role of interface properties increasing the level of complexity. Nanosciences and nanotechnology have a great deal to learn from bioscience, but it might also be the other way around:

Figure 1. Road map for Organic and Printed Electronics showing the variety of applications of this domain. (OE-A 2009)

"unless you can build it yourself, you don't understand it". In other words, by trying to build nanostructures and nanomachines, our understanding of natural complex architectures would greatly increase and generate new insights for the extraordinary complexity we see in Nature.

For these reasons nanoscale bio-medical applications and nano-robotics applied to treatment of information inside the body will be treated during the second year of the coordinated action by a new group headed by Joseph Samitier and Jean Pierre Aimé. This subject will be coordinated together with themes treated below, the Bio-Inspired construction in Electronics and "calculus" with DNA or Synthetic Biology.

Co adaptation of ICT with the ubiquitous world

Besides the above domains related to nanomaterials and to their applications to nanoelectronics, researchers are also interested in other directions. To shed some light on these various orientations, we divide them into domains where technology is already in process development, those with roadmaps already in place and finally those where "weak" signals indicate possible potential in nanotechnologies.

One "pre-industrial" technology: Organic Electronics

In general, technology is used after years of research on materials and on processes and after long discussions on standards (which have to be accepted worldwide). It is only then when the time is appropriate in economic terms that the technology becomes more appealing and the potential applications more unavoidable that it will begin to grow. This was for example the case with liquid crystal displays (LCD) which have taken the place of cathode ray tubes, or with CD taking the place of vinyl disks. This will probably be the case for Organic Electronics and printed technologies. And this has a direct bearing on nanomaterials and ICT. Indeed "Organic Electronics is based on the combination of a new class of materials and large area, high volume deposition and patterning techniques. Often terms like printed, plastic, polymer, flexible, printable organic, large area or thin film electronics or abbreviations like OLAE or FOLAE (Flexible and/or Organic Large Area Electronics) are used, and they essentially all mean the same thing: electronics beyond the classical (silicon) approach" (taken from the recent brochure of the Organic Electronics Association (OE-A), www.vdma.org/oe-a).

Organic Electronics is developing very rapidly as illustrated by the recent success of the Large-area, Organic and Printed Electronics Convention (LOPE-C conference) held in Frankfurt in 2009 (www.lope-c.com/) and by the publication of the 3rd edition of the OE-A brochure "Organic and Printed Electronics" which give an overview of the Organic Electronic Roadmap as provided by OE-A experts (a working group within the VDMA – the German Engineering Federation). The OE-A, is the leading international industry association for organic and printed electronics.

Europe has top-level research laboratories and companies in organic electronics and printing technologies. The objects used by OE are small molecules, polymers, SAMS (self assembled monolayers) and hybrids including nanoparticles like nanowires, nanotubes or quantum dots combined with organic films. This means that OE and molecular electronics share the same background knowledge; however for OE, technologies used for fabrication are low cost ones, like roll to roll or printing technologies very different from techniques used in microelectronics.Due to the inherent control of fabrication at the nanoscale of polymers and molecules in OE, this domain could also move towards deep submicronic (nanoscale) devices fabrication and meet, in the future, molecular scale electronics and "Beyond CMOS" R&D. In this case, the advantages of organic electronics such as flexibility, light weight and low cost would evolve and boundaries between nanoelectronics and organic electronics would begin to blur. Some precursors of this evolution can be found in the recent "OE-A roadmap for Organic Electronics" published version (www.vdma.org/oe-a). But the emergence of a domain where, roughly speaking, organic materials and devices will be merged with inorganic ones (CMOS) is not for tomorrow (even if organic CMOS-like device are now available).

The activity in OE leads to applications for the more mature technologies (OLED, OFET...) as listed just above in figure 1 but also generates new investigation, for example, on new devices such as organic memories or artificial neurones and synapses. These two last developments presuppose that by using nano-structures,

the problem of hyper-connectivity similar to that found in the brain will be solved mainly by using massive 3D circuitry.

One also observes the increasing activity for developing carbon based coherent spintronics (including nanotubes, graphene and organic compounds). Indeed, spin orbit coupling and hyperfine interaction are very small in carbon based materials, which yield very long relaxation times. The manipulation of spins in such new materials could enable the simultaneous combination of memory applications and data processes, opening new avenues for ICTs, including innovation in quantum computing.

Brain-Inspired Electronics

Over the past several years, new institutes on neurosciences are colonising university campuses and hospitals everywhere in the world www.dsv.cea.fr/neurospin/, http://neurosciences.ujf-grenoble.fr/ ... In parallel, simulation studies using massively parallel computation on how our brain is working are developing using large calculus facilities such as in the EPFL Blue Brain Project (http://bluebrain.epfl.ch/) or the FACET research project headed by the Heidelberg University (ftp://ftp.cordis.europa.eu/pub/ist/docs/fet/ie-jan 07-24_en.pdf).

The first project aims at stimulating and exploring the brain activity using (today) 10.000 (virtual) Si - CMOS based neurons wired while the second will develop a Neural Processing Unit to emulate, in high speed, VLSI a large number of Neurons (5x105) and Synapses (109) in order to emulate the neocortex. These two examples are not an attempt to "create" a brain, but these projects together with workshops such as the one on Brain-Inspired Electronic Circuits and Systems (BIECS), www.essderc2009.org/, indicate some guidelines taken by the research on ICT and particularly on the convergence between nanosciences and cognitive sciences aiming at a better knowledge on how the brain is working. However, we are far from being able to put together the pieces of nanomaterials (used in devices exhibiting a neural function), with the ones of architectures (functional building blocks), without forgetting the billions of interconnections between neurones (neurons cells typically form tens of thousands of connections with their neighbours, whereas traditional computer CMOS devices typically possess less than 10 connections). This approach is, with the one on self reproducible cellular automata (see below), one promising way to solve complex problems and is treated in Europe within various FP7 projects and seminars like http://nanoswec2009.cnanogso.org/.

Carbon nanotubes, nanowires, DNA strands, conductive polymers have been envisaged for the dense circuitry of such "computers". Indeed, in relation to these approaches on the brain we can also mention the "bio-inspired nanomaterials and nanosystems" to help fabricate connections, nanostructured materials, templates such as the various scaffolds recently fabricated using DNA knitting. Extension to microscopic materials such as cells or bacteria may even be pursued to develop a technology for processing information by considering them as computers. This is the domain of Synthetic Biology that we will briefly mention later on after some digression on chemistry and biology. Nevertheless, the increased "porosity" of all these domains of investigation allows to cross-develop many applications which are at the frontier between electronics, neuroscience and health such as repair of spinal cord, implantation of artificial retina, stimulation of brain by using µ-nanoelectrodes...). In the previous section we showed some of the contributions of brain research in microelectronics.

Conversely microelectronics enables biology to understand fundamental phenomena. We only mention here as an example the work of P. Fromherz' group which is studying the electrical interfacing of semiconductors and of living cells, in particular of neurons. "The research is directed (i) to reveal the structure and dynamics of the cell-semiconductor interface and (ii) to build up hybrid neuroelectronic networks". (www.biochem.mpg.de/mnphys/).

Chemio and Bio-Inspired construction in Electronics

The biological approach to nanotechnology has produced self-assembled objects, arrays and devices; likewise, it has achieved the chemical identification of inorganic species and the control of their growth in aggregates (dots of gold, cadmium...). Can these approaches now be integrated to produce useful systems?

Introduction

Design and fabrication of new nanodevices is enabled by using objects and techniques from chemistry and biology. A straightforward comparison of materials and tools used in these two domains show that manipulation and organization of matter is possible in both cases at the nanoscale (see table 2). Indeed, various ingenious and sophisticated experiments have been dedicated to the fabrication of scaffolds either for interconnections or for functional building blocks using viruses and DNA. Naturally, Europe has a presence and a FP7 project like "BeNatural", (Bioengineered Nanomaterials for Research and Applications, http://cordis.europa.eu) "uses Nature as a model for New Nanotechnology-based processes" and addresses problems which could be useful for ICT. In particular this is thanks to the possible lower fabrication costs than in standard approaches (see for example the creation of nanoscale shapes and patterns using DNA... (N. Seeman, inventor of DNA nanotechnology at http://seemanlab4.chem.nyu.edu/nanotech.html, P. W. K. Rothemund, (Nature, Vol 440|16 March 2006), A. Turberfield www.physics.ox.ac.uk/cm/people/turberfield.htm.

Two advantages of bio fabrication for electronic devices are that i) it can produce devices which are both nanoscale and complex and then ii) methods exist for their production at large scale and even their reproduction. Further, using interface properties (like membranes) complex problems such as, for example, the communication between various different scales (the nano AND macro-scale) can be handled. Today such interfaces can be optimized through self assembly using aptamers, peptids with phage (cell) display selection or genetic engineering of protein based materials. Applications of chemo and bio-inspired fabrications are no longer purely speculative (A. Belcher, Science 12 May 2006 312: 885-888) and bio-inspired nanotechnology is a rapidly progressing interdisciplinary research field. In the near term, the chief benefits will most likely be in basic research.
However, as nanosystems used in research will be constructed at large scales and commercialized, they will move from gathering basic knowledge in laboratories to collecting and treating data in applied engineering. The first applications could be those in which the relatively high cost and limited capabilities of these first generation devices will still provide significant improvements in overall system capability to justify the cost. Before industrial applications can be developed from nanosciences advances, molecular nanotechnology itself must become a practical discipline instead of just a theoretical one.

Chemical Assemblies	Bio-Chemical Assemblies
Lego® box Conjugated &/or metallated molecules, CNTs, nanowires **Assemblies** SAMs, vesicules, π-Stacking Supramolecular concepts **Motors/actuators** Rotaxane, Catenane, **Replication** Limited (Self catalysis, ...)	**Lego® box** DNA, peptides, proteins, virus **Assemblies** Membranes, cytoskeleton, Virus, ... **Motors** Microtubule/kinesin, Actin/Myosin, ATPase **Replication (by essence)** DNA, cells, virus, living species

Table 2. Comparison of materials, tools, devices and advantages in chemical and bio-chemical assemblies. By courtesy of G. Bidan (CEA-Grenoble)

There are several promising paths to the building of universal assembles among which are: genetic engineering, physical chemistry of biomolecules, use of scanning probe microscopies, and combination of top-down and bottom up approaches. Uncertainty remains as to which path is easiest and quickest, and hybrid approaches appear quite promising, so efforts should be spread across these areas.

Cells and bacteria as reproducible computers

One fairly new approach which mixes engineering concepts developed by Von Neumann about self reproducible cellular automata (von Neumann, J. 1966, Theory of Self-Reproducing Automata, Univ. of Illinois Press, Urbana IL.) and techniques from biology is Synthetic Biology (SB) (see for example : A synthetic oscillatory network of transcriptional regulators, Michael B. Elowitz & Stanislas Leibler, Nature, vol 43, 20 January 2000. Various recent reports, two European ones, from the EMBO organisation www.nature.com/embor/index. html,
"Synthetic Biology, a Nest Pathfinder Initiative" www.biologiesynthetique.fr/uploads/Main/programmes_europeens_07.pdf, and an English one published by the Royal Academy of Engineering www.raeng.org.uk/news/publications/list/reports/

Syn_bio_dialogue_report.pdf together with the following sites give an introduction and overview to the domain and present European activities in SB (www.biologiesynthetique.fr/pmwiki.php/ Main/HomePage and www.synthetic-biology.info/).

The goal of SB is to design complex biological processes by incorporating so-called "bio-bricks" in cells or bacteria (for example, Escherichia Coli) and reproduce organisms acting like computers or machines with the advantage of being self reproducible! The approach is strongly "engineering oriented". Movies of such bacteria which develop the function of emitting a green fluorescence and being reproducible can be found in the recent literature (http://www.nature.com/nature/journal/v456/n7221/extref/nature07389-s03.mov).

They give immediately an enlightened vision of the potential of SB. Other functions such as logic gates, oscillators, inverters, memories... have been built and the parallelism between programming languages for electronics and those used in synthetic biology stressed.

The connections with nanoICT are numerous: first, the synthetic biology community is developing applications reminiscent of what is done in ICT: fabrication of devices, communication, calculus, treatment of information; second, techniques for generating functional genomes and tools like microfluidics, or materials like nanotubes, quantum dots, ... could be used to stimulate, observe, characterize the populations of bacteria "doing their job".

Whether such living objects will be able in the future to solve complex problems such as the one solved by L. M Adleman in 1994 with DNA strands (salesman problem) is not established (Science, Vol. 266, pages 1021–1024; November 11, 1994). But it is probably worth to bring the two communities much closer together because interdisciplinarity will open new tracks for investigation in such domains as production of energy, depollution and treatment of information. Nano-objects might help in measuring and controlling in situ the properties of these micro machines or computers.

Finally one point deserves a special attention. We have seen that in "brain computers" the connectivity problem is crucial. Today, neither DNA scaffolds, nor carbon nanotubes or nanowires can solve this problem. Consequently, architectures have not evolved much over the past 10 years. But here, with cells and bacteria the insertion of information at the nanoscale level (genome) through the nanoscale pores of the membrane is naturally connected to the microscopic scale of the milieu in which these cells and bacteria are living and reproducing: In a certain sense the network of communication allows a transfer of information between the nano and micro-scale and is inherent to the pair "cell/bacteria - environment".

Miscellaneous

A point not covered until now concerns some "new" fabrication techniques used for nanosciences, nanotechnoloies and nanoelectronics. It is worth, aside from the techniques inspired by biology and described in the previous paragraph to mention such keywords as "nano-imprint lithography", "EUV and parallel (maskless) electron beam lithography" (two "rival" techniques using respectively photons and electron beams), "soft lithography", "elastomeric stamping", "self-assembling". All these words refer to techniques for replicating or fabricating structures. Depending on their degree of development they will be used for nanoscale device fabrication in conventional microelectronic processes. But in essence they are not revolutionary as would be DNA assembling or genetic modification of cells and bacteria as in synthetic biology.

Secondly, it is also worth mentioning the opening of microelectronics towards problems of energy. We extract from the recent ICT call "Towards Zero Power ICT" some targets: New disruptive directions are needed for energy-harvesting technologies at the nanometer and molecular scale, and their integration with low-power ICT into autonomous nano-scale devices for sensing, processing, actuating and communication.

Target outcome

a) Foundations of Energy Harvesting at the nano-scale: Demonstration of radically new strategies for energy harvesting and local storage below the micrometer scale. Exploration and harnessing of potential energy sources at that scale including kinetic energy present in the form of random fluctuations, ambient electromagnetic radiation, chemical energy and others. Research may also address bio-mimicked energy collection and storage systems.

b) Self-powered autonomous nano-scale electronic devices: Autonomous nano scale electronic devices that harvest energy from the environment, possibly combining multiple sources, and storing it locally. These systems would co-ordinate low-power sensing, processing, actuation, communication and energy provision into autonomous wireless nanosystems.

Expected impact

- The possibility of building autonomous nano-scale devices (from sensors to actuators), extending the miniaturisation of autonomous devices beyond the level of the 'smart dust'
- New applications in a vast number of ICT fields such as intelligent distributed sensing, for health, safety-critical systems or environment monitoring

  These few words indicate some of the trends already mentioned above such as ubiquity, autonomy, relation with "intelligent" sensing, safety, etc... all aspects important in inorganic ICT, but also for future Bio devices.

Quantum computers

The quantum bit or "Qubit" is the basic memory element of a quantum computer. Some small quantum computers have been built already in the 1990s and various algorithms designed for quantum logic would make it possible to do calculations out of reach for classical computers. Different technologies for "fabricating" the Qubit are available, among them some related to the Nanoscience field. We refer to two roadmaps http://cordis.europa.eu/ist/fet/qipc.htm and http://qist.lanl.gov/qcomp_map.shtml for getting more information related to ICT considerations and some recent progresses done with solid state devices (O'Brien, www.sciencemag.org/cgi/content/abstract/sci; 325/5945/1221 and L. DiCarlo et al., Nature 460, 240 (2009).

Conclusions

To attract the attention of a large spectrum of the scientific ICT community, this survey has been voluntarily written with a broad scope; it is also intended to stimulate critical feedback on the assertion that our group has identified and presented in SRA and position papers. It should encourage nanoICT members to react and identify additional topics which were forgotten. Thanks to this and cooperation among nanoelectronics initiatives and other fields, e.g. chemistry, opto/display electronics, biology, computer science, communication, etc Europe should enhance its knowledge, its capabilities and activities in the field of ICT.

Various scenarios are likely to shape ICT during the two next coming decades. We have seen that technology will at the same time follow the traditional microelectronics trends and depart from it by integration of "More than Moore" tendencies, by adopting and integrating new trends of development (energy, health, environment), and that other incoming technologies such as organic electronics will be major players in treatment of information and communication. Weak signals emitted by Quantum Computing, (mono) Molecular Electronics, Synthetic Biology show that the range of possible futures could be increased and enlarged. Silicon was at the heart of the micro/nano electronics and nanosystems technologies.

Bio-inspired technologies could lead to future developments in the fields of Medicine and Health, Ecology and Energy by nibbling or creating new nanosystems. Well established and new emerging communities of academics, scientists, engineers and others will contribute to this co-evolution between ICT, the needs of our society and new discoveries. Hardware will perhaps include "new" nanomaterials like carbon nanotubes, graphene, nanowires with various elements, organic molecules, quantum dots, biological bricks such as DNA, proteins, viruses and structures like NEMS assemblies, reproducible cells and bacteria, hybrids... Concepts such as "Classical", "quantum", "living" "complex", will also probably be used in these future technical developments aside "information" and "technology".

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2
Strategic Research Agendas

2.1 Carbon Nanotubes

Bill Milne (Cambridge University, UK) and nanoICT Carbon Nanotubes Working Group

Due to the interest generated by the early work on the physical, chemical and electrical properties of Carbon Nanotubes (CNTs), there is a vast amount of research that has been carried out by hundreds of groups throughout the world. This effort has produced countless potential applications in the ICT field, some of which are already in the marketplace, many of which are not far behind with others much further away and many which may never come to fruition.

It is thus very difficult to categorize future research in this field because it is materials-driven, rather than application driven; researchers possess a material for which industry is seeking applications, rather than producing a new device architecture which requires new material to meet the demand.

It is clear that the near-term applications of carbon nanotubes will have/already have a simple structure, do not require specificity and take advantage of their physical and chemical properties such as their shape, inertness, strength and (to some extent) conductivity. These applications vary in market size, but tend to be in smaller niche markets.

Falling into this category are field emitters/ ionizers, sensors, saturable absorbers, batteries/ supercapacitors, thermal management, thin film electrodes, antennae, microlenses and other NEMS applications. These devices do not require the control over the morphology and structure of CNTs that other applications require.

Applications in the more distant future will be determined by whether or not the holy grail of CNT growth, chirality and diameter control are achieved. Applications in this category have the largest potential market: e.g in vias and interconnects, diodes, logic circuits and solar cells. Reproducible, stable functionalization and doping could lead to single and network transistors, drug delivery, hydrogen storage, fuel cells, nanomedicine and nanofluidics. For these applications, much applied science, material and engineering research is still required for realization. The final category, which will not be discussed in detail, includes long-term ICT devices in quantum technologies which require both further research and market identification. If successful, they will be highly disruptive in fields such as sensors and computing.

Near-term applications

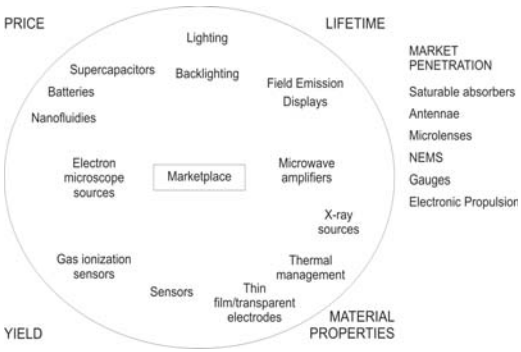

Figure 1. Overview of the possible near-term applications of CNTs. Distance from the centre indicates relative time to market; position dictates the key issues that need to be addressed. Outside the circle, market penetration is the issue, where the proposed devices have yet to justify their application or replacement of an established competing technology.

CNTs have already been added to composites to strengthen sports equipment. They have also been successfully spun into fibres which are being investigated for various applications. Their advantageous electrical conductivity and flexibility means they are already replacing carbon black in carbon brushes, but in the ICT field various factors are limiting the CNT from entering the market. Figure 1 summarizes the major obstacles that exist for various applications.

Emitter lifetime is the primary barrier to field emission applications such as in microscopes, displays, lighting and backlighting. Although the use of CNTs for FEDs seems to be on the wane (for instance, Sony's spin-out company "Field Emission Technologies" announced it was closing down in March 2009 due to the inability to raise capital) their use as efficient backlighting in AMLCDs is still of great interest as is the use of FE-based room lighting. The main issue for CNTs, like other field emitters, is that they are susceptible to damage in the vacuum conditions typically used in these applications. The CNTs can be destroyed by the resulting increased ion impact at higher pressures. Poor vacuum will result in these applications losing out to established technology on cost. They are also competiting with established technologies and face quite a barrier to market.
Supercapacitors and batteries require low-cost, reproducible CNT production over large areas to become viable alternatives to devices already available. Nanofluidics also loses out on cost and requires greater uniformity in the grown CNTs. For electron microscope sources, CNTs with high tolerances are required. Consequently, yield is the major issue. There is insufficient control over the CNT's dimensions at the moment even with the most successful reported methods of production.

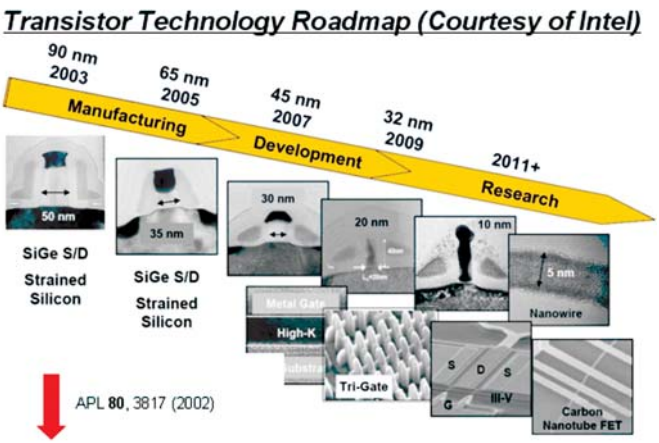

TABLE 1. Comparison of Key device performance parameters for a 260 nm long top gate *p-type* CNFET, a 15 nm bulk Si *p-type* MOSFET[a], and a 50 nm SOL *p-type* MOSFET[b].

	p-type CNFET	15nm bulk Si p-type MOSFET	50nm bulk SOI p-type MOSFET
Gate length (nm)	260	15	50
Gate oxice thickness (nm)	15	1.4	1.5
V_t (V)	– 0.5	– – 0.1	– – 0.2
I_{on} (μA/μm)	2100	265	650
($V_{ds} \equiv V_{gs}$-Vr ≈ -1 V)			
I_{off} (nA/Um)	150	<500	9
Subthreshold slope (mV/dec)	130	~100	70
Transconductance (μS/μm)	2321	975	650

Figure 2. Transistor Technology Roadmap (courtesy of Intel). If the current trend in channel width were to be maintained, CNTs would be required by 2025.

Other applications need further research into the improvement of overall properties. Gas ionization and other sensors suffer from poor selectivity and, in the case of ionization, efficiency. Functionalization of CNTs would be hugely significant in both cases, as would experimentation with device geometry but this would lead to a significant increase in the cost of ownership.

Greater packing density of CNTs is required for improved efficiency of thermal management devices, and though transparent electrodes are more durable than ITO, they aren't as transparent at similar conductivities and are reported to suffer from birefringence which is a problem for some display applications.The use of CNTs as electron sources in microwave amplifiers is exciting but bandwidth still requires optimization. High-current X-ray sources utilize similar technology, but work is still ongoing into harnessing the high current densities that planar CNT field emitters can produce.

Finally, many proposed devices have yet to establish a market and thus face a large barrier to entry. Sensors, saturable absorbers and electronic propulsion have relatively small or fragmented markets with a few players.

The application of CNTs to antennae is in its infancy although the technology for device fabrication is effectively developed. There seems to be little need for CNT gauges. NEMS and microlenses have yet to find a feasible application in their current form.

More distant applications

CNTs have been mooted as the ultimate solution to continued semiconductor scaling as devised in Moore's law (see figure 2). As semiconductors, the high mobilities of single CNTs and their small dimensions would produce devices much faster than today, but the market inertia is colossal. Even if the questions of chirality control, reproducible contacts, doping and large-scale positional control were answered, a complete overhaul of semiconductor industrial fabrication would be required for integration. If in the medium term, CNTs were employed to complement silicon, post-fabrication devices would require the maximum growth temperature to be 400ºC. Currently, CNTs grown at these temperatures do not produce optimal device characteristics because of a high defect density. The same applies for CNTS applied to vias and interconnects.

Network transistors are more reproducible but suffer poor on-off ratios (related to the metallic CNTs always being present due to a lack of chirality control), larger surface area and would have to be produced very cheaply to be justified, in areas such as flexible electronics for instance. They currently do not significantly improve on incumbent classical electronic technology. CNTs are amongst a number of materials being investigated for solar cells. Solar cells are one of the most intensively researched areas in ICT at present, but research into using the CNT as the active layer has waned recently.

The material which produces the greatest efficiency at a low price first will be employed. In fuel cells, CNTs have been found to have little net benefit, but more research is needed in this area. IR absorbance, doping and functionalization would greatly enhance the likelihood of tumour treatment, drug delivery and nanomedicine. Long-term health implications of CNTs are currently being explored and the possibility remains that they may not be suitable for this application.

Theoretically, CNTs should be excellent for hydrogen storage because of their large surface area; however, it is no better than activated carbon which is much cheaper to produce. Hence, research in this area continues to be disappointing, since their capacity isn't significantly better than incumbent technology. Finally, from the engineering point of view, the heat transfers involved in this hydrogen storage approach make it difficult to both get the hydrogen in and back out within the timeframe required by industry.

Conclusions

For CNTs there will always be the possibility that they may be more harmful to health than they are currently considered to be. Indeed, if ongoing research into their nanotoxicity finds this, the provision of sufficient protection for researchers may be too high for many research institutions to bear. For industry, extra health and safety costs may also adversely influence the price of all the devices proposed above. In the short term, institutions should be prepared to deal with this possibility.

2.2 Modelling

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There are several challenges that need to be addressed in the next few years in the field of nanoscale device modelling, involving the integration of different dimensional scales and of different expertises, which in some cases range far away from traditional device physics or device simulation.

Indeed, there is is clear need to make tools for the simulation of nanoscale devices predictive in terms of quantitative results and to integrate them within simulation hierarchies paralleling what already exists in terms of modelling for conventional device design. Models should shift from the idealized structures that have been explored in the past in order to grasp an understanding of principle of operation, to realistic device concepts in which i) coupling to phonons (with equilibrium or non equilibrium distributions) is fully taken into account, ii) thermal transport is handled on a parallel footing with respect to electric transport, iii) an ab-initio treatment of transport at the molecular level is included, with specific provisions for the interaction of molecules with substrates and metallic electrodes, iv) interfacing to bio-molecules is treated in a rigorous fashion, v) issues of spin transport, especially at interfaces, receive a proper quantum treatment, vi) coding is done exploiting the most cost/effective hardware that is available. In the following we try to provide an overview of most relevant tasks that face modelling for nanoscale information devices in the upcoming years; the presentation will be divided into sections, but distinctions between different fields of modelling (i.e. semiconductor devices, molecular devices, carbon based electronics, etc.) tend to become more and more blurred, since there is a convergence resulting from the common dimensional scale and the increasing application of ab-initio techniques to all fields.

Modelling for molecular electronics

Concerning the understanding of transport properties of molecular junctions, from the point of view of the first-principles calculations, there are several important challenges that need to be tackled during the next few years. Probably one of the most important is the ability to accurately predict the spectrum of electronic excitations for molecular systems on surfaces and metallic junctions. The correct alignment of the molecular levels with the electronic states of the metal is a prerequisite to have quantitative calculations of the transport properties in molecular systems, as well as for a correct estimation of the interface dipoles formed at the boundary between molecular layers and metal substrates. To date, most first-principle transport calculations are derived from electronic band structures obtained using Density Functional Theory calculations within the Kohn-Sham formulation using local or semi-local exchange-correlation functionals.

These calculations are well known to have severe limitations to correctly describe the energy positions of the molecular levels of small molecules. Furthermore, the effect of the dynamical screening by the metallic leads also causes a substantial modification of the position of the molecular levels, affecting in a different way the HOMO and the LUMO of the molecule.These effects are at the heart of many of the current disagreements between theory and experiment in the field of molecular electronics. Therefore, it is necessary to develop methods to include these effects, methods which should be, at the same time, sufficiently accurate and computationally efficient.

Another important issue is the coupling of the electronic degrees of freedom with vibrations. At present, non-equilibrium Green's functions (NGEFs) methods mainly considered the case of small electron-phonon coupling that can be treated perturbatively. This has already allowed for a satisfactory description of the inelastic tunneling spectroscopy in many systems. However, the regimes of intermediate and large electron-phonon coupling are quite relevant for organic systems, nanotubes and graphene, and are far more difficult to treat. In particular, the possibility to perform reliable transport simulations (at the level of DFT or beyond) in the presence of strong electron-phonon couplings is well beyond the existing capabilities.

A related issue is the formulation of schemes to perform reliable simulations of the coupled dynamics of electrons and nuclei. There are many subtle technical and basic difficulties behind these simulations. Many of these

difficulties are related with the classical limit usually assumed for the description of the nuclear dynamics (Born-Oppenheimer approximation).

The electron-ion coupled dynamics is interesting in many fields, including photochemistry, but in particular could provide a route to estimate the effects of temperature in the electronic transport in molecular junctions and the related dissipation issues. In general, the incorporation of different sources of inelastic scattering is a very interesting and active area of research that will allow going beyond the assumption of ballistic transport behind most first-principles NGEFs simulations to date and to address other regimes of transport. The joint modeling of charge and spin transport through molecular junctions possesses very strong challenges. The main issues are due to the electrode-molecule contact topology, the atomistic and electronic structures of the electrodes and molecule, the dynamical effects, and time dependent fields. Also, the effects of structural fluctuations via molecular dynamics simulations have to be addressed. The numerical implementation of these issues requires very efficient and accurate algorithms as well as the design of multiscale computational approaches, for eventually tackling more realistic description of materials and devices of technological concerns. A parallel but more demanding line of research to molecular electronics is bio-electronics. The theoretical understanding of the bio/inorganic interface is in its infancy due to the large complexity of the systems. Determining the charge migration pathways in bio-molecular systems is a crucial point, and due to the highly dynamical character of bio-molecular systems the electronic structure is strongly entangled with structural fluctuations. Therefore multi-scale simulation techniques are urgently required, which should be able to combine quantum-mechanical approaches to the electronic structure with molecular dynamical simulation methodologies dealing with the complex conformational dynamics of biological objects. Recent advances have been achieved on DNA molecules, and mote developments are necessary in the field of organic crystals/molecules, especially in low dimensionality.

Modelling for carbon-based nanoelectronics

Graphene doping and decoration

Important experimental results achieved in the last few years have further raised the interest in carbon-based nanoelectronic devices, in particular in the graphene material system. The many advantages of graphene, such as the very high electron mobility, are unfortunately offset by the fact that it is a zero-gap material, and therefore it is very difficult to achieve a modulation of conductivity (and on/off current ratio) large enough to be useful for digital applications. It has been suggested that doping would allow opening up a gap in bulk graphene and would enlarge the already existing gap of graphene nanoribbons. Considering the difficulties involved in an experimental verification of this effect, it would be essential to have a detailed theoretical understanding, in order to provide clear and detailed indications to experimentalists. Such an understanding must be rooted in ab-initio approaches, in order to be reliable, but must then be implemented in such a way as to be useful for efficient simulation of complete devices, for which a full ab-initio treatment would not be possible.

A multi-scale approach is therefore needed, with the extraction and validation of parameters from more refined techniques and their inclusion into more computationally efficient approaches, such as tight-binding. This will require a coordinated multidisciplinary effort with the contribution from different types of expertises, including chemical physics, electronic structure calculations, electron device simulation, solid state physics. These techniques should also be applied to the investigation of the potential of new proposed materials, such as graphane, interest in which is rising both in terms of its usage as an insulator or as a hydrogen storage medium.

Spin-based devices

Novel transport functionalities involving the spin of the carriers have very recently received a particularly strong attention in the BEYOND-CMOS area. For instance, conversion of spin information into large electrical signals using carbon nanotubes and graphene, or the observation of long spin relaxation times have suggested that carbon based materials (including organic materials) could drive the development of coherent spintronics at room temperature, including joint integration of memory storage and data processing devices. The convergence between spintronics and organic electronics will also open new horizons for low-cost technology and applications in the ICT field.

However charge transport phenomena in these materials require advanced theoretical description of

novel electronic states of matter such as massless Dirac fermions or polaronic states. To date, despite an increasing concern from the scientific community, efficient simulation tools with true predictive capability for assessing real devices functionalities are lacking. Particularly in Europe, first-principles calculations have been steadily improved to tackle with complex materials, including the treatment of spin degree of freedom. For instance, very large values of magnetoresistance have been predicted in ideal graphene nanoribbons-based spin valves, and many other appealing predictions on simplified device configuration have been reported.

However, the great challenge to overcome lies in the simulation of the full-device including self-consistent calculation of charge/spin flows and device characteristics, with realistic material description (including spin-orbit couplings, disorder, interfaces, etc.). To date, no simulation tool can tackle both spin injection at complex material (ferromagnetic/semiconductors) interfaces, along with the non equilibrium spin transport along the channel, including spin decoherence mechanisms at a first principles level. In the near future strong development of first principles non-equilibrium transport methods would be needed to allow for more realistic assessments and predictions of the true spintronics potential of carbon-based structures. This will stand as a critical issue for providing guidance and interpretation schemes to experimental groups.

Thermal transport

Being one of the areas in which nano-scale fabrication techniques offer a breakthrough in device performances, nano-thermoelectrics is a rapidly growing topic of research and development. Quasi one-dimensional disordered quantum wires, engineered molecular junctions, superlattices of quantum dots are the possible routes proposed for achieving high thermoelectric figure of merit. An accurate modeling of large disordered or self-assembled structures is required to guide experimental efforts. For this, fully parallelized O(N) methods for both electronic and phononic computations are needed.

Computational Issues

The computational effort needed for a quantitatively reliable simulation of nanoscale devices is steadily increasing as dimensions are scaled down and new physical phenomena have to be taken into account, thereby requiring more elaborate numerical models. In order to cope with this exploding need for computational resources, it is important to be able to take advantage of the most advanced computational platforms available.

One important aspect is the networking of European excellence in Nano-ICT simulation with the existing Pan European Research Infrastructure on High Performance Computing Centers (www.hpc-europa.eu/).

Such facilities allow for the most cutting edge advances in large scale computing, and should also entail great benefits to simulation at the nanoscale.
Additionally, a new and important platform, which has already been applied to several fields of computational science, is represented by Graphic Processor Units (GPUs). Indeed GPUs offer large scale parallelism at the low cost afforded by very large scale production; their processing units are specifically designed to perform matrix operations, which do represent a very significant portion within modeling codes. This means that large speedups are to be expected, and some initial tests have demonstrated factors up to 40 - 50. It is therefore important to fully assess the possible impact of this new technology and, if the preliminary evaluations are confirmed, to invest heavily in the development of optimized codes, implementing advanced simulation strategies for the device structures of main current interest.

Furthermore, it is essential that some device concepts will finally move from the research field to that of actual development and industrial exploitation: to this purpose it is essential that engineers will have advanced simulation codes available and that they will be able to run them for realistic device structures, with the possibility of exploring a vast parameter space. This is not likely to happen if simulation codes will run on supercomputers, because the availability of such facilities is expected to be limited also in the future. GPU based computation may represent the answer, if modeling codes are successfully developed on such a platform, because it will offer the required computational power at a cost accessible even to small companies.

It is however important to stress that there is still a lack of coordination of simulation tools development and implementation in the Information and Communication Technologies European programs. The emergent Spanish initiative named M4NANO (www.m4nano.com) is also complemented by other national research programs and networking such as IUNET in Italy or the NANOSIMULATION program launched by the CEA (France), but some European scale frame is lacking.

2.3 Mono-Molecular Electronics

Marek Szymonski Jagiellonian University (Krakow, Poland) and nanoICT Mono-Molecular Electronics Working Group.

Introduction

Future information technologies undoubtedly require radically new ideas and approaches in order to go beyond the conventional boundaries of ICT. Present day, transistor-based technology soon will meet the limit of its miniaturization. It is dictated by the fact that there is a certain, minimum number of atoms on the surface of a semi-conductor required to define the structure of a transistor in a currently accepted form.

Already in the second half of the 20th century concepts of using molecular devices instead of conventional ones in hybrid electronics have appeared and been studied since then(see for example famous Aviram and Ratner paper [1]).

Recently a brand new modus operandi has been proposed. Namely, the idea of integrating the elementary functions and interconnections required for desired computation into a single molecule [2].This proposal is not limited to computational tasks, i.e. electronics and telecommunication, only. Atomic and molecular scale devices may be designed as mechanical machines and transducers as well (see for example [3]).

Challenges of the single molecule based electronics

Here we focus on the concept of the single molecule electronics. The core of the single molecule electronics is an idea to design a molecular processor that would be incorporated into the future nanoelectronic device, interconnected with other elements of the system and especially with an output interface. A preliminary task, that will not be discussed further, is the design and synthesis of the molecule with desired properties. Assuming that one possesses the molecular processor of advantageous features, several technical obstacles arise.

Single molecule manipulation and imaging

First of all, one has to master single molecule manipulation and imaging on various substrates to a very high level of precision. Depending on the substrate of choice the means of imaging and manipulation will be different, namely STM for conducting and semi-conducting surfaces or nc-AFM for insulators. Combining the standard scanning probe techniques with new methods such as tip-enhanced Raman spectroscopy will greatly increase measurement precision.

A scanning tip induced manipulation of single molecules has already been confirmed for various systems and may be considered the state-of-the-art, therefore the possibility of manufacturing molecular assemblies with the tip is at hand (see for example [4]). In this context, the technological challenge that remains to be tackled is the automation of the manipulation process to such a degree that it will allow its industrial implementation. However, this task cannot be realized separately from other important issues concerning the single molecule based devices, that will be discussed below.

There are also other ways of realizing desired molecular assemblies on the surface. Namely, intensively studied self-assembly process, or the idea of the on-surface-chemistry. In the former case, either one would have to modify/functionalize the surface in such a manner that will guide the self-assembly or find the set of adsorption parameters that lead to the formation of the desired nanostructure (see for example [5-7]).

On the other hand, the concept of the on-surface-chemistry requires a careful choice of the substrate that will play a role on the reaction platform and the reactants that will undergo a chemical change in the assumed reaction and finally will form a desired structure or compound directly on the surface. The on-surface-chemistry approach depends strongly on the cross-pollination between physicists and chemists.

Connecting to the outer world

Next crucial aspect of the single molecule electronics is the ability to connect the molecular processor to the outer world in order to benefit from its computational properties. Successful communication between the nano- and micro- environment of the molecular electronic device is a decisive parameter for this approach. One has to realize not only interconnections between elements of the whole instrument, but especially with a tool's output interface. These two

types of interconnections would require different approaches, that may sometimes overlap. First, networking the molecular circuit elements may be realized with use of molecular wires fabricated as described in the preceding section (see for example [7]). However, from time to time one may need to provide not only horizontal connections, but also transversal conductive bridges spanning two different levels of the substrate. Precisely controlled processes of creating such a molecular interconnects inside of a device are of great importance for future technological applications. Search for such processes is challenging and requires close cooperation of chemists, on one hand, that design and synthesize molecules, and physicists, on the other hand, that test their assembling properties.

Second, connecting to the outer world would be based on molecular wires only to some extent. Namely, molecules could be used to connect to some kind of nano-metallic electrodes, that further evolve into micro-electrodes and allow addressing the device. Fabrication of gold nanowires on InSb by means of thermally-assisted assembling process seems to be a promising solution for such a task [8]. However, other realizations of the proposed scenario based on different materials are needed.

The final element of connecting the molecular processor to the outer world will depend on the single molecule manipulation discussed before. Achieving a technologically feasible route that integrates the manufacture nano- and micro-metallic pads with assembling of molecular wires, and deposition and positioning of all other molecular elements of the device is a very challenging, complex and high-risk task.

Device reliability

Previously considered problems of positioning of the molecule in the required place within the electronic circuit or interconnecting it with metal electrodes, are not the only difficulties faced by single molecule based electronics. It is obvious that properties of the molecular processor would rely on its internal structure. Nevertheless, the shape of the molecular orbital and the electronic structure are very vulnerable to the interaction with the chemical surrounding of the molecule and may be changed by interaction with it [9, 10]. That, in turn, implies alternation of the way the molecular processor operates as well.

Therefore, the next critical issue emerges. In particular, before very sophisticated molecular electronics systems are designed and fabricated, the role of the interaction between the molecule and its surroundings must be comprehended. Subsequently, one has to develop schemes for avoiding a strong coupling of molecules with the substrate on which they are deposited. Two separate approaches to achieve this goal have recently been undertaken.

One involves deposition of ultrathin insulating layers between the conducting or semi-conducting substrate and the molecule. It has been shown that at least partial decoupling of the molecule in such a configuration is feasible [11]. The other approach is based on the design and synthesis of molecules equipped with spacer groups that in principle should increase the separation between an active molecular board and the substrate.

A whole family of such molecules, namely, the Lander molecules family has been already synthesized and examined on various templates [4, 12-14], being at the moment regarded as prototypes of large organic molecules consisting of a planar polyaromatic molecular wire and equipped with spacer groups. Although much progress has been done in understanding the molecule-substrate interaction and some ideas of decoupling the molecules from the surface have been tested, present knowledge in this field is still far from being complete or even sufficient.

Conclusions

Presented analysis of the single molecule based approach to molecular electronics does not cover all possible technical obstacles arising upon experimental realization of that idea. However, highlighting only three issues, namely: the single molecule manipulation and imaging, the outer world connection and device reliability, is enough to express the complexity and high-risk nature of that topic. On the other hand, the successful realization of the single molecule based electronics will be a way to overcome current limitations in miniaturization.

Furthermore, it will not only result in an increase in computing power by orders of magnitude and therefore directly influence the development of ICT, but it will also open up the field of mechanical machines and transducers to atomic and molecular scale devices. As

an added value, the knowledge gained during examination of the molecule-substrate interaction could be utilized in the field of surface functionalization, that is a fundamental tool in making advanced materials of desired bulk and surface properties and devices of advantageous features.

That in turn influences many areas of technology such as solar cell industry, ceramics, gas and biosensors, just to mention a few. Although all pointed issues are crucial in developing single molecule based devices, one of them could be addressed in the FET 2011-12 Workprogramme, namely the device reliability issue. Such a choice is dictated by the fact, that each development in that particular field will have the biggest potential to influence other research areas. Exploration in that case could be realized by means of small projects <3M€ - 3 yrs.

The other points, single molecule manipulation and imaging and the outer world connection, could be studied jointly in later Workprogrammes depending on the output of the projects devoted to the device reliability. Achieving technologically feasible route that integrates the manufacture of nano- and micro-metallic pads with assembling of molecular wires, and deposition and positioning of all other molecular elements of the device, is a very challenging, complex and high-risk task.

Therefore, it should be realized as large projects: 4-6 M€ - 4-5 yrs. Moreover, as the aim would be to build a working prototype of single molecule based device and to prove its technological feasibility, the participation of high-tech companies in this research is necessary.

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2.4 Nano Electro Mechanical Systems (NEMS)

Juergen Brugger (EPFL, Switzerland) and nanoICT NEMS Working Group.

In contrast to micro/nanoelectronics, Micro- and Nano Electro Mechanical Systems (MEMS/NEMS) have been since the beginning a very multidisciplinary field with very disperse technologies. This has made somehow difficult to define precise roadmaps that foresee the development of MEM devices, and now the same issue is found for NEMS. The two main applications that have been spotted and are confirmed are sensing and electronics.

NEMS Sensors

Figure 1 shows the evolution of the mechanical sensors from MEMS to NEMS, which includes not only a reduction in size but also a real breakthrough in the applications and the signal to noise ratio that is achievable.

NEMS for electronics

The other main application, more related to the ICT, is to use NEMS for electronics, i.e. to use NEMS for the same functions that currently are performed using CMOS circuitry. Examples of these functions would be the fabrication of NEM-FET, NEM-based D/SRAM, NEM relay logic, etc. Inherent to any of those applications lays one of the main challenges for the future of NEMS, which is the monolithic integration with CMOS at large scale of mechanical devices.

Several groups have been working in the integration of mechanical systems and CMOS, but the number of mechanical elements was always much smaller than the number of transistors and was limited to a few tens per wafer. A clear example is the Analog Devices (ADXL50) accelerometer; with only 1 to 3 on-chip MEM structures of lateral dimensions on the order of 100 µm (see Figure 2).

Radio Frequency MEMS for different applications (tunable capacitors, high-Q inductors, filters, micro-switches, etc.) have been also integrated with CMOS improving the performance of existing and future

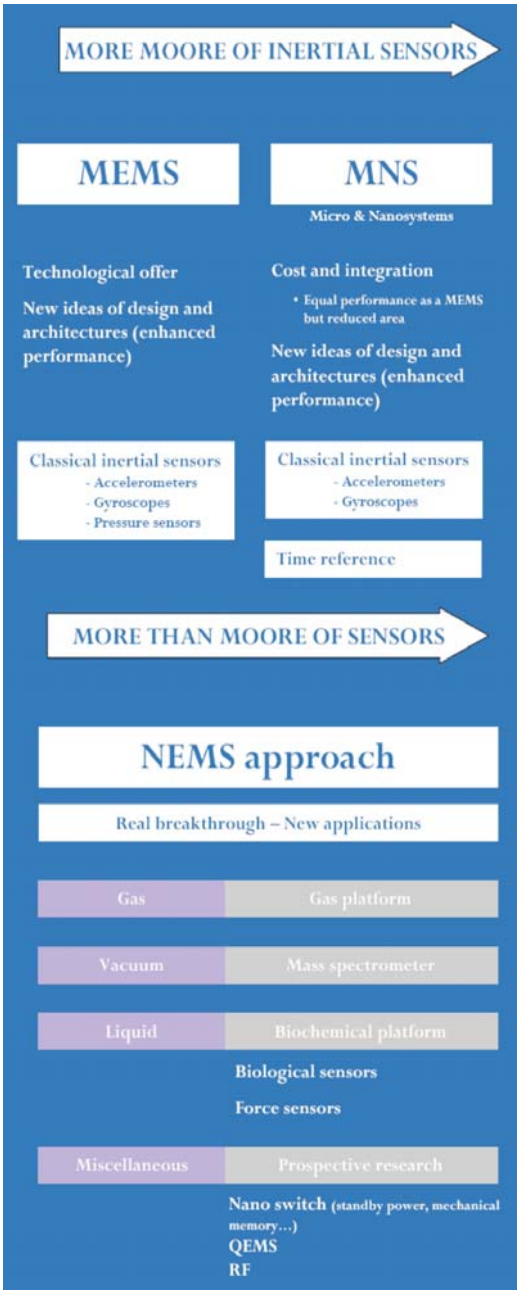

Figure 1. Shows the evolution of the mechanical sensors from MEMS to NEMS, which includes not only a reduction in size but also a real breakthrough in the applications and the signal to noise ratio that is achievable.

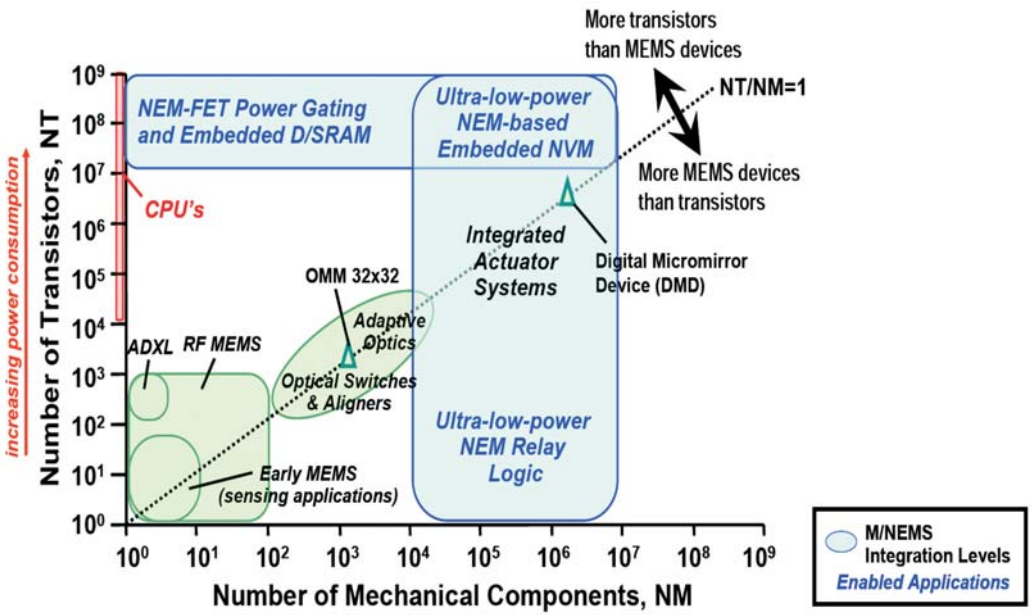

Figure 2. Summary of state of the art and future devices as a function of the number of transistors (NT) and the number of mechanical components (NM). Source: ITRS whitepaper authored by A. Ionescu (EPFL) et al.

wireless transceivers. The challenge will be then to achieve the integration of a much larger number of mechanical components with a high number of transistors, following the path marked by Texas Instrument with their digital micromirror device (DMD) for projection displays (see Figure 2).

With a relatively small number of NEM-FET switches (10^3) the CMOS power consumption could be managed and reduced, which will lead to a new and more energy efficient generation of chips. By increasing the number of mechanical devices (up to 10^7) it would be possible to obtain embedded (mechanically-based) memory.

Moreover, arrays of NEM relays could be used for ultra-low-power logic once contact reliability issues are resolved. Finally, NEM structures are also attractive for non-volatile memory (NVM) applications because much lower energy would be necessary to program them as compared with standard current memories.
The integration of NEMS with CMOS will also be radically beneficial for sensing applications, where it has been demonstrated that on-chip signal processing (amplifiers, filters, A/D converter, etc.) enhances the resolution by reducing the influence of external noise sources. That, combined with the fact that using an array of η mechanical sensors in parallel increases the signal to noise ratio by $\sqrt{\eta}$, will result in unprecedented sensing performance.

However, in order to achieve this goal, it is very important to develop standardized NEM fabrication process flows in a similar way as it is currently stipulated in CMOS foundries, otherwise the integration will not be viable. In some cases, it may not be necessary (or even possible) to have the CMOS and NEM processing in a single foundry.

In that case, the combination of a CMOS foundry and a NEMS foundry would be necessary, which will also imply the compatibility of wafer sizes between both foundries. In addition to a reduction of costs, standardized fabrication process flows will also allow the development of SPICE models and CAD tools for NEMS which will ease the system design, analysis and verification.

3

Annex I
NanoICT Working Groups position papers

3.1 Carbon Nanotubes

W.I. Milne[1], M. Mann[1], J. Dijon[2], P. Bachmann[3], J. McLaughlin[4], J. Robertson[1], K.B.K. Teo[5], A. Lewalter[3], M. de Souza[6], P. Boggild[7], A Briggs[8], K. Bo Mogensen[7], J.-C. P. Gabriel[9], S. Roche[10] and R. Baptist[11]

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[4]University of Ulster, UK
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KeyWords

Growth
Carbon nanotubes, multiwall, singlewall, nanofibres (all the words in a and the subtopics), cap structure, catalysts, adhesion, mechanism, modelling.

Post-growth modification
Doping & functionalization, dispersion and separation, purification, annealing, cap opening/closing, graphitization.

Properties/Characterization
Defects, electron transport, phonons, thermal properties/conductivity, wetting, stiction, friction, mechanical, chemical properties, optical, toxicity, structural properties, contacts.

Electronic applications
Field emission (X-ray, Microwave, FEDs, Ionization, Electron microscopy), interconnects, vias, diodes, thin-film transistors, thin-film electrodes, network transistors, single CNT transistors, thermal management, memory.

Optical applications
Absorbers, microlenses in LCs, optical antennae, lighting.

Electromechanical applications
NEMS (resonators), sensors, nanofluidics, bio-medical.

Energy applications
Fuel cells, supercapacitors, batteries, solar cells.

Blue sky
Spintronics, quantum computing, SET, ballistic transport.

1. Introduction

There has been extensive research into the properties, synthesis and possible applications of carbon nanotubes (CNTs) since they came to prominence following the Iijima paper [1] of 1991 [2]. Carbon nanotubes are composed of sp2 covalently-bonded carbon in which graphene walls are rolled up cylindrically to form tubes. The ends can either be left open, which is an unstable configuration due to incomplete bonding, they can be bonded to a secondary surface, not necessarily made of carbon, or they can be capped by a hemisphere of sp2 carbon, with a fullerenelike structure [3].

In terms of electrical properties, singlewalled CNTs can be either semiconducting or metallic and this depends upon the way in which they roll up, as illustrated in Figure 1. Multi-walled CNTs are non-semiconducting (i.e.

semimetallic like graphite) in nature. Their diameters range from 2 to 500 nm, and their lengths range from 50 nm to a few mm. Multi-walled CNTs contain several concentric, coaxial graphene cylinders with interlayer spacings of ~0.34 nm [5]. This is slightly larger than the single crystal graphite spacing which is 0.335 nm.

Studies have shown that the inter-shell spacing can range from 0.34 to 0.39 nm, where the inter-shell spacing decreases with increasing CNT diameter with a pronounced effect in smaller diameter CNTs (such as those smaller than 15 nm) as a result of the high curvature in the graphene sheet [6,7]. As each cylinder has a different radius, it is impossible to line the carbon atoms up within the sheets as they do in crystalline graphite. Therefore, multi-walled CNTs tend to exhibit properties of turbostratic graphite in which the layers are uncorrelated. For instance, in highly crystallized multi-walled CNTs, it has been shown that if contacted externally, electric current is generally conducted through only the outermost shell [8], though Fujitsu have been able to contact the inner walls with resistances of 0.7 kΩ per multi-walled CNT [9]. This position paper summarizes state-of-the-art CNTs dependent on the nature of the desired end-structure. It also summarizes possible electrical, electronic and photonic applications of carbon nanotubes (excluding bulk material composite applications).

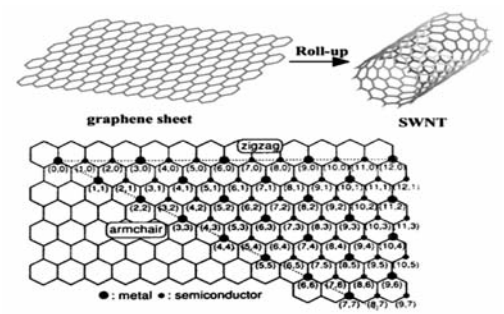

Figure 1. (top) A graphene sheet rolled up to obtain a singlewalled CNT. (bottom) The map shows the different single-walled CNT configurations possible. Were the graphene sheet to roll up in such a way that the atom at (0,0) would also be the atom at (6,6), then the CNT would be metallic. Likewise, if the CNT rolled up so that the atom at (0,0) was also the atom at (6,5), the CNT would be semi-conducting. The small circles denote semiconducting CNTs and the large circles denote non-semiconducting CNTs. Two thirds of CNTs are semi-conducting and one third metallic [4].

2. Catalyst preparation

The catalyst metals most commonly used for nanotube growth are Fe, Ni and Co [10]. There are several routes to the production of catalyst nanoparticles, the two main methods being the wet catalyst method and the coalescence of thin catalyst films. The wet catalyst method involves the deposition of metal nitrate/bicarbonate colloids onto a surface (shown in Figure 2a). On drying, the salt in the solution crystallizes to form small islands of the metal salt. The salt is reduced to a metal oxide by heating or calcinations and the oxide is then reduced by H_2 and/or thermal decomposition resulting in the formation of metallic catalyst islands from which the CNTs grow [11,12]. The wet colloid method produces an uneven distribution of catalyst particles, but does have a significant cost advantage over vacuum techniques such as sputtering and evaporation.

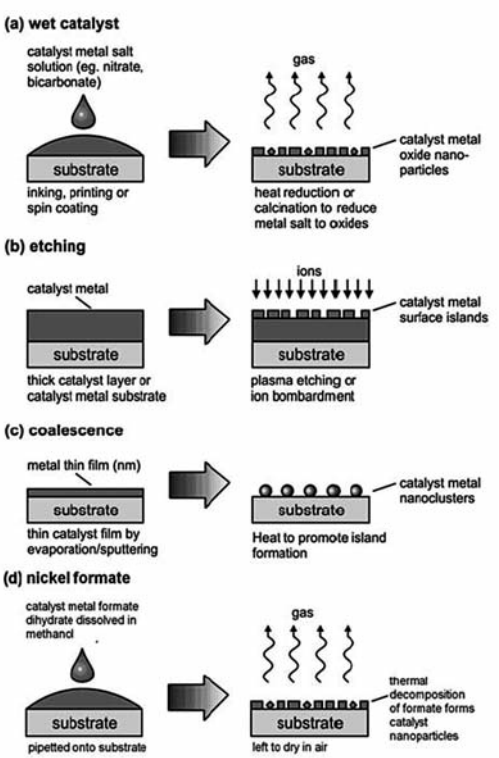

Figure 2. Methods of producing nano-sized catalysts for nanotube growth [13-16].

The most commonly used form of catalyst preparation for devices is coalescence (shown in figure 2c). A thin film (of thickness typically less than 10 nm) of Fe, Co or Ni is deposited onto a substrate by evaporation, sputter coating or electroplating. Upon heating, the thin film breaks up (known as dewetting) to form nanoislands as a result of increased surface mobility and the strong cohesive forces between the metal atoms [17,18]. CNT growth then nucleates from these nanoislands. When grown on silicon and polycrystalline substrates, barrier layers such as ITO, SiO_2 and TiN are required to prevent diffusion of catalyst into the substrate [19].

2(a) Catalyst for SWNT growth

CNT growth is affected by the catalyst and thus different catalysts are required to produce different CNT structures. Metal underlayers also affect resultant CNT growth [20]. Typical catalysts favoured for SWNT growth are an Al/Fe/Mo triple layer 10 nm, 1 nm and 0.1 nm thick respectively with the Mo layer on top [21]. This produces dense, vertically-aligned, SWNTs grown attached to the substrate. For epitaxial growth on quartz, only a thin layer of Fe is required. Resasco [22] uses a Co catalyst in the patented CoMoCat process on a silica substrate with a high purity, low diameter distribution of SWNTs as a result.

Others use Ni as a SWNT catalyst. The use of ferritin as the catalyst reported by Dai [23] and Rogers [24], or of polyoxometallates [25] enables tighter control of the catalyst particle size and thus the CNT diameter. For electronic applications, when the substrate is to play an insulating role, particular attention needs to be paid to the quality of the substrate as well as to the thermal treatment of the wafer in order to minimize the diffusion of catalyst into the substrate and to keep leakage current low. Dubosc et al. [26] have demonstrated the use of electrochemical deposition of Ni catalyst with the resultant CNT growth indistinguishable from catalyst deposited by other methods.

2(b) Catalyst for MWNTs

Catalyst thicknesses required for MWNT growth tend to be much greater than that for SWNT growth because catalyst thickness correlates with CNT diameter. Ajayan [27] reported the growth of MWNTs using ferrocene and xylene by CVD with the Fe contained within the ferrocene as the catalyst. This produces the best MWNTs if no patterning is required. For surface-attached growth, Ni, Fe and Co are the most commonly used catalysts, but the quality of the resultant MWNTs depends on the research group and there is little to discriminate between them for CVD processes.

However, for plasma-enhanced CVD (PE-CVD), most groups tend to favour Ni catalyst since they produce the straightest MWNTs with the greatest control over growth rate.

2(c) Placement/patterning of catalyst

For device-based applications it is desirable to position the catalyst on the substrate where CNTs are required to grow. The most desirable positioning method is by lithographical means, where optical or electron beam lithography exposes spin-coated resist followed by development, catalyst deposition and lift-off, which leaves behind catalyst deposited on developed areas. CNTs can then be grown in-situ where desired for device fabrication. This has been done most effectively by Teo et al. [28], where single, vertically aligned MWNTs were grown single Ni catalyst dots deposited on silicon (as shown in figure 3).

Many others have used this process to demonstrate positional growth of CNTs [29,30]. Very large scale integration of SWNTs at the 100 mm wafer level were reported in 2001 using deep UV lithography [31] and using a more standard available lithography process in 2003 [32]. Porous substances such as alumina have been used to grow CNTs with catalyst deposited in the pores. The resultant CNTs grow with the support of the pore walls that act as a template for growth [34]. Pores can also either be etched into silicon [35] or milled with a focused ion beam [36].

Catalyst can also be positioned by imprinting, where catalyst deposited on templated silicon is pressed onto a substrate [37]. Laser interferometry can also be used to position catalyst but only for array-like structures and with a spacing no greater than the size of the dot [38]. The use of nanosphere lithography for self-assembly of nanotube arrays have also been demonstrated by Ren et al [39].

European Position: Bernier and Loiseau optimised catalysts for arc production.

The USA with CoMoCat and HipCo as well as Hata in Japan with supergrowth have dominated the optimisation of catalysts for mass production CVD growth. Europe has made significant contributions to low T growth as well as controlled, patterning for multi-walled CNT growth.

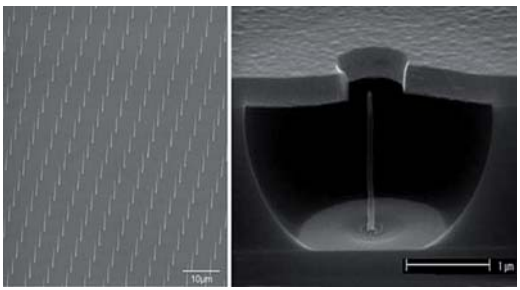

Figure 3. (a) Array of MWCNTs of height 5 μm and separation 5 μm[28] (b) Individual MWCNT grown in a micropore etched into SiO2 using a self alignment method [33].

3. Growth

The quality of grown carbon nanotubes is subjective, since their quality depends on the structures required. Some applications require high purity and crystallinity; others require tight dimensional control, whilst others might require high packing densities and/or alignment. Consequently, the state of the art depends on the type of structure required. The latest research indicates that, contrary to prior understanding, carbon nanotubes do not follow a vapour liquid solid (VLS) growth model, but rather a vapour solid solid (VSS) model. Hofmann et al. [40] have observed growth of both single and multi-walled carbon nanotubes in-situ in an environmental electron microscope. In all cases, the catalyst particle remains solid, with crystalline structure clearly observed. This indicates that growth primarily occurs through surface diffusion rather than the bulk diffusion proposed by Baker [10].

3(a) Single-walled CNTs

(i) State of the art for bulk single-walled growth

The highest quality single-walled CNTs (in terms of defects) are produced by laser ablation, a process developed by Smalley [41], in which the diameter of the grown CNT can be controlled by temperature. A composite graphite target made of Ni and Co produces the best CNTs with a yield of 70%. This is, however, the most expensive common production process. The highest purity CNTs nucleate from catalysts in a fluidized bed and are currently sold by Thomas Swan [42]. The process produces high-quality CNTs, inexpensively in large quantities [43]. In Windle's group CNTs are also grown in a continuous flow furnace. The nanotubes are created rapidly by injecting ethanol and ferrocene into a furnace at 1,200º C. An aerogel then starts to stick to the cooler wall in the furnace to form fibres. A spindle then winds the aerogel fibres into a thread, at several centimetres per second. The result is an extremely fine, black thread consisting of aligned CNTs [44]. Nanocyl also produce purified singlewalled nanotubes [45].

(ii) Vertically aligned single-walled CNTs

Water/oxygen/ethanol assisted growth provides amongst the longest vertically-aligned CNT mats produced and has been carried out by a number of groups including Maruyama and Dai [46], but it is Hata who can produce the longest CNTs with a carbon purity of 99.98%. The process uses ethylene as the carbon source gas with a small amount of water vapour incorporated into a hydrogen flow process. However, there is little control over growth rate because the mechanism is not clearly understood [47].

(iii) Horizontally aligned single-walled CNTs

Horizontally-aligned SWNTs have been grown on epitaxial surfaces such as sapphire and quartz with varying densities. The growing CNTs follow the crystal planes with a great degree of alignment. The process is standard CVD but the substrate needs to be annealed for surface reconstruction before growth. Among the best, Tsuji's group have grown on sapphire [48] and the Rogers group, who have grown on quartz [24] (figure 4).

Dai et al. have grown horizontally-aligned CNTs with the use of electric fields (figure 4). However, the fields only align metallic CNTs. Semiconducting CNTs are not affected by the field. Gas flows have also been used to control the horizontal alignment of SWNTs, but the flow needs to be very high and the degree of alignment is poor compared with methods mentioned above [49]. Most recently Hata has used a vertical

alignment and then by dipping in alcohol the tubes get aligned in plane by capillary forces when he pulls up the substrate from the liquid [50].

(iv) Challenges for SWNTs

The key challenges with SWNTs concern control of chirality during growth. For applications such as transistors, all grown CNTs need to be semiconducting (and preferably of identical chirality) whilst for interconnects, all CNTs need to be metallic. Control of diameter is related to this issue. The possibility of using very long CNTs cut into many pieces has been discussed as a possibility for chirality control in CNT devices, by using the pieces to act as catalysts for identical tubes. However, the chirality of some CNTs has been found to change along long CNTs (being caused by structural defects [51]). Returning to interconnects, a higher density (of ~ 1013 tubes/cm^{-3}) than that achieved so far is required if it is to replace copper. The yield of SWNTs grown with templates is very low and must be solved if it is to be seriously considered as a method for growing SWNTs. Also, for SWNT growth to be combined with CMOS, the temperature needs to be reduced to ~ 400 ºC.

To a certain extent the chirality problem has been overcome by using devices based on random network of nanotubes instead. This approach was first brought to light by Snow and co-workers in 2003 [52] although it was patented by Nanomix in June 2002 [53].

3(b) Multi-walled CNTs

Though Endo started the injection process, for bulk growth, the best CNTs are again grown by Thomas Swan (as a result of rigorous qualification by Raman and TEM) and Windle's group in Cambridge, though Hyperion [54] are the leading suppliers of nanofibres using a similar process to Thomas Swan. So-called Endo-fibres 150 nm in diameter can also be purchased from Showa Denko. Bayer produce narrower "Baytubes" 5-20 nm in diameter [55], but these are impure and need to be purified.

(i) Vertically aligned (including crowding)

There is typically no alignment of CNTs with the CVD process. The grown CNTs are often randomly orientated and resemble spaghetti. However, under certain reaction conditions, even in the absence of a plasma, closely spaced nanotubes will maintain a vertical growth direction resulting in a dense array of tubes resembling a carpet or forest. For this, the ferrocene-catalyzed growth of Ajayan produces MWNTs with the best control over diameter, height and with the greatest degree of alignment [56].

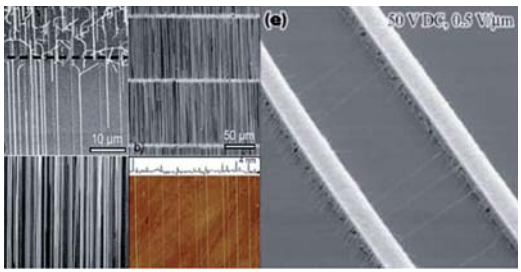

Figure 4. (a-d) CNTs grown along quartz crystal planes by the Rogers group [24]. Reprinted with permission from Coskun Kocabas, Moonsub Shim, and John A. Rogers. J. Am. Chem. Soc. 2006, 128, 4540-4541. Copyright (2006) Americal Chemical Society, (e) Horizontally aligned CNTs grown by Dai's group using field to align the CNTs [49]. Reused with permission from Yuegang Zhang, Applied Physics Letters, 79, 3155 (2001). Copyright 2001, American Institute of Physics.

In plasma-enhanced chemical vapour deposition (PECVD), the applied plasma creates a sheath above the substrate in which an electric field perpendicular to the substrate is induced. The deposition gases are broken down by a combination of heat and plasma and vertically aligned CNTs grow following the induced field. For vertically- aligned arrays of single or multiple MWNTs, Teo et al. [57] are able to control diameter (σ = ±4.1%) and height (σ = ±6.3%) by placing the catalyst by lithographical means and by positioning the substrate on a driven electrode and within the plasma sheath during a PECVD process.
Both CVD and PECVD hold a number of advantages over other synthesis methods. For tip growth, nanotube length increases with deposition pressure, and linearly with deposition time up to certain lengths [58]. The diameter is controlled by the thickness of the catalyst deposited and the position of the CNTs can be controlled by controlling the catalyst position. For instance, lithographical techniques can

be employed to deposit catalyst dots to control the position of grown CNTs that can be employed in field emission devices [28]. This results in much more control over the dimensions of the CNTs and removes the need to purify and separate CNTs grown by other methods.

(ii) Challenges for multi-walled CNTs

Some of the challenges for MWNT growth are identical to that of SWNT growth. Growth temperature needs to be reduced if CNTs are to be employed in CMOS. Raman spectra of MWNTs grown by CVD/PECVD at low temperatures show them to be highly defective. Post-annealing processes can increase graphitization, but these are typically at temperatures much higher than circuitry can withstand. There is also the question of contact resistance that is often quite high and variable. This needs to be addressed with still further improvements on dimensional control.

European Position: Europe led the way with research in arc deposition but commercialisation was limited. More recently Nanocyl [45], Thomas Swan [42], and Arkema [59] and Bayer [55] have made significant contributions to up scaling CVD and recently AIXTRON [60] and Oxford Instruments [61] have begun to provide large area PECVD capability.

The leading universities in Europe will include Cambridge Univ., Dresden and EPFL. Growth of MWNTs on large wafers (200mm) is now routinely done at various locations for microelectronics applications (see for example, images of CVD reactors at CEA-Grenoble in figure5). The aerosol-assisted CCVD process allowing the production of carpets of aligned nanotubes is produced at CEA-Saclay in the group of Martine Mayne (and can be seen in figure 6).

4. Post growth modification

CVD generally produces the poorest quality CNTs with the greatest number of defects. When the growth process ends, power is shutdown and the substrate allowed to cool, but this often results in the deposition of amorphous carbon around the CNT. This can be removed either by hydrogen or ammonia plasma, or a rapid thermal annealing process that also increases the graphitization, conductivity and contact of the CNT [62].

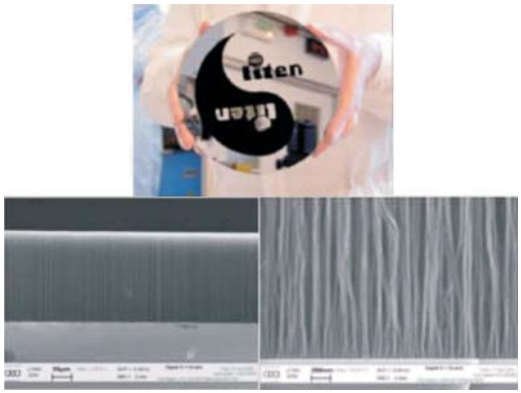

Figure 5. Dense forest of Small diameter MWCNT from left to right: a) Patterned layer on a 200mm layer b) 50µm high forest on conductive layer of TiN c) close view of the material with individual CNT making bundles of 60nm of diameter (courtesy of CEA-LITEN).

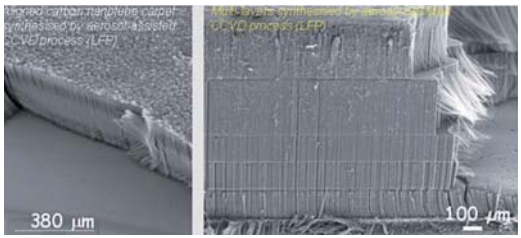

Figure 6. images showing the growth of CNT carpets grown by an aerosol-assisted process.

For CNTs grown by arc discharge and laser, various techniques have been employed to purify, given the best samples are only 70% pure (using laser ablation), with the remainder made up of amorphous carbon. CNTs are first dispersed by sonification [63]. The gas-phase method developed at the NASA Glenn Research Center to purify gramscale quantities of single-wall CNTs uses a modification of a gas-phase purification technique reported by Smalley and others [64], by combining high-temperature oxidations and repeated extractions with nitric and hydrochloric acid. This procedure significantly reduces the amount of impurities such as residual catalyst, and nonnanotube forms of carbon within the CNTs, increasing their stability significantly. Once the CNTs are separated, the use of a centrifuge enables the isolation of certain chiralities of SWNTs, particularly (6,5) and (7,5) as shown by Hersam's group at North

Western University [65]. This method seems to be the way forward for scalable chirality separation.

European Position: The US lead the way in novel techniques based on density differentiation but in Europe, Krupke, Knappes and co-workers at Karlsruhe pioneered the dielectrophoresis method.

5. Doping

Conventional doping by substitution of external impurity atoms in a semiconductor is unsuited for CNTs, since the presence of an external atom breaks the ideal symmetry properties in the CNT. Theoretically, substitutional doping by nitrogen (n-type) and boron (p-type) has been widely examined [66-71]. Adsorption of gases such as H_2, O_2, H_2O, NH_3, NO_2 have been reported in [72-75]. More appropriate doping strategies which conserve the mean free path of the charge carriers involve physisorption of alkali metal atoms [76-91]. Alkali-metal atoms located outside or inside the tube act as donor impurities [92,93] while halogen atoms, molecules, or chains act as acceptors [76,84,94,95]. Fullerenes or metallofullerenes, encapsulated inside CNTs, allow good structural stability and have been used to tune the band gap and/or Fermi level of the host tube [96-99].

"Doping" by physisorption of molecules, lies at the heart of a growing field of chemical sensors, but there are issues with stability.

European Position: In Europe Maurizio Prato's group in Trieste is the most successful in this area.

6. Oxidation/Functionalization

CNTs can be oxidized by various means. Refluxing in acids such as nitric or sulphuric, or with potassium manganate adds functional groups to the CNTs that alter the wetting angle.
The caps of CNTs can be opened either by physical means or more commonly, by chemical means, in which the cap is opened by heating CNTs in the presence of a oxidizing gas such as oxygen or carbon dioxide.

Open-capped CNTs, unless functionalized, are unstable structures because of dangling bonds. Cap closing of open-capped structures often occurs during field emission.

De Jonge et al. [100] demonstrated this happens for currents as low as 80 nA per tube. The chemical inertness and low surface energy of the graphitic structure of the CNT is not conducive to functionalization. Recent progress in solubilisation has facilitated chemical functionalization of SWNTs for various applications such as catalysis, catalysts support, sensors, gas storage, highperformance composites, biological and organic/inorganic compounds [101-111]. Most functionalization methods involve strong acid treatment of the CNT producing extensive nanotube breakage. A class of functionalization reactions that does not involve acid treatment is the direct addition to the π-electrons of the CNT [112,113]. The main approaches for functionalization can be grouped into the following categories:

(a) the covalent attachment of chemical groups through reactions onto the π-conjugated skeleton of CNT;

(b) the non-covalent adsorption or wrapping of various functional molecules; and Within category (a) reports of fluorination [114,115], atomic hydrogen [116], aryl groups [117], nitrenes, carbenes, and radicals [118], COOH [119,120], NH2 [121] N-alkylidene amino groups [122], alkyl groups [123] and aniline [124] amine and amide [125] have been reported. Within category (b) are included grafting of biomolecules such as bovine serum albumine [126-128] or horse spleen ferritin [129], poly-Llysine, a polymer that promotes cell adhesion [130,131], Streptavidin [132] and biotin at the carboxylic sites of oxidized nanotubes [133] and polymers [134-139].

European Position: Haddon and co-workers in the US were early leaders and Carroll and co-workers in Wake Forrest University applied functionalization to devices. In Europe Hirsch in Erlangen has made major contributions and Coleman and co-workers at TCD have furthered our knowledge in this area.

7. Properties/Characterization

CNTs typically have a Young's Modulus ~10 times that of steel [140] and an electrical conductivity many times that of copper [141]. Some important properties of CNTs are listed in table 1.

The properties of CNTs are determined by a number of methods. Electronic properties are determined by

adding contacts and the use of probe stations. It should be noted that a drawback to this method is the variability in contact quality that can cause significant variance in measured attributes. Raman spectra are used to characterize defects in the CNTs; the higher the Id:Ig ratio, the lower the number of defects. Also, radial breathing modes can be used to characterize the diameter distributions of the grown CNTs in a sample [144, 145].

The band structures of all single-walled CNTs can be summarized using the Kataura plot [146].

MECHANICAL PROPERTIES	
Young's modulus of multi-walled CNTs	~1-1.2 TPa
Young's modulus of single-walled CNT ropes	~1 TPa
Tensile strength of single-walled nanotube ropes	~60 GPa
Stiction	~10^{-7} N on 5 μm latex beads[i]
Hydrophobicity	161° contact angle[ii]
THERMAL PROPERTIES AT ROOM TEMPERATURE	
Thermal conductivity of single-walled CNTs	1750-5800 WmK
Thermal conductivity of multi-walled CNTs	>3000 WmK
ELECTRICAL PROPERTIES	
Typical resistivity of single- and multi-walled CNTs	10^{-6} Ω m
Typical maximum current density	10^{7}-109 A cm^{2}
Quantized conductance, theoretical/measured	$(6.5\ k\Omega)^{-1}/(12.9\ k\Omega)^{-1}$ per channel
ELECTRONIC PROPERTIES	
Single-walled CNT band gap	
Whose n-m is divisible by 3	0 eV (metallic)
Whose n-m is non-divisible by 3	0.4-0.7 eV (semiconducting)
Multi-walled CNT band gap	~0 eV (non-semiconducting)

Table 1. Summary of main properties of CNTs [19].

8. Electronic applications

Various applications for CNTs in the ICT field have been touted but in the near term only a few of these seem feasible: their use in field emission applications and their inclusion in the production of transparent conductors and in interconnects and vias seem most probable.

8(a) Field emission

Field emission from CNTs can be applied to many technologies because of their high-current-carrying capability, chemical inertness, physical strength and high aspect ratio. The major applications are listed below.

(i) Field emission displays

Motorola in the early/mid 1990's investigated the use of carbon based materials for Field Emission Displays including the use of diamond, DLC and CNTs [147,148]. More recently they have reported a CNT based Field Emission HDTV [149].

Over the last 10 years or so various companies including Philips, TECO Nanotech, ISE Electronics and especially Samsung (SAIT) [150] have worked on the use of CNTs for TV applications. SAIT successfully produced demos of full colour 39"diagonal TVs and this technology was transferred to Samsung SDI for production in the mid 2000s. However, no displays based on this technology are yet on the market. More work continues on Field Emission displays but the only recent major announcements are on SEDs (Surfaceconduction Electron-emitter Displays).

Formerly a collaboration between Toshiba and Canon, the displays utilise emission from carbon but not CNTs [151]. Legal disputes have prevented this from coming to market thus far. Most recently, Sony have announced a major investment in FEDs based on a Spindt process. Teco Nanotech Co Ltd (a small company based in Taiwan) also market three basic CNT-based FEDs, the largest being 8.9" diagonal [152]. CEA (France) continue to fund research in this area, with typical displays produced shown in figure 7.

Figure 7. Two stages of development of CNT FED at CEA. On the left: monochrome display with 350μm pixels, on the right: color video display with 600μm pixels. On these display the non uniformity from pixel to pixel is 5% while it is 3% with LCD displays and 2% for CRT (courtesy of CEA-LITEN).

(ii) Microwave generators

High power/frequency amplifiers for higher bandwidth, more channels and microwave links are increasingly using the 30 GHz and above frequency range. In order to satisfy the power (tens of Watts) and bandwidth requirements (30 GHz), satellites are

using travelling wave tubes (TWTs) based on thermionic cathodes. Present day TWTs, however, are bulky and heavy, and take up valuable space and weight budget in a satellite, and any miniaturization of the current TWT would give rise to cost savings in a satellite launch and aid the implementation of microsatellites.Solid state devices are not used in this high frequency regime because the maximum power attained by solid state devices today at 30 GHz is ~1 W.

Attempts have been made to replace the thermionic cathode in a TWT with a Spindt tip cathode delivering the dc electron beam. However, the bulk of the TWT device is still there, since it is the tube (in which the electron beam modulation takes place) that is physically large. The most effective way to reduce the size of a TWT is via direct modulation of the e-beam, for example, in a triode configuration using CNTs as the electron source.

Thales, in collaboration with Cambridge University Engineering Department, have successfully demonstrated a Class D (i.e. pulse mode/on-off) operation of a carbon nanotube array cathode at 1.5 GHz, with an average current density of 1.3 A/cm^2 and peak current density of 12 A/cm^2 (see figure 8); these are compatible with travelling wave tube amplifier requirements (>1 A/cm2) [153].

Recently, they have also achieved 32 GHz direct modulation of a carbon nanotube array cathode under Class A (i.e. sine wave) operation, with over 90% modulation depth. This unique ability to directly modulate or generate RF/GHz electron beams from carbon nanotube emitters is especially important for microwave devices as it essentially replaces the hot cathode and its associated modulation stage [154].

Other advantages that carbon nanotube cathodes offer include no heating requirement and the ability to turn on or off instantly (for efficient operation). Because of their small size, and their ability to generate and modulate the beam directly on demand without the need for high temperatures, CNT cathodes could be employed in a new generation of lightweight, efficient and compact microwave devices for telecommunications in satellites or spacecraft. Xintek have also been working on CNT-based microwave amplifiers for the US Air Force [155]. The main problem at present is the limited modulation bandwidth associated with such devices.

(iii) X-ray Instruments

Oxford Instruments have worked together with NASA on CNT-based X-ray sources that employ field emission as the electron source, rather than thermionic emission, which has much lower power efficiency [156].

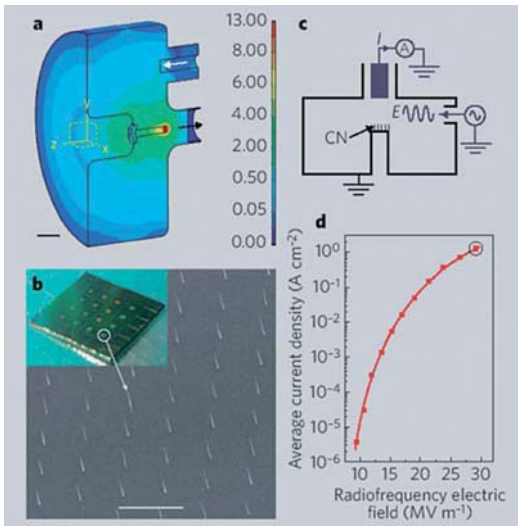

Figure 8. Simulation of the coaxial resonant cavity (a crosssection is shown) that was used to generate a high electric field (red) at the carbon-nanotube-array cathode from the radiofrequency input; colour scale shows the applied macroscopic electric field in volts (105) per metre. White arrow, coaxial radiofrequency input; black arrow, emitted electron beam, collected by an antenna; scale bar 10 mm. b) Electron micrograph of the carbon-nanotube-array cold cathode at a tilt of 45°. The carbon nanotubes have an average diameter of 49 nm, height of 5.5 μm and a spacing of 10 μm; scale bar, 15 μm. Inset, photograph of 16 cathodes. c) Representation of the equivalent electrical circuit, where E is the applied electric field and I is the emitted current; CN, carbon nanotube array. d) Measured average current density plotted against applied radiofrequency electric field using 1.5-GHz sinusoidal input. The circled point corresponds to I=3.2 mA. The cavity-quality factor was 3,160 [153]. Reprinted by permission from Macmillan Publishers Ltd: Nature, K.B.K. Teo, E. Minoux, L. Hudanski, F. Peauger, J.-P. Schnell, L. Gangloff, P. Legagneux, D. Dieumgard, G.A.J. Amaratunga and W.I. Milne. "Microwave Devices: Carbon Nanotubes as Cold Cathodes", Nature 437, 968 (2005), copyright 2005.

Their application is targeted towards lowpower use for a space mission to Mars (though high power would be more preferable), once again because of their low weight and fast response time.

Oxford Instruments have also developed and sold hand-held low power X-ray imagers which can be applied to medicine and for diagnostics in circuit boards [157]. Zhou and co-workers at Xintek (see figure 9) have developed a fast response, sharp-focus X-ray tube with quick pulsation [158]. MoXtek have also produced similar devices [159].

Challenges for these devices are in achieving high power with stability and reproducibility.

(iv) Ionization for propulsion and detection electric propulsion

Replacing hollow and filament cathodes with field emitter (FE) cathodes could significantly improve the scalability, power, and performance of some meso- and microscale Electric Propulsion (EP) systems.

There is considerable interest now in microscale spacecraft to support robotic exploration of the solar system and characterize the near- Earth environment. The challenge is to arrive at a working, miniature electric propulsion system which can operate at much lower power levels than conventional electric propulsion hardware, and meets the unique mass, power, and size requirements of a microscale spacecraft. Busek Company, Inc. (Natick, MA), has developed field emission cathodes (FECs) based on carbon nanotubes [160]. The non-thermionic devices have onset voltages about an order of magnitude lower than devices that rely on diamond or diamond-like carbon films.

Worcester Polytechnic Institute (WPI) falls under the programs headed by Professors Blandino and Gatsonis. Blandino's research is largely focused on the study of colloid thrusters for small satellite propulsion, and in the development of novel, earth-orbiting spacecraft formations [161]. The Gatsonis activity also includes modelling of plasma micropropulsion [162].

Groups from the Rutherford Appleton Laboratory [163] and Brunel University [164] are studying Field emission performance of macroscopically gated multi-walled carbon nanotubes for a spacecraft neutralizer.

Gauges/Sensors

The Physical Metrology Division, Korea Research Institute of Standards and Science are using the field emission effect of a carbon nanotube to characterize a new type of technology for detecting low pressure. The fabricated low pressure sensor is of a triode type, consisting of a cathode (carbon nanotubes field emitter arrays), a grid, and a collector.

The gauge has a triode configuration similar to that of a conventional hot cathode ionization gauge but also has a cold emission source. Due to the excellent field emission characteristics of CNT, it is possible to make a cost effective cold cathode type ionization gauge. For an effective CNT cathode they used the screen-printing method and also controlled the collector and the grid potentials in order to obtain a high ionization current.

They found that the ratio of the ionization current to the CNT cathode current changes according to the pressure in the chamber [165].

Miniaturised gas ionization sensors using carbon nanotubes

Ajayan et al. from the Rensselaer Polytechnic Institute have developed Ionization sensors work by fingerprinting the ionization characteristics of distinct gases [166]. They report the fabrication and successful testing of ionization microsensors featuring the electrical breakdown of a range of gases and gas mixtures at carbon nanotube tips.

The sharp tips of nanotubes generate very high electric fields at relatively low voltages, lowering breakdown voltages several-fold in comparison to traditional electrodes, and thereby enabling compact, battery-powered and safe operation of such sensors.

The sensors show good sensitivity and selectivity, and are unaffected by extraneous factors such as temperature, humidity, and gas flow. As such, the devices offer several practical advantages over previously reported nanotube sensor systems. The simple, low-cost, sensors described here could be deployed for a variety of applications, such as environmental monitoring, sensing in chemical processing plants, and gas detection for counter-terrorism.

McLaughlin and Maguire [167] at University of Ulster report the use of CNT's in order to decrease the turn-

on voltage associated with microplasmas and the enhancement of emission spectra associated with gas types. In particular the device focuses on mixed gas types such as breath analysis and environmental monitoring. The ability of low cost CNT structured electrodes is key to improving performances related to higher sensitivity and specificity of gases such as NOx. Catalyst free growth techniques have been reported using thermal CVD routes and the study is also looking at the optimum CNT spacing and height required for short time ionisation or FE applications to gas sensors. The main driver at present is to improve the efficiency which currently lies at around 1%.

(v) Backlighting

Although their use in full colour TVs is still problematical, the use of CNTs as electron emitters in FE-based backlight units for AMLCDs is still under investigation by various companies worldwide. Major players in the TFT-LCD display industry, such as Samsung, Corning and LG Electronics (LGE), are keen to develop carbon-nanotube (CNT) backlight modules, with Taiwan-based backlightmodule makers also interested in following suit [168]. In Korea Iljin also have several years of experience in this area [169].

In theory, CNT backlight modules have a lower temperature, consume less power and are less expensive to produce than traditional backlight modules. It is a good candidate to eventually replace CCFL (cold cathode fluorescent lamp) backlighting but has strong competition from LEDs, which could be much cheaper to produce. The challenges are again to improve the lifetime of the emitters and to reduce cost to be competitive with other technologies.

(vi) Electron microscopy

Electron microscopy demands a bright, stable, low-noise electron source with a low kinetic energy spread to maximise spatial resolution and contrast. Recent research has investigated whether the carbon nanotube can act as an improved electron source for this application and how it compares to the other electron sources available today.

Various groups from FEI, CUED, EMPA, El-Mul etc. Have researched the optimum way to produce CNTs for use in microscopy. The most detailed analysis was carried out by De Jonge and co-workers and the field emission properties of CNTs collated from all of de Jon

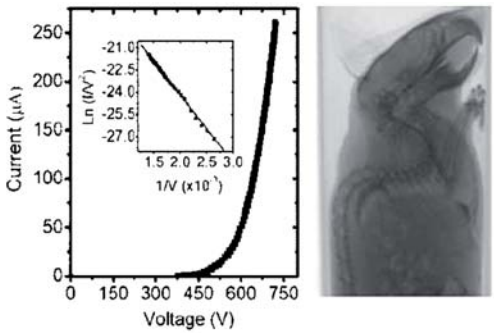

Figure 9. Left, the x-ray tube current versus the gate voltage measured with the anode voltage fixed at 40 kV. It follows the classic Fowler–Nordheim relation. The distance between the cathode and the gate is 150 μm. Right, X-ray image of a normal mouse carcass (25 g) obtained using a CNT source-based imaging system [158]. Reprinted with permission from J Zhang, Rev. Sci. Instrum. 76, 094301 (2005). Copyright 2005, American Institute of Physics.

ge's papers [170] for their use in SEM/TEM sources are summarized below:

Reduced Brightness/($Asr^{-1}m^{-2}V^{-1}$)	10^9
Energy Spread/eV	0.25 - 0.50
Short-term stability %	0.2
Running Temp/K	700 - 900
Vacuum Level/mBar	$< 2\times10^{-8}$

iVirtual source size is analogous to the effective emitting area on the surface of the carbon nanotube in which the advantage lies in this area being minimized.

The CNTs act as a cold cathode source and the standard manufacturing procedure is to add them to the tip of a standard tungsten emitter. Several different methods of attachment/growth have been attempted. Teo et al. used a carbon glue to attach the CNT to the tungsten tip. Growth, rather than attachment is felt to be a better process. Riley et al. [171] have shown that a forest of highly efective CNTs can be grown on a tungsten tip by thermal chemical vapour deposition (TCVD), but in order for electron beam equipment to work effectively, there must be only a single source of electrons, hence a single CNT on each tungsten tip. Mann et al. [172] therefore used PECVD and describe how such a procedure is scalable with the ability to grow a single

CNT on each W tip (shown in figure 10). It is also possible to grow many tips simultaneously. El Mul has developed a silicon-based CNT microcathode in which the CNT is grown in an etched pore [173].

Though the emission characteristics of the CNT have been found to be extremely promising with the attachment process has been essentially overcome. Progress is also being made in improving stability and reproducibility.

European Position for Field Emission and Applications

From a display viewpoint Europe were very much forerunners but then Samsung provided the more recent display drive. As regards work on sources for electron microscopy in Europe De Jonge and co workers did some excellent work on characterisation of single emitters as did Groning on arrays of emitters. Thales in collaboration with several universities have continued European interest in the design of high frequency CNT based sources. For X-ray sources Oxford Instruments led the way and more recently Xintek in the US and Philips in Europe have expanded the work. In backlighting as in Displays the Far East leads the way. The leaders in the FE based propulsion area are in the US where the Jet Propulsion Laboratory Pasadena, Busek Co., Inc. and the Worcester Polytechnic Institute (WPI) lead the way. In Europe the main groups are from the Rutherford Appleton Laboratory, Brunel University, the University of Groningen, and the University of Ulster.

8(b) Interconnects, vias

In order to achieve the current densities/conductivity needed for applications in vias, dense arrays of CNTs are required. Very dense arrays of nanotubes have been grown by chemical vapour deposition (CVD) by various groups, following Fan et al. [174]. They are called forests, mats or vertically-aligned nanotube arrays. They are usually multi-walled and grown from Ni, Co or Fe catalysts.

It has been suggested that a nanotube density of at least 1013 cm^{-2} was needed in order to produce the required conductivity but recently Fujitsu have indicated that 5x1012 cm^{-2} would be acceptable [175]. However growing such dense arrays in vias of high aspect ratio is not so straightforward. Numerous groups worldwide are trying to optimise the process including CEA but Fujitsu [176] (see figure 11) have reported the most significant advances and have recently reported that they have achieved a density of 9x1011 cm^{-2}. They have also reported a resistivity of 379 μΩcm for a via 2 μm in diameter. A Microwave CVD method was employed to produce CNTs at temperatures compatible with CMOS. However, much improvement is still required before these become a practical proposition.

Figure 10. Left, electron micrograph of a single CNT grown on a tungsten tip. Note that the growth is aligned with the tungsten axis. Centre, a tungsten tip mounted in a suppressor module. Right, a CNT grown on a tungsten already mounted in the suppressor in situ.

Problems include choice of catalyst, catalyst deposition, depositing top contacts, increasing the packing density and reducing the overall resistivity. The growth also needs optimization for back-end processing and must be carried out at low enough temperatures so as not to damage CMOS. If SWNTs are to be employed, the packing density of metallic tubes must be high enough to justify replacing metal interconnects. For MWNTs, for a sufficient current density, internal walls must also contribute to conduction. Neither have as yet been achieved.

European Position: Infineon identified Vias as a possible early application of CNTs in electronics, Intel in the US evaluated spun-on CNTs for contacts but more recently Fujitsu. Japan lead the way.

8(c) Transparent, conductive contacts/membranes

As the use of ITO becomes ubiquitous and indium becomes more scarce and thence more expensive there is an ongoing search for alternative transparent conducting contact materials. Initiated at Nanomix [178], various groups worldwide including those of

Rinzler, Roth, Chhowalla and Grüner have worked in this area to replace indium tin oxide (ITO) in e.g. LCDs, touch screens, and photovoltaic devices.

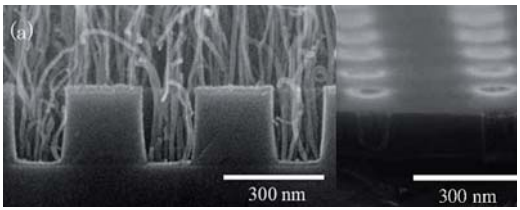

Figure 11. Left, CNT vias grown in pores etched into silicon [177], © [2007] IEEE. Reprinted, with permission, from M. Nihei et al., "Electrical Properties of Carbon Nanotube Via Interconnects Fabricated by Novel Damascene Process", Proceedings of IEEE/ IITC 2007. Right, CNTs grown in pores in Silicon.

Nantero Inc. (Boston), Eikos Inc. Of Franklin, Massachusetts and Unidym Inc. (recently bought by Arrowhead) of Silicon Valley, California are also developing IP and transparent, electrically conductive films of carbon nanotubes [179]. CNT films are substantially more robust than ITO films mechanically, potentially making them ideal for use in displays for computers, cell phones, PDAs and ATMs as well as in other plastic electronic applications. At SID2008, University of Stuttgart and Applied Nanotech presented

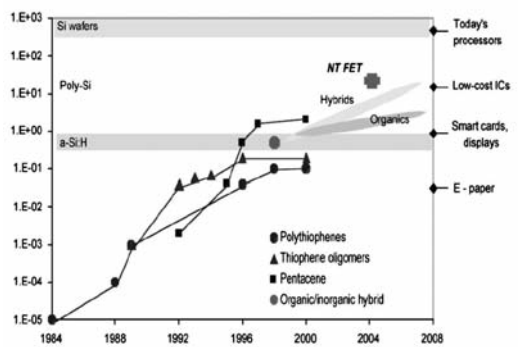

Figure 12. The evolution of the mobility of the plastic FET devices over the past decades. The mobility of CNTN FETs is indicated by the bold cross towards the top right-hand corner. Some application barriers are also indicated on the right side of the figure [182]. G Gruner. J. Mater. Chem., 2006, 16, 3533 – 3539 – Reproduced by permission of the Royal Society of Chemistry.

the world's first 4-inch QVGA colour LCD display using CNT as the transparent conductive film. The CNT were deposited by spray coating [180].

There is still a need to increase conductivity whilst maintaining a sufficiently high (~95%) transparency and for some applications, roughness is a problem. Also, most recently it has been pointed out by Fanchini et al. [181] that CNT/Polymer films are anisotropic and suffer from birefringent effects which may cause problems in some of its most useful potential application areas such as OLEDs, Displays and PV. Gruner summarizes the work in this area well (figure 12).

European Position: US dominates this area through the work of Eikos Inc, Nanomix Inc., Grüner and co-workers and Rinzler's group in Florida. Chhowalla at Rutgers has now carried on this work and Roth in Stuttgart leads the way in Europe.

8(d) Thermal management

There is also an increasing need to replace indium for thermal interfaces in eg: CPUs, graphic processors and (automotive) power transistors, as price and scarcity increase. Various companies and universities (such as Ajayan's group [183]) are working in this area but very little (if anything) has been published.
Current problems in using CNTs are insufficient packing density and problems with graphitisation leading to a reduction in conductivity.

European Position: Ajayan is the most notable contributor to this research. Very little work has been published by workers from the EU.

8(e) Transistors and diodes for logic

(i) Individual CNT-based transistors

Arguably this has been the electronic application on which most research has focused. As shown in table 2. Martel et al. and Tans et al. first reported a bottom gate individual single walled carbon nanotube field effect transistor (SWNT-FETs) with an on/off ratio of ~10^5 and a mobility of 20 cm^2/Vs in 1998 [184,185]. Afterwards, Durkop et al. claimed a mobility for bottom-gate SWNT-FET of >10^5 cm^2/Vs with a subthreshold swing ~100 mV/decade [186].

First author	Contact	Architecture	Mobility /cm²/Vs	On-Off ratio	Conductance S/m	Sub-threshold slope/mV/dec
Martel [184] Tans [185]	Au	Bottom gate (SiO_2/Si)	20	10^5	0,0017	——-
Durkop [186]	Cr/Au	Bottom gate (SiO_2/Si)	>10^5	——-	1,4	100
Wind [187]	Ti	Top gate (SiO_2/Al or Ti)	2300	10^6	3.25	130
Rosenblatt [188] Minot [189]	Au	NaCl and KCl solution top gate (Ag/AgCl probe)	1500	10^5	20	80
MH Yang [190] Javey [191]	Pd Mo	Top gate Al ZrO_2 top gate (Metal Ti/Au)	——- 3000	10^5 10^4	1000 6	67-70 70

Table 2

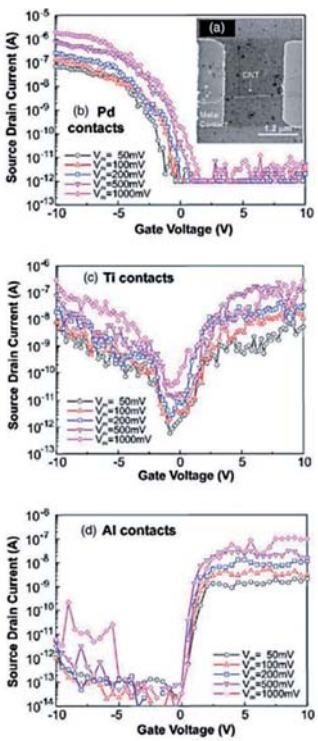

Figure 13. SWNT-FET transistor characteristics with different contacts. Top, Pd makes and ohmic contact which results in p-type conduction. Centre, Ti contacts result in strong ambipolar behaviour. Bottom, Al makes a Schottky contact which results in n-type conduction but with a strong leakage current.

This mobility is still the highest reported for bottom gate CNT-FETs thus far. Meanwhile, top gate SWNT-FETs were also attracting attention since such a structure can be readily used for logic circuits. In 2002, Wind et al. First demonstrated a top gate SWNT-FET with an on/off ratio of ~10^6, a transconductance of 2300 S/m and a subthreshold swing of 130 mV/decade [187]. Rosenblatt et al. And Minot et al. [188,189] using NaCl and KCl solutions as the top gate SWNT-FETs showed a mobility of 1500 cm^2/Vs, a subthreshold swing of ~80 mV/decade and an on/off ratio of 10^5. Yang et al. [190] showed a very high transconductance of 1000 S/m in a top gate device (shown in figure 13, together with a bottom gate device). Javey et al. Also demonstrated high performance SWNT-FETs using high-k dielectric ZrO_2 as the top gate insulator. Devices exhibited a mobility of 3,000 cm^2/Vs, a transconductance of 6000 S/m and a subthreshold swing of ~70 mV/decade respectively [191].

Several groups have also investigated vertical CNT-FETs (wrap-around gate). Choi et al. reported the first vertical MWNT-FET with a best conductance of 50 mS in 2003 [192] but this only works at low temperatures. Maschmann et al. demonstrate a vertical SWNT-FET in 2006 [193]. Their devices exhibited a good ohmic SWNTmetal contact, but the gate effect is not as efficient as either the top gate or bottom gate SWNT-FETs. SWNTFET always exhibit p-type operation when contacted ohmically, but n-type SWNT-FETs are also needed for fabrication of logic circuits. Derycke et al. claimed both annealing (removal of oxygen) and doping

(e.g. potassium) can convert a p-type SWNT-FET into a n-type and a logic inverter was demonstrated [194,195]. Javey et al. and Chen et al. reported that using different metal electrodes (e.g. Al) they could also obtain n-type SWNT-FETs with a ring oscillator also fabricated [196,197].

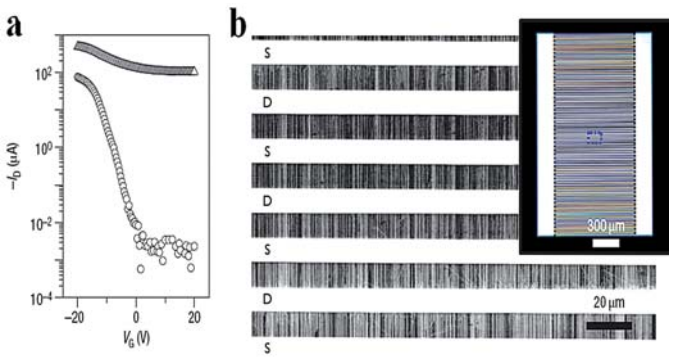

Figure 14. (a) Transfer curves from a transistor that uses aligned arrays of SWNTs transferred from a quartz growth substrate to a doped silicon substrate with a bilayer dielectric of epoxy (150 nm)/SiO_2 (100 nm). The data correspond to measurements on the device before (open triangles) and after (open circles) an electrical breakdown process that eliminates metallic transport pathways from source to drain. This process improves the on/off ratio by a factor of more than 10,000.

(b) Optical (inset) and SEM images of a transistor that uses interdigitated source and drain electrodes, in a bottom gate configuration with a gate dielectric of HfO_2 (10 nm) on a substrate and gate of Si. The width and length of the channel are 93 mm and 10 µm, respectively. The box indicated by the dashed blue lines in the optical image inset delineates the region shown in the SEM image [201]. Reprinted by permission from Macmillan Publishers Ltd: Nature (London), Seong Jun Kang, Coskun Kocabas, Taner Ozel, Moonsub Shim, Ninad Pimparkar, Muhammad A. Alam, Slava V. Rotkin, John A. Rogers, Nature (London), 2, 230 (2007), copyright 2007.

Challenges for the future include controlling the chirality, improving the yield of working devices, improving the reproducibility of the contact, ensuring all CNTs are semiconducting, improving the uniformity of the devices, controlling their positioning, and developing a process that can be scaled up to mass-production.

European Position: The state-of-the-art transistors (dependent on characteristics) are those produced by the groups of Avouris at IBM and in Europe, Bourgoin at CEA, Saclay, Ecole Polytechnique and Dekker at Delft University of Technology.

(ii) Network CNTs

In order to overcome the various problems with individual CNT transistors, numerous groups have concentrated on the production of transistors manufactured from CNT networks or even CNT/ Polymer mixtures. In 2002, the first report (a patent) for transistors based on random network of nanotubes and its use in chemical sensors was deposited by Nanomix Inc. [198], followed in 2003 by the disclosure of their integration onto a 100 mm Si wafer [199]. First public disclosure was made in 2003 by Snow et al. [200] who demonstrated a SWNT thin film transistor with a mobility of >10 cm^2/Vs and a subthreshold swing of 250 mV/decade with an on/off ratio of 10. In 2007, Kang et al. grew highly dense, perfectly aligned SWNT arrays on a quartz substrate which was then transferred to a flexible plastic substrate (PET). The SWNTFETs were fabricated on the PET substrate and exhibited a mobility of 1000 cm^2/Vs and a transconductance of 3000 S/m [201]. The Rogers group has exhibited state-ofthe-art network transistors for on-off ratio and mobility (see figure 14). Grenoble have also investigated this and have made a small chip of 75 such transistors.

The interest of the networks comes from the fact that if the average nanotube length is small compared to the distance between source and drain, more than one tube is needed to make the connection. Hence the probability of having an electrical path made only of metallic tubes is ~$(1/3)^n$ where n is tne number of tubes needed to make the junction. Secondly, the on/off ratio increases since, even if two tubes are metallic, their contact is not metallic [202].

Finally, even a single defect is enough to open a bandgap in a metallic tube, turning it into a semiconductor [203]. This means that controlling the number of defects is an important challenge to

overcome. Note that the first transparent CNT based transistor made on a flexible substrate was achieved by transferring a CNT random network and its contact from its initial silicon substrate onto a polyimine polymer [204].

European Position: Rogers in the USA produces the state of the art thin Film transistors and in Europe, apart from some preliminary work in Universities little seems to be happening.

9. Optical applications

9(a) Saturable absorbers

The band gap of semiconducting CNTs depends on their diameter and chirality, i.e. the twist angle along the tube axis [205]. Thus, by tuning the nanotube diameter it is easy to provide optical absorption over a broad spectral range [206]. Single-walled CNTs exhibit strong saturable absorption nonlinearities, i.e. they become transparent under sufficiently intense light and can be used for various photonic applications e.g in switches, routers and to regene-rate optical signals, or form ultra-short laser pulses [207-209]. It is possible to achieve strong saturable absorption with CNTs over a very broad spectral range (between 900 and 3000 nm [210]). CNTs also have subpicosecond relaxation times and are thus ideal for ultrafast photonics [211,212]. CNT saturable absorbers can be produced by cheap wet chemistry and can be easily integrated into polymer photonic systems.

This makes a CNT-based saturable absorber very attractive when compared to existing technology, which utilises multiple quantum wells (MQW) semiconductor saturable absorbers and requires costly and complicated molecular beam epitaxial growth of multiple quantum wells plus a post-growth ion implantation to reduce relaxation times [213]. Additionally, the MQW saturable absorbers can operate only between 800 and 2000 nm, a much narrower absorption bandwidth.

The major laser systems mode-locked by CNT saturable absorbers demonstrated so far (see figure 15) includes fibre lasers, waveguide lasers and solid-state lasers, generating sub-ps pulses in a broad spectral range between 1070 and 1600 nm [214]. The shortest pulse of about 68 fs was achieved with a solid state Er^{3+} glass laser by using a CNT-polyimide composite [215].

Additionally, amplified spontaneous emission noise suppression has been demonstrated with CNT-based saturable absorbers, showing great promise for this technology for multi-channel, all-optical signal regeneration in fibre telecom systems [216].
Challenges include justifying the research to industry due to the limited market potential.

European Position: There are 5 major research groups working on CNT saturable absorber applications around the world: Sakakibara at National Institute for Advanced Industrial science and Technology (AIST),

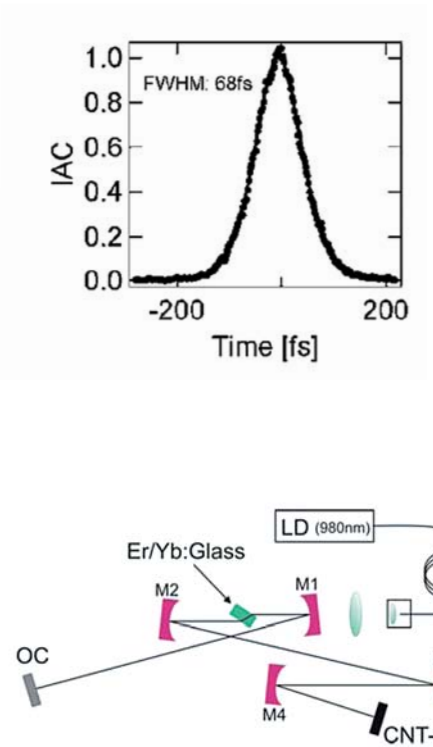

Figure 15. Top, Experimental setup of the Er/Yb:glass laser. OC: output coupler; M1-M4: standard Bragg-mirrors; CNT-SAM: Saturable absorber mirror based on carbon nanotubes; LD: pigtailed laser diode for pumping the Er/Yb:glass (QX/Er, Kigre Inc., 4.8 mm path-length). Bottom, background-free autocorrelation. The solid line is a sech2 fit with a corresponding FWHM pulse-duration of 68 fs [215].

Tsukuba, Japan, Maruyama and Yamashita at Tokyo University & Set in Alnair Labs, and Yoshida at Tohoku University and in Europe. Dr. E. Obraztsova in the Institute for General Physics, Moscow, and Cambridge University Engineering are the major players.

9(b) Microlenses in LCs

Microlenses in liquid crystal devices have potential applications in adaptive optical systems (where different focal lengths are required dependent on position), wavefront sensors (which measure the aberrations in an optical wavefront) and optical diffusers (which take a laser beam and redistribute it into any pattern desired). The use of sparse, MWCNT electrode arrays has been used to electrically switch liquid crystals.

The nanotubes act as individual electrode sites which produce an electric field profile, dictating the refractive index profile within the liquid crystal cell (see figure 16). The refractive index profile then acts to provide a series of graded index profiles which form a simple lens structure. By changing the electric field applied, it is possible to tune the properties of this graded index structure and hence form an electrically reconfigurable micro-optical array [217].

The problems for the lenslets come mostly from the alignment of the LC and the limited aperture of the lenslets. More generally, for the kinoform or modal hologram, the problem is to be able to individually address each CNT. Growing them onto a TFT or a VLSI circuit would be ideal (such as an LCOS backplane).

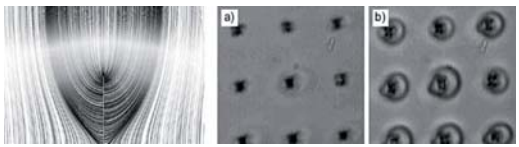

Figure 16. Left, Simulated electrical field profile surrounding the single carbon nanotube (10 μm high) with an applied field of 1V m^{-1}. Right, Defocus of the nanotube lenslet array at 40x. a) Defocused image of the array at 0 V μm^{-1} applied field. b) Array brought into focus with 2.1 V μm^{-1} applied field [217].

European Position: The Engineering Department in Cambridge as far as we know, are the only group in Europe working in this area.

9(c) Antennae

Ren at Boston College has demonstrated the use of a single multi-walled CNT to act as an optical antenna, whose response is fully consistent with conventional radio antenna theory [218]. The antenna has a cylindrically symmetric radiation pattern and is characterized by a multi-lobe pattern, which is most pronounced in the specular direction. Possible applications for optical antennae include optical switching, power conversion and light transmission. One particular application is the "rectenna", which is the light analogue of the crystal radio in which an antenna is attached to an ultrafast diode. This could lead to a new class of light demodulators for optoelectronic circuits, or to a new generation of highly efficient solar cells.

European Position: Early stages of research in the Dept of Engineering at Cambridge University in collaboration with Queen Mary College, London and ALPS (Electric), Japan.

9(d) Lighting

There is ongoing work on the use of CNTs for low energy lighting applications. The use of CNTs as electron emitters to stimulate phosphors has been reported by various groups and the replacement of metallic filaments with carbon CNTs/Fibres has been investigated by groups mostly in China. Carbon nanotube bulbs made from CNT strands and films have been fabricated and their luminescent properties, including the lighting efficiency, voltage-current relation and thermal stability have been investigated.

The results show that a CNT bulb has a comparable spectrum of visible light to a tungsten bulb and its average efficiency is 40% higher than that of a tungsten filament at the same temperature (1400-2300 K). The nanotube filaments show both resistance and thermal stability over a large temperature region. No obvious damage was found on a nanotube bulb held at 2300 K for more than 24 hours in vacuum, but the cost needs to be significantly reduced and the lifetime significantly increased for this to be considered seriously as an option.

European Position: Mostly in the Far East but Bonnard et al at EPFL have worked in this area.

10. Electromechanical and sensor applications

10(a) NEMS

Recently Amaratunaga et al [219] demonstrated novel non volatile and volatile memory devices based on vertically aligned MWCNTs (see figure 17).

Nanoelectromechanical switches with vertically aligned carbon nanotubes have been produced. However, Nantero are the market leaders in this area and have created multiple prototype devices, including an array of ten billion suspended nanotube junctions on a single silicon wafer [220]. Nantero's design for NRAM™ involves the use of suspended nanotube junctions as memory bits, with the "up" position representing bit zero and the "down" position representing bit one. Bits are switched between states through the application of electrical fields.

In theory the NRAM chip would replace two kinds of memory. While cell phones, for example, use both flash chips and SRAM or DRAM chips, NRAM would perform both functions. However the memory market is oversupplied and they frequently have to be sold at a loss, making it difficult for any new technology to break in. In addition, several other major companies are developing their own non-volatile memory technologies with PRAM perhaps the leading contender at present. PRAM, FRAM, MRAM and RRAM are all large companies.

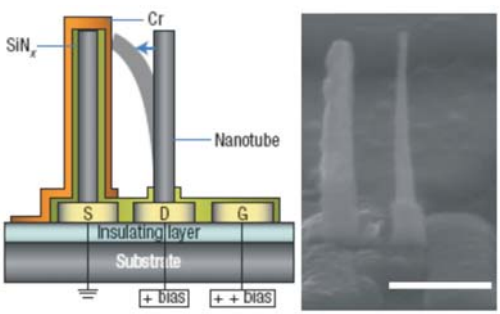

Figure 17. Left, a schematic diagram showing a cross-section of a switch fabricated by Jang et al.. Both contacts and catalyst were deposited with e-beam lithography. Right, an electron micrograph showing the grown CNTs acting as a switch [219]. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnolog , J.E. Jang, S.N. Cha, Y.J. Choi, D.J. Kang, T.P. Butler, D.G. Hasko, J.E. Jung, J.M. Kim and G.A.J. Amaratunga. "Nanoscale Memory Cell Based on a Nanoelectromechanical Switched Capacitor", Nature Nanotechnology 3, 26 - 30 (2008), copyright 2008.

With Nantero's relatively small size, market penetration is a big issue.

European Position: Nantero are the world leaders but in Europe ETH, TU Denmark, Cambridge Univ. Engineering in collaboration with Samsung and Thales plus numerous other groups are making significant contributions.

10(b) Sensors

CNTs for sensing is one of their most interesting electronic applications. Both SWCNTs and MWCNTs, functionalised and unfunctionalised, have been investigated. They have been used as gas, chemical and biological sensors and Nanomix Inc was the first to put on the market an electronic device that integrated carbon nanotubes on a silicon platform (in May 2005 they produced a hydrogen sensor) [221]. Since then, Nanomix has taken out various other sensing patents e.g. for carbon dioxide, nitrous oxide, glucose, DNA detection etc [222]. The next product to become available should be a breath analyzer detecting NO as a marker of asthma. More recently workers in Cambridge and Warwick University in collaboration with ETRI, South Korea have integrated CNTs onto SOI substrates to produce smart gas sensors (see figure 18) [223]. The CNTs have been locally grown on microheaters allowing back end deposition at T ~700 ºC.

Numerous other groups worldwide continue to investigate CNTs for sensing because of their ease of functionality and high surface area. Dekker and his group are focusing on biosensors and electrochemical sensors using carbon nanotubes.There are very many problems to overcome in bringing this technology to the market. Reproducibility of the CNT growth, processing as well as variable behaviour once integrated in a sensor can result in poor selectivity and sensitivity. In some devices, defects play a key role, in others, the source/drain metal-nanotube contact is key.

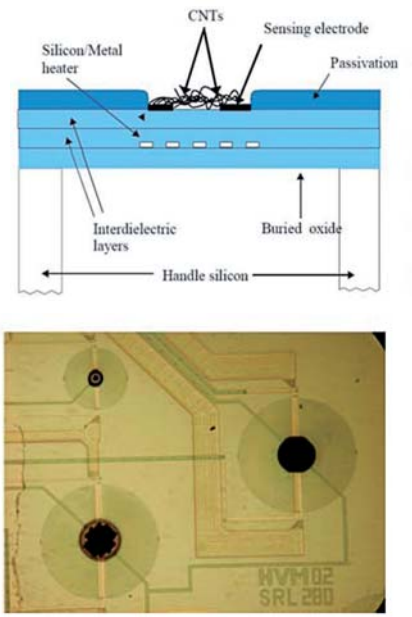

Figure 18. Top, structural cross-sectional layout of the sensing area of the chip. Bottom, microscopic images of carbon nanotubes grown locally on ultrathin membranes incorporating a tungsten heater [223]. Reprinted by permission from IOP Publishing Ltd. M.S. Haque, K.B.K. Teo, N.L. Rupesinghe, S.Z. Ali, I. Haneef, S. Maeng, J. Park, F. Udrea, and W.I. Milne. "On-chip Deposition of Carbon Nanotubes using CMOS Microhotplates", Nanotechnology 19, 025607 (2007). Author and Publisher are acknowledged.

Also, both the nanotube-nanotube junction or even amorphous carbon remaining on the nanotube can play a significant role in the detection scheme [224]. Indeed, there are many possible sensing mechanisms, hence a fundamental understanding of them is required to enable good optimisation and reproducibility of the sensors.

Although Nanomix has already raised $34 millions they have yet to deliver a significant, high volume product to the market. However, progress in these areas continues to be made globally.

European Groups Many companies and research institutions are carrying out work in this area, with THALES, Dekker (Delft), being the most successful.

10(c) CNT's in biotechnology and medical devices research

Definition: Nanomedicine, for the purpose of this section is defined as the application of nanotechnology to achieve breakthroughs in healthcare. It exploits the improved and often novel physical, chemical and biological properties of materials at the nanometer scale. Nanomedicine has the potential to enable early detection and prevention, and to essentially improve diagnosis treatment and follow-up of diseases. This document addresses the overall roadmaps associated with nanomedicine and in particular identifies the role of CNT's. The key issues associated with CNT's related to nanomedicine is mainly related to the following issues:

- Some of the main challenges are linked to industrialisation. There is no conventional manufacturing method that creates low cost CNTs. Desirable properties are robustness, reproducibility, uniformity and purity.
- Reproducible production relating to surface defects; surface chemistry, size (hight and diameter; morphology; type etc.
- The ability to functionalise the surface with appropriate chemistries.
- The ability to produce arrays; periodicity; catalyst freeor tailored catalyst grown from self-assembly.
- To produce lost cost routes to manufacture in the case of disposable or competitive devices.
- The ability to integrate into microfluidic systems; CMOS circuitry or flexible substrate systems.

A clear set of studies are required to resolve all the issue of biocompatibility and nanotoxicity associated with the use, manufacture and purchase of CNT's of all forms.
In the next ten years, the development of biosensors and importantly, nanotechnology, will allow the design and fabrication of miniaturised clinical laboratory analysers to a degree were it is possible to analyse several laboratory measurements at the bedside with as little as 3μL of whole blood. The use of quantum dots; self-assembly; multifunctional nanoparticles, nano-templates and nano-scale fabrication including nanoimprinting will have a major impact on the design

and development of much improved highly sensitive and rapid diagnostics; thus allowing accurate drug delivery integration. Nanoenabled high throughput analysis will also reduce the time it takes to bring a new drug delivery platform to market.

Nanomix is attempting to put such a device on the market in the next 12-18 months, with its NO sensor which is applied to monitoring asthma.

10(d) Nanofluidics

The interest in taking advantage of the unique properties of carbon nanotubes in nanofluidic devices has increased tremendously in the last couple of years. The carbon nanotubes can either be used directly as a nanofluidic channel in order to achieve extremely small and smooth pores with enhanced flow properties [225] or be embedded into existing fluidic channels to take advantage of their hydrophobic sorbent properties and high surface-to-volume ratio for improving chemical separation systems [226,227].By integrating vertically aligned carbon nanotubes into silicon nitride [228] and polymer membranes [229,230] respectively, it has been possible to study the flow of liquids and gases through the core of carbon nanotubes.

The flow rates were enhanced with several orders of magnitude, compared to what would be expected from continuum hydrodynamic theory [225]. The reason for this is believed to be due to the hydrophobic nature of the inner carbon nanotube sidewall, together with the high smoothness, which results in a weak interaction with the water molecules, thereby enabling nearly frictionless flow through the core of the tubes. This effect is resemble transport through transmembrane protein pores, such as aquaporins, where water molecules line up in a single file with very little interaction with the sidewall.

This application of carbon nanotubes is envisioned to result in novel ultrafiltration and size-based exclusion separation devices, since the pores size is approaching the size of ion channels in cells [225]. The carbon nanotube membranes are, however, fabricated by CVD and this application is therefore suffering from the lack of large scale cost-effective CNT depositing equipment. In the last couple of years CNTs have also been investigated as a sorbent material for improving both the resolution and sensitivity of chemical separations [226,227].

This has been done by incorporating the nanotubes in the stationary phase of mainly gas chromatography columns to take advantage of their high surface-to-volume ratio and better thermal and mechanical stability compared to organic phases, which make them ideal for especially temperature programmed separations [226,227,231]. The carbon nanotubes, in the form of powder, is hard to pack directly in the columns due to its marked tendency for aggregation and hence channel blockage [226,227,232] so the CNTs have typically either been incorporated in a monolithic column [233] immobilized on the inner channel wall [234] (or deposited on the surface of beads that subsequently were packed) [235]. A major complication of these methods, beside that they are manual and very labor intensive, is that they rely on the necessity of forming uniform CNT suspensions, which is difficult, since CNTs are insoluble in aqueous solutions and most organic solvents [226]. It is therefore typically required to either dynamically or covalently modify the CNTs to avoid aggregation [227].

These problems can be overcome by direct growth of the CNTs on a surface, in e.g. microfluidic channels [236,237,238] so they are anchored to the channel wall and therefore unable to from aggregates. This also allows a much higher CNT concentration without clogging the fluidic devices. Growing of CNTs in microfluidic systems has the additional benefit that lithography can be used for the pattern definition, which should make it possible to make much more uniform and therefore more efficient columns [239].A major limitation of this application is also the lack of low cost CNT deposition equipment, since it is necessary to use vertically aligned CNTs that are attached to the surface to avoid aggregation and to benefit from the high uniformity of the nanostructures.

European Position: Montena Components of Switzerland are in competition with Maxwell Technologies in this area.

II. Energy applications

II(a) Fuel cells

Carbon nanotubes can be used to replace the porous carbon in electrode-bipolar plates in proton exchange membrane fuel cells, which are usually made of metal or graphite/carbon black. The CNTs increase the conductivity and surface area of the electrodes which means that the amount of platinum catalyst required can

be reduced [240]. The state of the art in this area is the mixing of CNTs and platinum catalyst particles reported by F. Chen et al. of Taiwan.

Whilst CNTs reduce the amount of platinum required, it is only a small percentage, which means that the cost of the fuel cell remains high. Also, CNTs are comparable in price to gold, meaning the saving is minimal.

European Position: The leaders in this area are the Taiwanese groups. The European leaders are linked to S Roth (Max Planck Institute, Stuttgart).

II(b) Supercapacitors

Electric double-layer capacitors, or supercapacitors have energy densities 1000 times greater than typical electrolytic capacitors. This occurs because they use the high surface area of porous carbon or nanotubes, and the narrow thickness of the electrochemical double layer as the capacitor separation. Supercapacitors allow inverters in electric trains to transform between voltages. They allow electric vehicles to have greater acceleration than from simple batteries. They would allow smoothing of power supplies on mobile phones.

Experimental devices replace the activated charcoal required to store the charge with carbon nanotubes, which have a similar charge storage capability to charcoal (which is almost pure carbon) but are mechanically arranged in a much more regular pattern that exposes a much greater suitable surface area. The figures of merit are energy density, related to the capacitance per unit volume of the carbon, and thereby the surface area of the porous carbon, and secondly the power density, related to the series resistance.

Activated carbon is close to the theoretical surface area of carbon layers already, so going to nanotubes does not gain so much. But nanotubes have lower electrical resistance than porous carbon, so there is a gain in power density. In order to gain in energy density, development is towards hybrid CNT-polymer supercapacitors, using polypyrrole etc. Ionic displacement within the Ppy acts as a pseudo capacitance/battery. The weakness of supercapacitors in electric vehicle applications is that they must be priced against conventional batteries which are very low in price.

European Position: Leader in Europe is Beguin et al. [241] who have used multi-walled CNTs mixed with polymers to create capacitance values of 100-330 F/g. Europe also has a strong industrial; input in this area with companies such as Maxwell (formerly Montena, Switzerland).

II(c) Batteries

The outstanding mechanical properties and the high surface-to-volume ratio make carbon nanotubes potentially useful as anode materials [242] or as additives [243] in lithium-ion battery systems. The CNTs give mechanical enhancement to the electrodes, holding the graphite matrix together. They also increase the conductivity and durability of the battery, as well as increasing the area that can react with the electrolyte. Sony produce the best CNT enhanced lithium-ion batteries. The main problem is the high cost of CNTs. Recently, a so-called paper battery has been developed, where CNTs are used as electrodes which are attached to cellulose immersed in an electrolyte. The technology is cheap, the batteries are flexible and no harmful chemicals are required [244]. The main problem with this is the high production cost of the battery, which needs to be reduced for mass production. The ambition is to print the batteries using a roll-to-roll system.

European Position: Although much of the innovation in this are has been carried out in the US and the Far East, in Europe there are various groups notably in Germany contributing in this area.

II(d) Solar cells

There has been much research into incorporating carbon nanotubes into solar cells. One application is the dispersion of CNTs in the photoactive layer. Amaratunga [245] has observed enhancement of the photocurrent by two orders of magnitude with a 1.0% by weight single-walled CNT dispersion. However, the power efficiency of the devices remains low at 0.04% suggesting incomplete exciton dissociation at low CNT concentrations. At higher concentrations, the CNTs short-circuit the device. More recently, a polymer photovoltaic device from C60-modified SWCNTs and P3HT has been fabricated [246]. P3HT, a conjugated polymer was added resulting in a power conversion efficiency of 0.57% under simulated solar irradiation (95

mW cm^{-2}). An improved short circuit current density was attributed to the addition of SWCNTs to the composite causing faster electron transport via the network of SWCNTs.

Further optimization is required to improve the efficiency still further. Furthermore, photoconversion efficiencies of 1.5% and 1.3% have been achieved with SWCNTs deposited in combination with light harvesting CdS quantum dots and porphyrins, respectively [247].

CNTs have also been developed as a replacement for transparent conductive coatings to replace ITO which is becoming more expensive as supply runs out. Studies have demonstrated SWCNT thin films can be used as conducting, transparent electrodes for hole collection inOPV devices with efficiencies between 1% and 2.5% confirming that they are comparable to devices fabricated using ITO [248,249].

Finally, CNTs have been investigated for application in dye-sensitized solar cells (DSSC). CNT networks can act as a support to anchor light harvesting semiconductor particles. Research efforts along these lines include organizing CdS quantum dots on SWCNTs. Other varieties of semiconductor particles including CdSe and CdTe can induce charge-transfer processes under visible light irradiation when attached to CNTs [250]. The SWNTs facilitate electron transport and increase the photoconversion efficiency of DSSCs. Other researchers fabricated DSSCs using the sol-gel method to obtain titanium dioxide coated MWCNTs for use as electrodes [251].

European Position: Although much of the work in this area has been driven by the USA and Japan significant input on both the incorporation of the CNTs as part of the active layer and in transparent contact materials has been made in universities across the European community.

I1(e) Hydrogen storage

CNTs have been suggested as potential candidates for hydrogen storage. However, the reported hydrogen uptake varies significantly from group to group, with the mechanism not clearly understood. Current methods involve compressing the CNTs into pellets which are then subjected to hydrogen at high pressure.

The target set by the US Department of Energy is 6% by weight hydrogen by 2010. Whilst most groups have found hydrogen uptake to be in the 1-2% region [252], amongst the highest reported are Gundish et al. [253] at 3.7% and Dai's group [254] at 5.1%. It should be noted that Hirschler and Roth found most values to be false [255], for example due to Ti take up during sonication.

From a more fundamental point of view, since the average adsorption energy of hydrogen on CNTs is not significantly different from its value on amorphous carbon. It is mainly the surface area which plays a crucial role. Hence 5.8% was achieved a long time ago on super-high surface area activated carbon [256].

European Position: Over the last 10 or so years there have been numerous groups worldwide working in this area; especially in the USA, Japan and China. Europe too has made a significant investment, notably through groups in Germany, France, Greece (theoretical work) and the UK but still the DoE 6% target remains elusive.

I2. Future/Blue Sky

I2(a) Spintronics

Spin transport has been demonstrated over lengths of hundreds of nanometers in CNTs [257], and the limit may be much longer. The Kondo effect has been demonstrated [258], and Fano resonances have been found [259]. Spin blockade has been demonstrated in a double dot structure [260].

Problems to overcome include the production of uniform, defect-free SWNTs, free from paramagnetic impurities, and with a single chiral index and fabrication of reproducible devices with uniform contacts.

European Position: Hitachi, Cambridge Laboratory, the Cavendish Lab Charles Smith, in collaboration with Andrew Briggs at Oxford are the leaders in the field; Others include Delft (Leo Kouwenhoven) and the Niels Bohr Institute, Copenhagen.

I2(b) Quantum computing

Arrays of qubits have been created in the form of endohedral fullerenes in SWNTs, to make so-called peapod [261]. The interactions between the spins have

been characterized by electron paramagnetic resonance, showing transitions from exchange narrowing to spin-spin dephasing.

Theoretical architectures have been developed for global control of qubits [262]. The spin properties of N@C60 have been shown to make it one of the strongest candidates for condensed matter quantum computing [263].

Quantum memories have been demonstrated, in which information in the electron spin is transferred to the nuclear spin, and subsequently retrieved. In this system the gate operation times is of order 10 ns, and the storage time is in excess of 50 ms, which clearly needs to be improved. Problems to overcome include the development of the technology for single spin read out in CNTs and the demonstration of entanglement using peapods.

European Position: Oxford leads the world in peapods for quantum computing, in collaboration with Princeton (Steve Lyon), Nottingham (Andrei Khlobystov), Cambridge (Charles Smith), EPFL (Laszlo Forro), There is also activity in Berlin (Wolfgang Harneit), at L. Néel Institute in Grenoble and at CEMES-CNRS in Toulouse [264].

I2(c) Ballistic transport

Owing to their perfect geometry, carbon nanotubes are expected to exhibit ballistic transport for most radii encountered in experimentation [265]. However, backscattering due to electron-phonon interactions has been demonstrated in single-wall carbon nanotubes at biases of several volts [266]. This scattering is nonetheless only manifested in relatively low-energy electrons in devices of lengths of several hundred nanometers [267].

The mean free path for acoustic phonon scattering in CNTs is long (~ 1 micron) and hence its impact on the drain current for a 50 nm channel length is negligible [268,269]. The mean free path for optical scattering is about 10 nm and the energy of emission is ~ 0.16 eV [270]. The injected hole can be backscattered near the drain, but the likelihood of it scattering back to the source is small on account of the higher Schottky barriers encountered at the drain [6].

Monte Carlo simulations including electron-phonon interactions yield mobility values similar to those under ballistic transport (~ 10^4 cm^2/Vs) in semiconducting tubes of radii up to ~ 2 nm [271]. It is worth noting though that onset of ambipolar conduction in CNTFETs has been found to be modified by phonon scattering [272]. Monte Carlo simulations have also revealed steady-state velocity saturation due to optical phonon scattering and negative differential mobility at high electric fields [273].

Regarding other scattering mechanisms, by using a k.p approximation, Ando and co-workers provided an elegant proof of the suppression of back scattering for impurities with smooth potential range, much larger than the lattice constant [274]. However the nature of disorder in nanotube-based materials and devices is more complex, including topological defects, chemical impurities, vacancies, etc..

The impact of such defects can strongly jeopardize initial good ballistic capability of otherwise clean nanotubes, and its study is therefore genuinely relevant. Several advanced computational scheme based on first principles (see reference [273]) allow a realistic description of scattering potentials, with quantitative estimation of associated elastic mean free paths and charge mobilities.

Additionally, even though transport in CNTs can be considered largely ballistic, CNTFETs have been demonstrated to be Schottky barrier FETs [275]. Even undoped CNTFETs, with zero-Schottky-barrier contacts are limited by voltage-controlled tunnelling barriers, presented by the body of the CNT, at the source and drain [276]. As a result, the current is strongly controlled by the CNT diameter, chirality, contact geometry/type/thickness and oxide thickness, all of which modulate the barriers and present problems such as ambipolar conduction.

Both inter and intraband tunnelling needs to be taken into account when modelling the transport. Furthermore, a correct treatment requires taking into account quantum confinement around the tube circumferential direction, quantum tunnelling through Schottky barriers at the metal/nanotube contacts, quantum tunnelling and reflection at barriers in the nanotube channel. Limitations in predicting CNTFET

transport arise both from theory and experiment. To date there has not been any demonstration of the relationship of the electrical property of a CNTFET to its physical structure. Notwithstanding limitations of experimental techniques, limitations of theory include many-body effects in the atomistic modelling of the CNT and the dependence of transport modelling on "fitting" parameters.

The main remaining challenges is to better understand high-bias transport regimes because of their relevance in device performances (high flow of current densities), as well as the possible control of Schottky-Barrier features by a proper choice of metal contacts/nanotubes characteristics/ environment exposure/chemical functionalization, and so forth. Furthermore, the performances of nanotubebased vias also need to be increased by optimised control of tube growth processes. In that respect, sophisticated computational modelling tools and expertise are clearly essential factors to allow the indepth exploration of transport properties and device performance optimization.

European Position: In Europe, several groups have brought key contributions [277] to the fields of modelling carbon nanotubes physical (and transport) properties, mainly in Belgium (Jean-Christophe Charlier at University of Louvain), France with Xavier Blase (Institut Néel, Grenoble) and Stephan Roche (CEA Grenoble, France), and Spain with Angel Rubio (University of San Sebastian).

These scientists are leading the international community in several fields from ab-initio computation of growth processes, electronic and vibrational properties, to the simulation of quantum transport in nanotubes-based materials and devices. Several other European groups are also contributing to the field of device simulation such as Giuseppe Iannaconne in Pisa (Italy), Kosina/Selberherr at TU Vienna, Giovanni Cuniberti at TU-Dresden in Germany, to cite a few. This community expert in theory and simulation is extremely important to sustain experimental efforts and device optimisation.

I2(d) Single electron transistors

A single electron transistor (SET) is a device in which a quantum dot (QD) is connected with source and drain contacts through small tunnel junctions. A QD is a small metallic island in which electrons are confined. Therefore, it is sometimes compared with a natural atom, where electrons are confined in the Coulomb potential on a much smaller scale. When the discrete levels and the shell structure are clearly formed, the quantum dot is called an artificial atom. In the SWCNT QD, electrons are confined in the axial direction as well as the circumference direction.

Single electron transistor (SET) operation in single-walled carbon nanotubes (SWNTs) to estimate the length of ballistic conduction in laser-synthesized SWNTs has been investigated. The devices were fabricated by an alternating current-aligned method and the SWNTs were sidecontacted to the electrodes.

At 5 K, Coulomb oscillation and Coulomb diamonds were observed and the Coulomb island length, i.e., the ballistic conduction length, was calculated to be about 200-300 nm. Whilst many groups have published work in this area, as far as it can be ascertained, this is the only report of a true SET action in CNTs [278].

European Position: Major efforts have been made in Japan including work in various companies such as Toshiba, Hitachi, NEC and NTT. The work in Europe tends to be at the more fundamental/University level.

I3. Conclusions

CNTs have many unique and indeed useful properties for applications in the ICT area. Research into CNTs will continue for at least the next several years especially into quantum effects and associated behaviour, as well-characterized, high-quality SWCNTs become more available.Although CNTs are still being touted for various industrial applications, much more investment is necessary for them to reach commercial viability. The USA and Japan lead in this development but Europe has made significant impact in many areas despite the fact that investment in Europe is but a fraction of that in the other major high-tech industrial zones.

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3.2 Status of modelling for nanoscale information processing and storage devices*

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During the 2009 meeting of the Theory and Modelling working group the current status of modelling for nanoscale information processing and storage devices has been discussed and the main issues on which collaboration within the modelling community is needed have been pointed out. An analysis of the current situation in Europe in comparison with that in the rest of the world has been performed, too. The previous version of the present report (resulting from the 2008 meeting) has been updated reflecting the new issues that have been recognized as relevant and of significant current interest.

Introduction

We are presently witnessing the final phase of the downscaling of MOS technology and, at the same time, the rise of a multiplicity of novel device concepts based on properties of matter at the nanoscale and even at the molecular scale.

Ultra-scaled MOS devices and nanodevices relying on new physical principles share the reduced dimensionality and, as a result, many of the modelling challenges. In addition, new materials and process steps are being included into MOS technology at each new node, to be able to achieve the objectives of the Roadmap; these changes make traditional simulation approaches inadequate for reliable predictions. So far modelling at the nanoscale has been mainly aimed at supporting research and at explaining the origin of observed phenomena.

In order to meet the needs of the MOS industry and to make practical exploitation of new device and solid-state or molecular material concepts possible, a new integrated approach to modelling at the nanoscale is needed, as we will detail in the following. A hierarchy of multi-scale tools must be set up, in analogy with what already exists for microelectronics, although with a more complex structure resulting from the more intricate physical nature of the devices.

A coordinated effort in the field of modelling is apparent in the United States, where significant funding has been awarded to the Network for Computational Nanotechnology, which is coordinating efforts for the development of simulation tools for nanotechnology of interest both for the academia and for the industry.

Although the required integrated platforms need to be developed, the efforts made in the last few years by the modelling community have yielded significant advances in terms of quantitatively reliable simulation and of ab-initio capability, which represent a solid basis on which a true multi-scale, multi-physics hierarchy can be built. The combination of these new advanced software tools and the availability of an unprecedented and easily accessible computational power (in particular considering the recent advances in terms of GPU-based general purpose computing) make the time ripe for a real leap forward in the scope and performance of computational approaches for nanotechnology and nanosciences.

Current status of MOS simulation and industrial needs

The continuous downscaling of MOSFET critical dimensions, such as the gate length and the gate oxide thickness, has been a very successful process in current manufacturing, as testified, e.g., by the ITRS requirements. However, conventional scaling down of MOSFET channel length is declining as the physical and economic limits of such an approach are coming closer. Novel solutions are increasingly being used in MOSFET channel engineering within the industry.

Among the new technological features of very advanced devices, high-k dielectrics, the archetype of which is hafnium oxide, can significantly reduce gate leakage. Mechanical strain applied in the channel and substrate

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orientation can also significantly improve carrier mobility. Moreover, alternative geometries, such as double-gated devices, in which the channel doping level is relatively low, must be evaluated within the perspective of an industrial integration. In particular, the subsequent effects of the high-k gate dielectric and of the double-gate geometry on channel mobility must be clearly quantified.

Technology Computer-Aided Design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor devices. State-of-the-art commercial TCAD device simulators are currently working using the Drift-Diffusion (DD) approximation of the Boltzmann transport equation. Quantum effects are accounted for using the Density Gradient approximation, that works well for traditional bulk devices, but that can be unreliable for advanced devices such as the double-gated-MOS structure or for new materials. Moreover, emerging materials also significantly challenge the conventional DD-based tools, mostly due to a lack of appropriate models and parameters. It becomes urgent to develop new physically-based models with a view of integrating them into a standardized simulation platform that can be efficiently used in an industrial environment. For this purpose, tight collaborations between world-class universities and research institutions, CAD vendors and industrial partners must be established.

Within the framework of these collaborations, there will be the best chances of success, both in terms of academic model development and theoretical achievements, but also in terms of concrete implementations and benchmarks of new models in TCAD tools. Innovative concepts based on nano-materials or molecular devices, new models and simulation tools would provide our ICT industries a competitive advantage for device development and optimization in terms of time-cycle and wafer-costs.

Commercial v.s. academic quantum-transport solvers

In response to the industrial need of new simulation tools, a class of quantum and transport solvers is emerging. These commercial state-of-the-art solvers can be divided into two categories. In the first category, one can find the quantum-transport solvers, such as those based on the Non-Equilibrium Green Function Method, in which carrier transport is treated using the full quantum Green function formalism. In the second category one can include the Monte Carlo Solvers, that model carrier transport via the Boltzmann equation. This equation is solved in a stochastic way, using a classical description of the free fly of the electrons but a quantum description of the interactions. The currently available high-level NEGF [1] and MC solutions [2] are still in the development phase, and no ready-to-use industrial solutions are available so far to meet the requirements of the 32 nm node and beyond.

From the point of view of technology development support, the Monte Carlo simulators should be able to provide reliable electrical results on a regular basis for 32 nm MOS devices. However the need for full-band Monte-Carlo codes together with band structure solvers that account for strain and are capable of dealing with new materials must be highlighted. Indeed, some commercial 3D Schroedinger solvers [1] combined with NEGF solvers start being available. These solvers can be used to model ballistic quantum transport in advanced devices with strong transverse confinement. However, they do not include any inelastic scattering mechanism, and thus are not suitable for the calculation of transport properties in the 32 nm node devices and near-future nodes.

On the other hand, high-level device simulation tools are at an early stage of development in universities and research institutions. These codes generally include advanced physical models, such as strain-dependent band structure and scattering mechanisms, and should provide accurate predictions in complex nano-systems. However, such simulation tools are in general difficult to use in an industrial environment, in particular because of a lack of documentation, support and graphical user interface, although an increasing number of academic codes are now including graphic tools [3,4]. Taking advantage of these ongoing research projects, it should be possible to integrate such high-level codes into industrial TCAD tools or to use them to obtain calibrated TCAD models useful for the industry. Concerning this latter point, the quantum drift-diffusion-based solution must be “customized”, in order to make fast and accurate simulations of advanced devices possible. For instance, the effect of the high-k gate dielectric stack on device performance must be addressed with a particular attention to its impact on carrier transport properties. This is definitely one of the most challenging issues in semiconductor industry at present.

Efficient modelling tools, as well as accurate physics highlights, would certainly bring a significant competitive advantage for the development and the optimization of the 32 nm CMOS technology and for future technologies, including molecular devices.

Importance of modelling variability

Near the end of the current edition of the International Technology Roadmap for Semiconductors (ITRS) in 2018, transistors will reach sub-10 nm dimensions [5]. In order to maintain a good control of the electrical characteristics, new transistor architectures have to be developed. It is widely recognized that quantum effects and intrinsic fluctuations introduced by the discreteness of electronic charge and atoms will be major factors affecting the scaling and integration of such devices as they approach few-nanometer dimensions [6-11].

For instance, in conventional one-gate nanotransistors, variations in the number and position of dopant atoms in the active and source/drain regions make each nanotransistor microscopically different from its neighbours [12-16]. In nanowire MOS transistors the trapping of one single electron in the channel region can change the current by over 90% [17,18]. Interface roughness of the order of 1-2 atomic layers introduces variations in gate tunnelling, quantum confinement and surface/bulk mobility from device to device. The inclusion of new materials such as SiGe will induce additional sources of fluctuations associated with random variations in the structure, defects, strain and inelastic scattering [19,20]. These intrinsic fluctuations will have an important impact on the functionality and reliability of the corresponding circuits at a time when fluctuation margins are shrinking due to continuous reductions in supply voltage and increased transistor count per chip [7,8].

The problem of fluctuations and disorder is actually more general and affects fundamental aspects of information storage and processing as device size is scaled down. The presence of disorder limits the capability of patterning by introducing a spatial variance: when the pattern size approaches the spatial variance, patterns are unavoidably lost. An analogous problem exists as a result of time fluctuations (shot noise) associated with the granularity of charge: as current levels are reduced, the signal power decreases faster (quadratically with current) than the shot noise power (linear with current), leading to a progressive degradation of the signal-to-noise power ratio.

Disorder has demonstrated all of its disruptive power on nanodevices in the case of single-electron transistors: as a result of their extreme charge sensitivity, stray charges, randomly located in the substrate, are sufficient to completely disrupt their operation.

Fluctuations associated with the granularity of charge and spatial disorder are fundamental roadblocks that affect any effort towards handling information on an increasingly small scale.

It is thus of strategic importance to develop device simulation tools that are capable of efficiently exploring the extremely large parameter space induced by such variability and evaluate the actual performance limits of new nanodevices. Strategies to decrease the amount of naturally occurring disorder or to cope with it need to be devised as emerging devices are developed into new technologies aiming at the limits of the downscaling process.

Integration between material and device simulation

Both for decananometric MOSFETs and for most emerging devices, the distinction between material and device simulation is getting increasingly blurred, because at low dimensional scales the properties of the material sharply diverge from those of the bulk or of a thin film and become strongly dependent on the detailed device geometry. Such a convergence should start being reflected also in research funding, because, at the dimensional scale on which research is currently focused, a project cannot possibly take into consideration only one of these two aspects. This was not the case until a few years ago, when a material could be investigated within the field of chemistry or material science and then parameters were passed on to those active in the field of device physics and design, who would include them in their simulation tools.

Fortunately, the nanoelectronics simulation community is not starting from scratch in terms of atomic scale materials computations. Computational physics and quantum chemistry researchers have been developing sophisticated programs, some with on the order of mil-

lions of lines of source code, to explicitly calculate the quantum mechanics of solids and molecules from first principles. Since quantum mechanics determines the charge distributions within materials, all electrical, optical, thermal and mechanical properties, in fact any physical or chemical property can in principle be deduced from these calculations.

However, these programs have not been written with nanoelectronics TCAD needs in mind, and substantial theoretical and computational problems remain before their application in process and device modeling reaches maturity. However, the coupling of electronic structure theory programs to information technology simulations is occurring now, and there is nothing to suggest this trend will not continue unabated. Quantum electronic structure codes come in essentially two flavours: those using plane wave expansions (or real-space grids) and those using basis sets of atomic orbitals to span the electronic wave functions. Plane wave codes are suitable for solid state calculations and have been mainly developed within the Solid State Physics community. Codes using atomic orbitals were initially developed within the Quantum Chemistry community, although recently have also become popular within the Materials Physics community. Quantum Chemistry codes rely heavily on the expansion of the atomic orbitals in terms of Gaussian functions. This is mainly due to the fact that, with the use of Gaussians, the four-center-integrals associated with Coulomb and exchange interactions become analytic and easy to calculate. H wever, within the framework of Density Functional Theory, due to non-linear dependence of the exchange - correlation energy and potential with the density, the evaluation of such contributions to the energy and Hamiltonian has to be necessarily performed numerically and the advantage of using Gaussian functions is mainly lost. This has opened the route for the use of other types of localized basis sets optimized to increase the efficiency of the calculations. For example, localized basis orbital can be defined to minimize the range of the interactions and, therefore, to increase the efficiency of the calculation, the storage, and the solution of the electronic Hamiltonian [21].

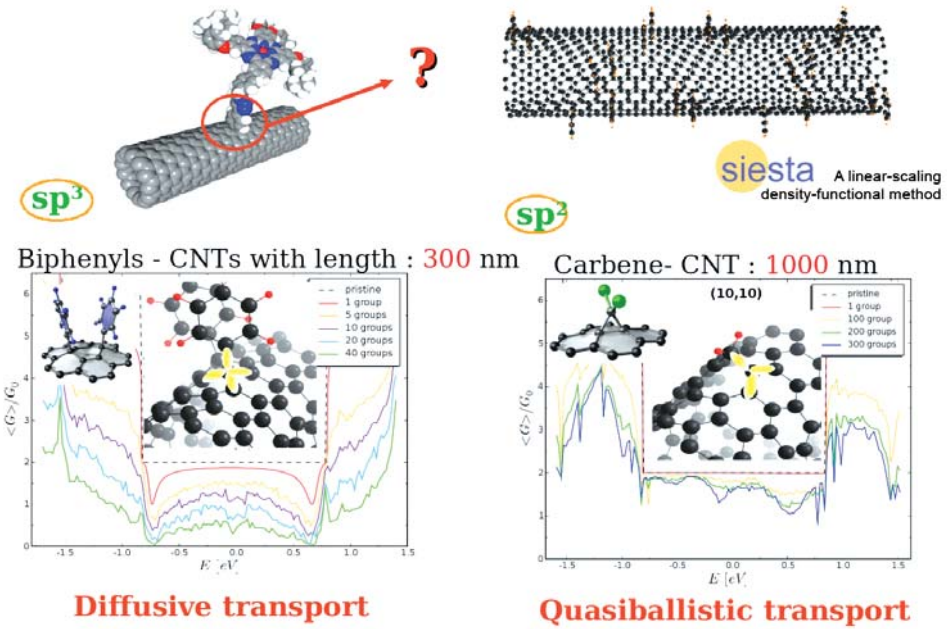

Figure 1. Codes such as SIESTA can be used for the ab-initio simulation of relatively large structures.

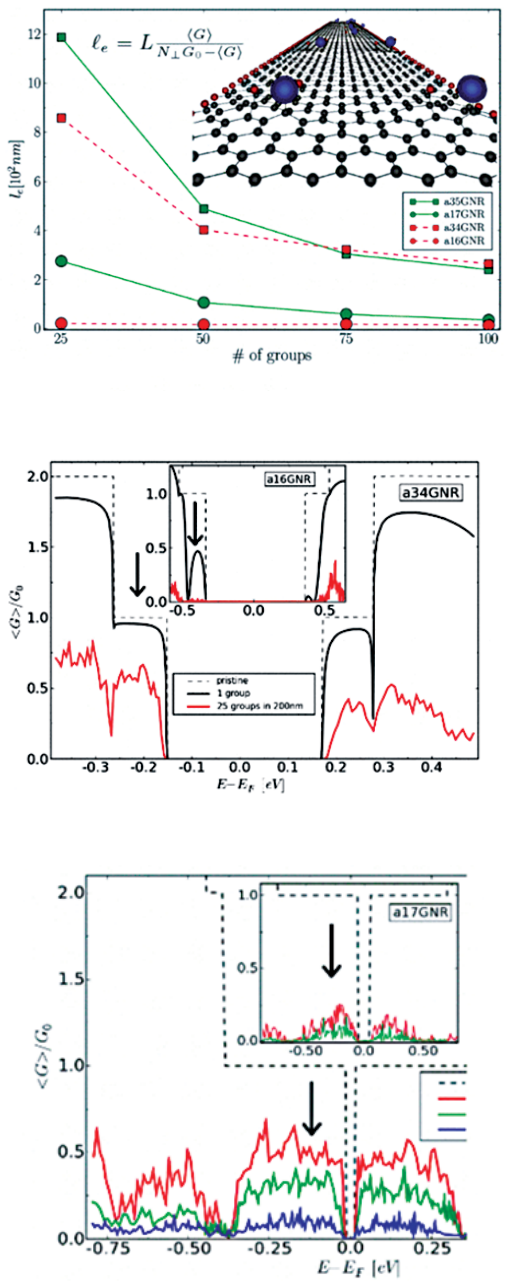

Figure 2. With the help of ab-initio calculations, the effect of functionalization on graphene nanoribbon conductance can be evaluated.

In particular, so-called order-N or quasi-order-N methodologies have been developed over the last two decades that, using the advantages of such local descriptions, allow for the calculation of the electronic structure of very large systems with a computational cost that scales linearly or close to linearly with the size of the system [22,23]. This is in contrast with traditional methods that typically show a cubic scaling with the number of electrons in the system. Order-N schemes are particularly powerful and robust for insulators and large biomolecules. However, the design of efficient and reliable order-N methods for metallic systems is still a challenge.

The most widely used codes for ab initio simulations of solids and extended systems rely on the use of the Density Functional Theory, rather than on Quantum Chemistry methods. Many of them have been developed in Europe, and some of them are commercial, although their use is mostly limited to the academic community. Among the commercial code, we can cite the plane-wave codes VASP [24] and CASTEP [25], and the Hartree-Fock/DFT code CRYSTAL [26] that utilizes Gaussian basis functions. Other widely used plane-wave codes are the public domain CP2K [27] and Abinit [28]. Abinit is distributed under GNU license and has become a very complete code with a rapidly growing community of developers. Among the most popular DFT codes using local atomic orbitals as a basis set we can mention the order-N code SIESTA [21,29], which uses a basis set of numerical atomic orbitals, and Quickstep [30], that uses a basis set of Gaussian functions.

One of the reasons why codes using basis sets of atomic orbitals have recently become very popular is that they provide the ideal language to couple with transport codes based on Non-Equilibrium-Green's functions (NEGFs) to study transport properties in molecular junctions and similar systems. Using the local language implicit behind the use of atomic orbitals (with tight-binding-like Hamiltonians) is trivial to partition the system in different regions that can be treated on different fotings. For example, it becomes relatively simple to combine information from a bulk calculation to describe the electrodes with information obtained from a simulation that explicitly considers the active part of the device. Again Europe has taken the lead along this path. Two of the most popular simulation tools for ballistic transport using NEGFs combined with DFT have been developed

based on the SIESTA code: tranSIESTA [31] and Smeagol [32]. In particular, tranSIESTA was developed by a collaboration of Danish and Spanish research groups and, although there is a public domain version that will be distributed with the latest version of the SIESTA code (siesta.3.0), it has also given rise to a commercial simulation package called QuantumWise [33].

Electronic structure theory represents the lowest and most sophisticated level of computation in our simulation hierarchy. At this level there are many different degrees of rigor and associated errors in the computations. The most accurate results are provided by post-Hartree-Fock Quantum Chemical methods. Unfortunately, they are extremely demanding and not well suited for simulations of solids and condensed matter systems. As already mentioned, the most popular approach to study such systems is Density Functional Theory, which provides a good balance between the computational cost and the accuracy of the results. However, even at the DFT level, ab initio calculations are computationally too demanding to perform realistic simulations of devices. Therefore, it is necessary to develop more approximate methods and, finally, to combine them in the so-called multi-scale approaches, in which different length scales are described with different degrees of accuracy and detail.

An interesting intermediate stage between DFT calculations, which take into account the full complexity of the materials, and empirical models, which disregard most of the chemistry and structural details of the system, is provided by the tight-binding approaches. Here a minimal basis of atomic orbitals is used to describe the electronic structure of the system. As a consequence, only the valence and lowest lying conduction bands can be accurately treated. Traditionally, the hopping and overlap matrix elements were considered empirical parameters that were adjusted to describe the electronic band structure of the material and its variation with strain. This has proven a quite powerful approach to describe complex system like, for example, quantum dots containing thousands or millions of atoms [34, 35].

A very interesting variation of these methods has been developed in recent years: the so-called DFT-tight-binding. Here the tight-binding parameters (hoppings, overlaps and short-ranged interatomic repulsive potentials) are not obtained by fitting to empirical information but they are obtained from DFT calculations for simple systems (mainly diatomic molecules) [36]. The parameters obtained in this way have proven to be transferable enough to provide a reasonable description of systems like large molecules and even solids.

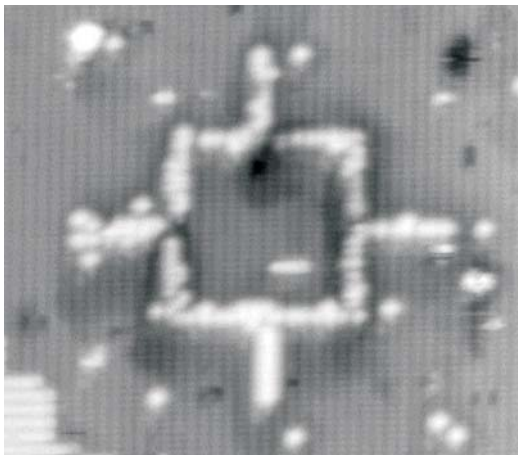

Figure 3. Ultra-high-vacuum STM image of a substrate after the fabrication with single-atom manipulation, of a complete interconnection circuit for an OR gate, obtained by removing hydrogen atoms from a silicon hydride surface.

The ability to treat varying length and time scales, within varying degrees of approximation, leads to the already mentioned requirement for a multi-scale approach to coupled materials/device simulation. Although a multi-scale approach is more than ever needed at this stage, parameter extraction cannot be performed for a generic material, but must be targeted for the particular device structure being considered, especially for single-molecule transistors. There has to be a closed loop between the atomistic portion of the simulation and the higher-level parts, guaranteeing a seamless integration. This convergence between material and device studies also implies that a much more interdisciplinary approach than in the past is needed, with close integration between chemistry, physics, engineering, and, in a growing number of cases, biology.

To make an example, let us consider the simulation of a silicon nanowire transistor: atomistic calculations are needed to determine the specific electronic structure for the cross-section of the device being investigated, then this information can be used in a full-band solver

for transport or parameters can be extracted for a simpler and faster transport analysis neglecting interband tunneling; then the obtained device characteristics can be used for the definition of a higher-level model useful for circuit analysis. It is apparent that, for example, the atomistic simulation is directly dependent on the device geometry, and that, therefore, work on the different parts of the simulation hierarchy has to be performed by the same group or by groups that are in close collaboration. Indeed, the dependence between results at different length scales sometimes requires the combination of different techniques in the same simulation, not just the use of information from more microscopic descriptions to provide parameters for mesoscopic or macroscopic models. Following the previous example, the electronic properties of a silicon nanowire are largely determined by its geometry.

However, the geometry of the wire is determined by the strain present in the region where it grows, which in turn is a function of the whole geometry of the device, its temperature and the mechanical constraints applied to it. Thus, a reliable simulation of such device can require, for example, a quantum mechanical description of the nanowire itself, coupled to a larger portion of material described using empirical interatomic potentials, and everything embedded in an even much larger region described using continuum elastic theory. Although still at its infancy, this kind of multi-scale simulations has already been applied very successfully to the study of quite different systems, like biological molecules, crack propagation in mechanical engineering or combustion processes [37, 38]. This is certainly one of the most promising routes towards the simulation of realistic devices.

Another example where multi-scale and multi-physics simulations become essential is represented by the effort to merge electronics with nanophotonics. The integration of CMOS circuits and nanophotonic devices on the same chip opens new perspectives for optical interconnections (higher band widths, lower-latency links compare with copper wires) as well as for the possible role of photons in the data processing. These involve the modelling of "standard" passive components, such as waveguides, turning mirrors, splitters and input and output couplers, as well as active elements, such as modulators and optical switches. Modelling of ultra-scaled optoelectronic components involve the design of nanometer scale optical architectures with new properties that may differ considerably from those of their macroscopic counterparts.

This requires the development of new numerical tools able to describe electromagnetic interactions and light propagation at different length scales. They should be able to describe the electromagnetic field from the scale of a few light wavelengths (already of the order of the whole micro-device) down to the nanometer scale elements. These new tools should include a realistic description of the optical properties including electro- and magneto-optical active nanostructures and plasmonic elements which are expected to be key ingredients of a new generation of active optoelectronic components.

A mayor challenge of the "multi-physical" modelling will be to simulate a full nanodevice where electronics, mechanics and photonics meet at the nanoscale. For instance, the coupling between mechanical vibrations and quantum conductance of single nanotubes has been recently observed. The interaction of an optical field with a device takes place not only through the electromagnetic properties, but also through the mechanical response (radiation pressure forces). The physical mechanisms and

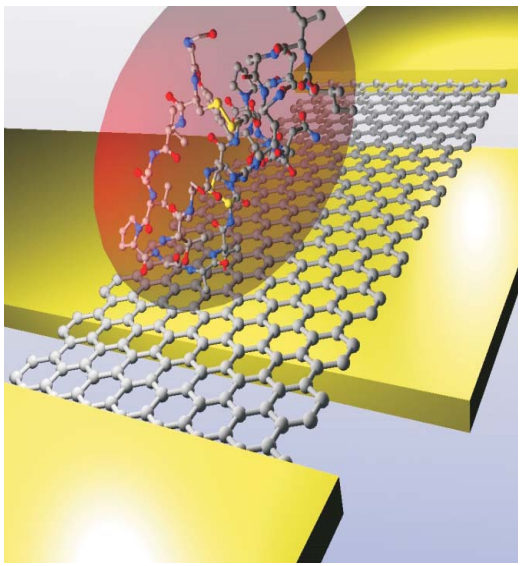

Figure 4. Functionalized graphene nanoribbons can be used to detect organic molecules.

possible applications of optical cooling of mechanical resonators are being explored. Modelling Nano-Electro-Mechano-Optical (NEMO) devices is going to play a key (and fascinating) role in the development and optimization of new transducers and devices.

Thus, one of the main challenges for modelling in the next few years is the creation of well organized collaborations with a critical mass sufficient for the development of integrated simulation platforms and with direct contacts with the industrial world.

Carbon-based electronics and spintronics

Amongst the most promising materials for the development of beyond CMOS nanoelectronics, Carbon Nanotubes & Graphene-based materials and devices deserve some particular consideration. Indeed, first, their unusual electronic and structural physical properties promote carbon nanomaterials as promising candidates for a wide range of nanoscience and nanotechnology applications. Carbon is unique in possessing allotropes of each possible dimensionality and, thus, has the potential versatility of materials exhibiting different physical and chemical properties. Diamond (3D), fullerenes (0D), nanotubes (1D-CNTs), 2D graphene and graphene ribbons are selected examples. Because of their remarkable electronic properties, CNTs or graphene-based materials should certainly play a key role in future nanoscale electronics. Not only metallic nanotubes and graphene offer unprecedented ballistic transport ability, but they are also mechanically very stable and strong, suggesting that they would make ideal interconnects in nanosized devices. Further, the intrinsic semiconducting character of either nanotubes or graphene nanoribbons, as controlled by their topology, allows us to build logic devices at the nanometer scale, as already demonstrated in many laboratories. In particular, the combination of 2D graphene for interconnects (charge mobilities in graphene layers as large as 400.000 $cm^2V^{-1}s^{-1}$ have been reported close to the charge neutrality point) together with graphene nanoribbons for active field effect transistor devices could allow the implementation of completely carbon-made nanoelectronics.

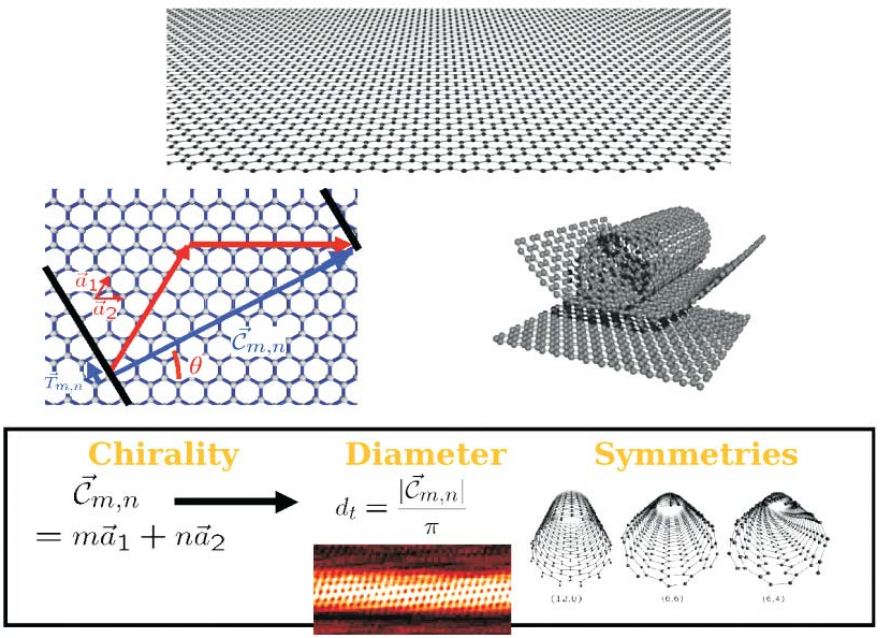

Figure 5. A carbon nanotube consists of a rolled up sheet of graphene.

Besides the potential of 2D graphene and GNRs for electronic device applications, transport functionalities

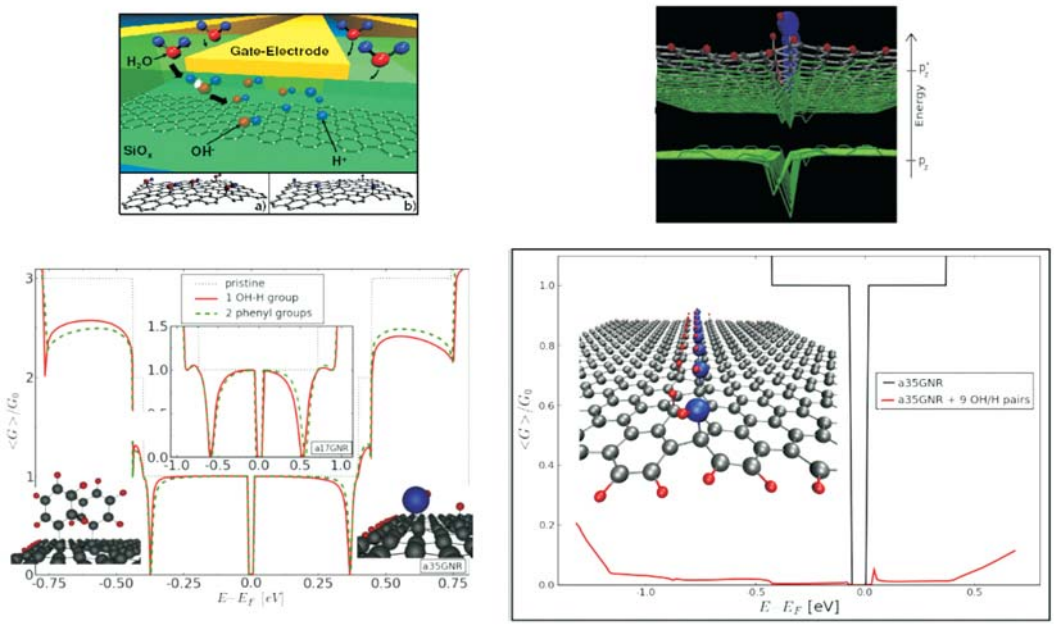

Figure 6. Functionalization of graphene nanoribbons.

involving the spin of the carriers have very recently received a particularly strong attention. First, although spin injection through ferromagnetic metal/semiconductor interfaces remains a great challenge, the spectacular advances made in 2007 converting the spin information into large electrical signals using carbon nanotubes [39] has opened a promising avenue for future carbon-based spintronic applications. The further demonstration of spin injection in graphene [40] and the observation of long spin relaxation times and lengths [41] have suggested that graphene could add some novelty to carbon-based spintronics. For instance, taking advantage of the long electronic mean free path and negligible spin-orbit coupling, the concept of a spin field-effect transistor with a 2D graphene channel has been proposed with an expectation of near-ballistic spin transport operation [42]. A gate-tunable spin valve has been experimentally demonstrated [43]. Finally, a ferromagnetic insulator, such as EuO, may be used to induce ferromagnetic properties into graphene, through the proximity effect [44] and also to control the spin polarization of current by a gate voltage [45, 46]. This configuration does not make use of any ferromagnetic metallic contact to inject spin-polarized electrons. Thus, it could be a way to circumvent the problem of "conductivity mismatch" [47-49] which possibly limits the current spin injection efficiency into a conventional semiconductor from a ferromagnetic metal. These phenomena and the corresponding devices need to be investigated using the appropriate models of relativistic-like electron transport in 2D graphene structures. Additionally, the presence of spin states at the edges of zigzag GNRS has also been demonstrated [50-52], and may be exploited for spintronics. Using first-principles calculations, very large values of magnetoresistance have been predicted in GNR-based spin valves [53,54].

Additionally, the potential for 3D based organic spintronics has been recently suggested by experimental studies [55]. Organic spin valves have shown spin relaxation times in the order of the microsecond and spin tunnel junctions with organic barriers have recently shown magnetoresistance values in the same order of magnitude as that of inorganic junctions based on Al_2O_3. However, spin transport in these materials is basically unknown, and many groups are trying to decipher the

impressive experimental complexity of such devices. Organic materials, either small molecules or polymers, will definitely allow large scale and low cost production of alternative non volatile memory technologies, with reduced power consumption. These new materials have therefore the potential to create an entirely new generation of spintronics devices, and the diverse forms of carbon-based materials open novel horizons for further hybridization strategies and all-carbon spintronics circuits, including logic and memory devices.

The performance of these spintronic devices relies heavily on the efficient transfer of spin polarization across different layers and interfaces. This complex transfer process depends on individual material properties and also, most importantly, on the structural and electronic properties of the interfaces between the different materials and defects that are common in real devices. Knowledge of these factors is especially important for the relatively new field of carbon based spintronics, which is affected by a severe lack of suitable experimental techniques capable of yielding depth-resolved information about the spin polarization of charge carriers within buried layers of real devices.

In that perspective, it is noteworthy to remark that the fantastic development of first principles non-equilibrium transport methods is progressively allowing for more and more realistic assessment and anticipation on the true spintronics potential of carbon-based structures. This aspect also stands as an essential point for providing guidance and interpretation schemes to experimental groups. As a matter of illustration, a few years ago it has been theoretically shown that organic spin valves, obtained by sandwiching an organic molecule between magnetic contacts, could manifest large bias-dependent magnetoresistance, provided a suited choice of molecules and anchoring groups was made, which is now confirmed by experiments [56].

Finally one also notes that in addition to the potential for GMR in carbon-based materials, the spin manipulation and the realization of spin Qubits deserves a genuine consideration. Recent theoretical proposals have shown that spin Qubits in graphene could be coupled over very long distances, as a direct consequence of the so-called Klein paradox inherent to the description of charge excitations in terms of massless Dirac fermions.

The related challenges for device fabrication need to be observed from different perspectives. Indeed, recent experiments in ^{13}C nanotubes reveal surprisingly strong nuclear spin effects that, if properly harnessed, could provide a mechanism for manipulation and storage of quantum information.
This may help to overcome the performance limitations of conventional materials and of the conventional technology for spin valve devices. The real potential of graphene-based materials for FET and related spintronics applications thus requires advanced modelling methods, including *ab initio* techniques, and a precise description of spin degree of freedom.

To date, the development of nanotubes and graphene science have been strongly driven by theory and quantum simulation [57,58]. The great advantage of carbon-based materials and devices is that, in contrast to their silicon-based counterparts, their quantum simulation can be handled up to a very high level of accuracy for realistic device structures. The complete understanding and further versatile monitoring of novel forms of chemically-modified nanotubes and graphene will however lead to an increasing demand for more sophisticated computational approaches, combining first principles results with advanced order N schemes to tackle material complexity and device features, as developed in some recent literature [59].

The molecular scale and the end of the road

Molecular electronics research continues to explore the use of single molecules as electron devices or for even more complex functions such as logic gates [60]. Experimentally and theoretically the majority of research work focuses on single molecules between two metallic electrodes or on molecular tunnel junctions.
Reproducibility of the measurements and accurate predictions for currents across single molecule tunnel junctions remains a challenging task, although the results of theory and experiment are converging [61]. To achieve the goal of using molecular components for computing or storage, or indeed for novel functions, requires refinement of the theoretical techniques to better mimic the conditions under which most experiments are performed and to more accurately describe the electronic structure of the molecules connected to the leads.

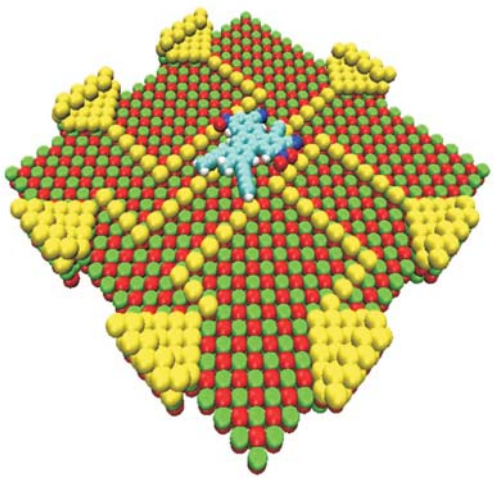

*Figure 7. Molecule connected to seven atomic wires on a ionic crystal. This setup is composed of 2025 atoms and more than 9700 atomic orbitals are needed to accurately calculate the function of the molecule (from "Picotechnologies : des techniques pour l'échelle atomique", C. Joachim, A. Gourdon and X. Bouju in Techniques pour l'ingénieur **NM130**, 1-16 (2009).*

Most simulations of transport in molecular junctions to date are based on the combination of the non-equilibrium Green's functions techniques with DFT calculations [62,63]. Although this approach has proven quite powerful, it also presents important shortcomings. In particular, the transport calculation is based on the Kohn-Sham spectrum as calculated using standard local or semi-local exchange-correlation functionals. These functionals usually give a reasonable description of the electronic spectrum for the normal metals that constitute the leads. However, they are known to be much less reliable to predict the energy spectrum of small molecules. This is extremely important, since the relative position of the molecular levels and the Fermi energy of the leads is crucial to determine the transport characteristic. Some of the deficiencies of DFT to describe localized levels can be corrected by including the so-called self-interaction corrections [64]. Still, the position of the molecular levels is also strongly influenced by the dynamical screening induced by the metallic leads [65,66]. An accurate description of all these effects requires more elaborate theoretical treatments, beyond standard DFT calculations. Fortunately, part of the effects of screening can be included using a simple non-local self-energy model that basically contains image charge interactions that affect differently the HOMO and LUMO levels [68].

Another interesting issue is that of the coupling of the electrons with structural deformations and vibrational modes. Within the framework of NEGF+DFT calculations inelastic effects associated with the excitation of localized vibration within the contact region have been successfully included in recent years. Most of the approaches rely on different perturbative expansions or on the so-called self-consistent Born approximation [69]. This allows for accurate simulations of the inelastic signal in molecular junctions and, therefore, the characterization of the path followed by

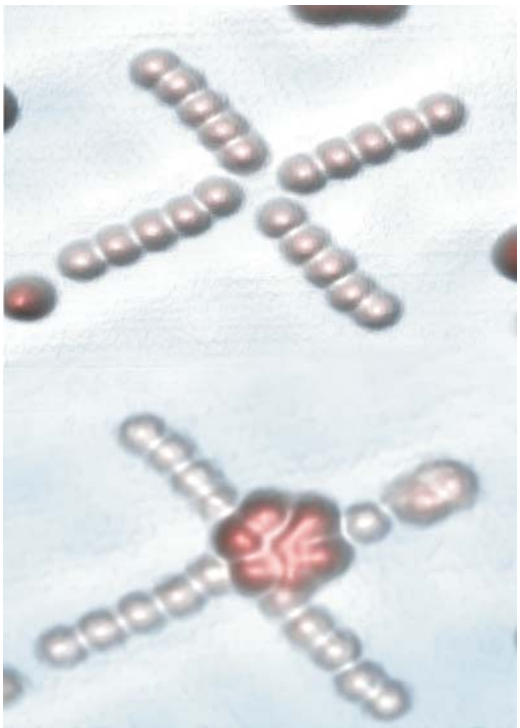

Figure 8. Connection of a molecule to four atomic wires. Each wire has been fabricated (left panel) with five gold atoms deposited on the substrate; the molecule has then been placed at the center of the device (right panel), slightly modifying the structure of one of the wires.

the electrons by identifying which vibrations are excited during the conduction process. Unfortunately, the self-consistent Born approximation does not allow accounting for polaronic effects that are crucial to understand the electronic transport in flexible organic molecules [70]. In these cases more sophisticated methods are necessary, the coupling of which to ab initio DFT simulations is still an open question.

Hence much of the work to date has focused on the underlying physical mechanisms of charge transport across molecules, whereas very little is understood in terms of the use of molecular components in complex, or even simple, circuits. This research area could also be categorized as in its infancy in that very little is known about time-dependent or AC responses of molecules in tunnel junctions or other circuit environments. To exploit molecules in information processing, the use of multi-scale tools [71] as described previously are needed to embed molecular scale components between what are essentially classical objects: leads, drivers, and circuits. Further development of the simulations is needed to accurately describe the transport processes in molecular junctions and its coupling to structural degrees of freedom and, in particular, to molecular vibrations also in the time-dependent response of the molecules to external voltages and their interaction with light needs to be studied.

Finally, to position a single molecule at the right place, experimental equipment has to be developed with accurate manipulation capabilities, as well as precision electrical probes for four terminal measurements [72]. Further development of the simulation techniques is needed to describe the time-dependent response of molecules to external voltages and their interaction with light. As the size of molecules considered as a component remains quite large, adapted methods using a scattering approach seem to be more relevant than high-level NEGF or other sophisticated methods [73,74]. The concept of a molecular logic gate has emerged recently and specific approaches including quantum Hamiltonian computing [75] will be used for a numerical integration.

Nano-bio-electronics

A further fundamental research line which emerged in parallel to the development of molecular electronics is bio-electronics. It mainly aims at (i) mimicking of biological and biophysical processes via molecular electronic circuits, and (ii) the exploitation of self-assembling and self-recognition properties of many biomolecules as scaffolds in the integration of nano- and sub-nanoscale devices, and (iii) exploring the potential of arrays of biomolecules (like DNA and its artificial modifications) to serve as molecular wires interconnecting different parts of molecular electronic devices. Obviously, great challenges from both the experimental and from the theoretical side exist on the road to achieve such goals.

The theoretical understanding of the bio/inorganic interface is in its infancy, due to the large complexity of the systems and the variety of different physical interactions playing a dominant role. Further, state of the art simulation techniques for large biomolecular systems are to a large degree still based on classical physics approaches (classical molecular dynamics, classical statistical physics); while this can still provide valuable insight into many thermodynamical and dynamical properties of biomolecular systems, a crucial point is nevertheless missing: the possibility to obtain information about the electronic structure of the biomolecules, an issue which is essential in order to explore the efficiency of such systems to provide charge migration pathways. Moreover, due to the highly dynamical character of biomolecular systems - seen e.g. in the presence of multiple time scales in the atomic dynamics- the electronic structure is strongly entangled with structural fluctuations. We are thus confronting the problem of dealing with the interaction of strongly fluctuating complex molecules with inorganic systems (substrates, etc).

As a result, multi-scale simulation techniques are urgently required, which should be able to combine quantum-mechanical approaches to the electronic structure with molecular dynamical simulation methodologies dealing with the complex conformational dynamics of biological objects. Conventional simulation tools of semiconducting microdevices can obviously not deal with such situations.

Thermoelectric energy conversion

The importance of research on thermoelectric energy conversion is growing in parallel with the need for alternative sources of energy. With the recent developments in the field, thermoelectric energy generators have become a commercial product in the market and their efficiencies are improving constantly, but the commercially available products did not take the

advantage of nano-technology yet. In fact, thermoelectricity is one of the areas in which nano-scale fabrication techniques offer a breakthrough in device performances.It was predicted theoretically that, lowering the device dimensions, it is possible to overcome the Wiedemann-Franz Law and enhance the device performances significantly [76].

Quasi one-dimensional quantum wires [77], engineered molecular junctions [78,79], superlattices of quantum dots [80] are the other possible routes proposed for achieving a high thermoelectric figure of merit, *ZT*.

The thermoelectric figure of merit includes three properties of the material, namely the electrical conductivity σ, Seebeck coefficient *S*, the thermal conductivity $\kappa=\kappa_{el}+\kappa_{ph}$ with electronic and phononic contributions as well as the temperature *T*, $ZT=\sigma S^2 T/\kappa$. In order to optimize *ZT*, an electron-crystal together with a phonon-glass behavior is required [81].

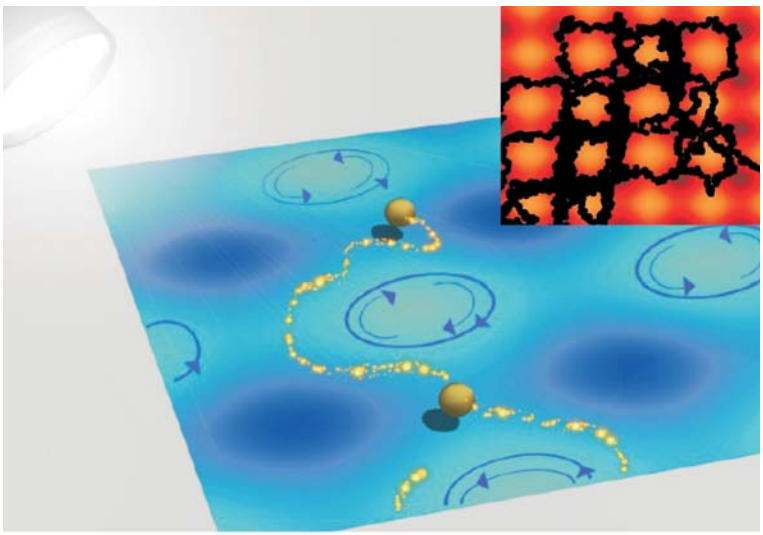

Figure 9. Diffusion processes are of fundamental importance in many disciplines of physics, chemistry and biology. A low diffusion rate may hinder progress in many issues related to technology and health improvement. For example high viscosity may prevent tailored chemical reactions or work as an undesired barrier for targeted nano-engineered drug delivery in bio-chips. The classical diffusion of a small particle in a fluid can be greatly enhanced by the light field of two interfering laser beams. Langevin Molecular Dynamics simulations show that radiation pressure vortice, due to light interference, spin the particle out of the whirls sites leading to a giant acceleration of free diffusion. The effective viscosity can then be notably reduced by simply increasing the laser intensity. [Albaladejo et al., Nano Letters 9, 3527 (2009)].

Indeed, it has recently been shown that Si nano-wires with rough surfaces can serve as high performance thermoelectric materials, since the edge roughness suppresses phonon transport by a few orders of magnitude whereas the electronic transport is weakly affected from surface roughness in these wires. Similar behavior is also reported for graphene nanoribbons where edge disorder reduces lattice thermal conductivity while electrons in the first conduction plateau stay almost intact [82].

At the sub-band edges, however, the electronic mean free path is discontinuous which yields a large increase of the Seebeck coefficient and *ZT*. Another criteria for high *ZT* is to have a narrow distribution of the energy of the electrons participating in the transport process [83]. In molecular junctions, it is shown that the Seebeck coefficient is maximized when the electrode-molecule coupling is weak and the HOMO level is close to the Fermi energy, these fulfill Mahan's criterion in the zero-dimensional case [84]. The weak coupling condition is also in favor of the need of reduced vibrational thermal conduction. Therefore self-assembled layers of molecules between semiconducting surfaces are supposed to yield high *ZT* values.

These developments offer new challenges for increasing device performances and also for the modelling of new devices. An accurate modelling of the disordered structures or of the layered structures of self-assembled molecules between surfaces requires a lot of improvements both from the methodological and from the computational point of view. Simulation of these systems entails consideration of very large number of atoms, of the order of 10^6 to 10^8. Therefore fully parallelized order - *N* methods for both electronic and

phononic computations are needed. Though important progress has been achieved in order-N electronic calculations, such methods are still lacking a proper description for the phonons. Adoption of the methods already developed for electrons to phonons is a first goal to be achieved.

Multifunctional oxides

Multifunctional oxides, ranging from piezoelectrics to magnetoelectric multiferroics, offer a wide range of physical effects that can be used to our advantage in the design of novel nanodevices. For example, these materials make it possible to implement a variety of tunable and/or switchable field effects at the nanoscale. Thus, a magnetoelectric multiferroic can be used to control the spin polarization of the current through a magnetic tunnel junction by merely applying a voltage; or a piezoelectric layer can be used to exert very well controlled epitaxial-like pressures on the adjacent layers of a multilayered heterostructure, which e.g. can in turn trigger a magnetostructural response.

These are just two examples of many novel applications that add up to the more traditional ones – as sensors, actuators, memories, highly-tunable dielectrics, etc. – that can now be scaled down to nanometric sizes by means of modern deposition techniques. In fact, nanostructuring of different types, ranging from the construction of oxide nanotubes to the more traditional multi-layered systems, is opening the door to endless possibilities for the engineering/combination of the properties of this type of compounds, which are strongly dependent on the system's size and (electrical, mechanical) boundary conditions.

The current challenges in the field are plenty, from the more technical to the more fundamental. At the level of the applications, the outstanding problems include the integration of these materials with silicon or the identification of efficient and scalable growth techniques for complex oxide heterostructures.

At a more fundamental level, there is a pressing need to identify new systems and/or physical mechanisms that can materialize some of the most promising concepts for the design of devices; for example, we still lack a robust room-temperature magnetoelectric multiferroic system that can be integrated in real devices, we still have to understand the main factors controlling the performance of a ferroelectric tunnel junction, etc.

Finally, it should be stressed that the field is rich in opportunities for the emergence of novel effects and concepts that go beyond the current prospects in the general area of electronics, the recent discovery of high electronic mobilities in all-oxide heterostructures (i.e., at the interfaces between $LaAlO_3$ and $SrTiO_3$) being a remarkable example.

Quantum-mechanical simulation is playing a key role in the progress in multifunctional oxides. This has been historically the case, with many key contributions from the first-principles community to the understanding of ferroelectric, magnetic and magnetoelectric bulk oxides [85,86]. This trend is just getting stronger in this era of nanomaterias, for two reasons: (i) there is greater need for theory to explain the novel physical mechanisms at work in systems that are usually very difficult to characterize experimentally, and (ii) modern deposition techniques offer the unique chance to realize in the laboratory the most promising theoretical predictions for new materials.

Thus, the importance of first-principles simulation for fundamental research in functional oxides is beyond doubt, and very recent developments, e.g. for the first-principles study of the basic physics of magnetoelectrics [87], ferroelectric tunnel junctions [88] or novel oxide superlattices [89], clearly prove it.

The contribution from simulations to resolve more applied problems (e.g, that of the integration with silicon) is, on the other hand, just starting, and its progress will critically depend on our ability to develop novel multi-scale simulation methods that can tackle the kinetics of specific growth processes (from pulse-laser deposition to sputtering methods under various oxygen atmospheres) directly. This is a major challenge that will certainly generate a lot of activity in the coming couple of decades.

Major current deficiencies of TCAD

A clear gap, which has in part been addressed in the previous sections, has formed in the last few years between what is available in the TCAD market and what would actually be needed by those working on the development of advanced nanoscale devices. As already mentioned, classical TCAD tools have not been upgraded with realistic quantum transport models yet, suitable for the current 32 nm node in CMOS technology or for emerging technologies, and, in addition, there are some fields of increasing strategic

importance, such as the design of photovoltaic cells, for which no well-established TCAD platforms exist.

Bottom-up approaches, which, if successful, could provide a solution to one of the major bottlenecks on the horizon, i.e. skyrocketing fabrication costs, are not supported by any type of TCAD tools as of now. This may be due to the fact that bottom-up approaches are still in their infancy and have not been demonstrated in any large-scale application, but the existence of suitable process simulation tools could, nevertheless, facilitate their development into actual production techniques. Sophisticated tools that have been developed within research projects are available on the web, mainly on academic sites, but they are usually focused on specific problems and with a complex and non-standardized user interface.

An effort would be needed to coordinate the research groups working on the development of the most advanced simulation approaches, the TCAD companies and the final users, in order to define a common platform and create the basis for multi-scale tools suitable to support the development of nanoelectronics in the next decade.

New computational approaches

The development of highly parallel and computationally efficient graphic processors has recently provided a new and extremely powerful tool for numerical simulations. Modern Graphic Processing Units (GPU) approach a peak performance of a Teraflop (10^{12} floating point operations per second) thanks to a highly parallel structure and to an architecture focusing specifically on data processing rather than on caching or flow control. This is the reason why GPUs excel in applications for which floating point performance is paramount while memory bandwidth in not a primary issue. In particular, GPU hardware is specialized for matrix calculations (fundamental for 3D graphic rendering), which do represent also the main computational burden in many types of device simulations.

As a result, speed ups of the order of 30 - 40 have been observed, for tasks such as the simulation of nanoscale transistors, with respect to state-of-the-art CPUs. Up to now the main disadvantage was represented by the availability, in hardware, only of single-precision operations, but last generation GPUs, such as the FireStream 9170 by AMD, are advertised as capable of handling double precision in hardware, although at a somewhat reduced rate (possibly by a factor of 5). Another impressive feature of GPU computation is the extremely high energy efficiency, of the order of 5 Gigaflops/W in single precision or 1 Gigaflop/W in double precision, an aspect of growing importance considering the costs for supplying power and air conditioning to computing installations.

The latest GPU hardware opens really new perspectives for simulation of nanodevices, also in "production environments," because GPU based systems could be easily standardized and provided to end-users along with the simulation software. Overall, this is a field that deserves investing some time and effort on the part of the device modelling community, because it could result in a real breakthrough in the next few years.

Overview of networking for modelling in Europe and the United States

In the United States, the network for computational nanotechnology (NCN) is a six-university initiative established in 2002 to connect those who develop simulation tools with the potential users, including those in academia, and in industries. The NCN has received a funding of several million dollars for 5 years of activity.

One of the main tasks of NCN is the consolidation of the nanoHUB.org simulation gateway, which is currently providing access to computational codes and resources to the academic community. According to NCN survey [23], the total number of users of nanoHUB.org reached almost 70.000 in March 2008, with more than 6.000 users having taken advantage of the online simulation materials.

The growth of the NCN is likely to attract increasing attention to the US computational nanotechnology platform from all over the world, from students, as well as from academic and, more recently, industrials researchers. In Europe an initiative similar to the nanoHUB, but on a much smaller scale, was started within the EU funded "Phantoms network of excellence" and has been active for several years; it is currently being revived with some funding within the nanoICT coordination action. (www.europa.iet.unipi.it)

In a context in which the role of simulation might become strategically relevant for the development of nanotechnologies, molecular nanosciences, nanoelectronics, nanomaterial science and nanobiotechnologies, it seems urgent for Europe to set up a computational platform infrastructure similar to NCN, in order to ensure its positioning within the international competition. The needs are manifold. First, a detailed identification of European initiatives and networks must be performed, and de-fragmentation of such activities undertaken. A pioneer initiative has been developed in Spain through the M4NANO database (www.m4nano.com) gathering all nanotechnology-related research activities in modelling at the national level.

This Spanish initiative could serve as a starting point to extend the database to the European level. Second, clear incentives need to be launched within the European Framework programmes to encourage and sustain networking and excellence in the field of computational nanotechnology and nanosciences. To date, no structure such as a Network of Excellence exists within the ICT programme, although the programme NMP supported a NANOQUANTA NoE in FP6, and infrastructural funding has been provided to the newly established ETSF (European Theoretical Spectroscopy Facility, www.etsf.eu). This network mainly addresses optical characterization of nanomaterials, and provides an open platform for European users, that can benefit from the gathered excellence and expertise, as well as standardized computational tools. There is also a coordinated initiative focused on the specific topic of electronic structure calculations, the Psi-k network (www.psi-k.org).

An initiative similar to the American NCN would be needed in Europe, within the ICT programme that encompasses the broad fields of devices and applications or, better, in conjunction between the ICT and the NMP programme, since the full scope from materials to devices and circuits should be addressed. Other initiatives such as the "Report on multiscale approaches to modelling for nanotechnology" [90] intends to provide an overview, albeit limited and certainly not exhaustive, of relevant aspects of modelling at the nanoscale, pointing out some important issues that are still open and affording the reader that is not yet active in the field with an introduction to several widely used techniques and with a large body of references.

This review has been written by experts in the fields of computational modelling; most of them have strongly contributed to the development of European excellence in recent years, and have been leading EU-initiative over FP5, FP6 and FP7. Although more efforts will be needed to bridge different communities from ab initio development to device simulation, such initiatives need to be supported considering that contributors of this report are overviewing promising methodologies to fill the gap between scientific communities, establishing some framework for further promoting European-based networking activities and coordination.

Past, present and future European advances in computational approaches.

This novel initiative should be able to bridge advanced ab-initio/atomistic computational approaches to ultimate high-level simulation tools such as TCAD models that are of crucial importance in software companies. Many fields such as organic electronics, spintronics, beyond CMOS nanoelectronics, nanoelectromechanical devices, nanosensors, nanophotonics devices definitely lack standardized and enabling tools that are however mandatory to assess the potential of new concepts, or to adapt processes and architectures to achieve the desire functionalities. The European excellence in these fields is well known and in many aspects overcomes that of the US or of Asian countries. Within the framework of a new initiative, specific targets should be addressed in relation with the modelling needs reported by small and medium sized software companies active in the development of commercial simulation tools, such as

QUANTUM WISE (www.quantumwise.com)
SYNOPSYS (www.synopsys.com)
NANOTIMES (www.nanotimes-corp.com)
SILVACO (www.silvaco.com)
NEXTNANO3 (www.nextnano.de)
TIBERCAD (www.tibercad.org)

Similarly, larger companies such as STMicroelectronics, Philips, THALES, IBM, INTEL make extensive usage of commercial simulation tools to design their technological processes, devices and packaging. The

sustainable development of the computational simulation software industry, including innovative materials (carbon nanotubes, graphene, semiconducting nanowires, molecular assemblies, organics, magnetic material) and novel applications (spintronics, nanophotonics, beyond CMOS nanoelectronics), could therefore be crucial to foster industrial innovation in the next decade.

Conclusions

Recent advances in nanoscale device technology have made traditional simulation approaches obsolete from several points of view, requiring the urgent development of a new multiscale modelling hierarchy, to support the design of nanodevices and nanocircuits. This lack of adequate modeling tools is apparent not only for emerging devices, but also for aggressively scaled traditional CMOS technology, in which novel geometries and novel materials are being introduced. New approaches to simulation have been developed at the academic level, but they are usually focused on specific aspects and have a user interface that is not suitable for usage in an industrial environment.

There is therefore a need for integration of advanced modelling tools into simulators that can be proficiently used by device and circuit engineers: they will need to include advanced physical models and at the same time be able to cope with variability and fluctuations, which are expected to be among the greatest challenges to further device down scaling.

In addition, as dimensions are scaled down, the distinction between material and device properties becomes increasingly blurred, since bulk behavior is not observed any more, and atomistic treatments are needed. There is therefore a convergence between material and device research, which should be reflected also in the formulation of research projects.

Furthermore, new materials, such as carbon, bio-molecules, multifunctional oxides, are emerging, with an impressive potential for device fabrication and with completely new requirements for simulation. A unique opportunity is now surfacing, with powerful new modelling approaches being developed and new low-cost computational platforms (such as GPUs) with an unprecedented floating point performance.

The combination of these two factors makes it clear that the time is ripe for a new generation of software tools, whose development is of essential importance for the competitiveness and sustainability of European ICT industry, and which requires a coordinated effort of all the main players.

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3.3 Mono-molecular electronics on a surface: challenges and opportunities

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1. Introduction

Technology continues to produce functioning transistors on ever smaller scales. The day will come soon, however, when there will not be enough atoms on the surface of a semi-conductor to define the structure of a transistor and, consequently, of complex electronic circuits. At this stage, new approaches and new technologies are necessary for building computers, memory or telecommunication devices [1]. Anticipating this challenge, researchers in a few laboratories around the world are now looking for the maximum number of atoms required to fabricate, for example, a calculating unit able to perform a computation by itself.

This problem of creating an atom based techno-logy is not limited to electronics or to telecommunication and encompasses all types of devices, including mechanical machines and transducers. Meeting the atom technology challenge for ICTs requires new understanding in four now well identified fields of science and technology:

1. Learning the kinds of architectures for molecule-machines (or atom surface circuits) which will permit to perform for example complex logic operations stabilized at the surface of a solid where the required interconnection will be constructed.

2. Creating a surface multi-pads interconnection technology with a picometer precision, respecting the atomic order of the surface which is supporting the nano-system assemblage.

3. Cultivating molecular surface science accompanied with molecule synthesis (respectively atom by atom UHV-STM fabrication on a surface).

4. Creating a packaging technology able to protect a functioning atom-technology-based machine, while at the same time insuring its portability.

Those 4 topics were discussed during the 1st nanoICT mono-molecular electronics Working Group meeting in Toulouse, France between the 8th and the 10th of December 2008.

2. The architecture

Molecular devices i.e. hybrid molecular electronics are on the agenda of the micro-electronics roadmap since the seminal Aviram-Ratner paper in 1974 [2]. Until the turn of the century, such a futurist possibility of using molecules instead of solid state devices for electronics was just considered as a game for exploring the limits of calculating machines and memory devices. Approaching the end of the ITRS roadmap, things are now changing.

Thanks to an intense experimental and theoretical effort, molecular electronics has now positively evolved from concepts to the first measurements and comparison with calculations [3]. There is now a real shift towards the full integration of a computing power in a single and the same molecule i.e. the mono-molecular approach [4]. This is now followed by exploring also the possibility of

using atomic circuit fabricated on the surface of a passivated semi-conductor surface for implementing quantum dot based computer approach [5] and may be one day a mixture of both approaches.

The different possible architectures for a single molecule (or an atomic circuit) to compute include the design of single molecule circuits in a standard electrical architecture, electronic wave-like atomic or molecule circuits located on the surface of a semi-conductor or quantum Hamiltonian like computing architectures. All those approaches are now studied by quantum chemistry software able to take into account the surface electronic structure, the interconnects and the local quantum structure of the computing circuit. Let us take the simple example of a logic gate. There are 3 ways of designing a logic gate at the atomic scale:

(1) The use of surface missing atom to fabricate an atomic scale circuit mimicking the topology of a macroscopic electronic circuit. Those surfaces are generally passivated semi-conductor surface with a relatively large gap. Atoms are extracted one at a time to create a specific surface electronic structure in the electronic surface gap. This new electronic structure will form the surface atomic circuit [6].The STM vertical manipulation of the single surface atoms can automated and proceed in parallel.

(2) The full molecule, instead of the surface can be the electronic circuit. In this case, it is the □ system of such an extended molecule which will define the circuit and the □ skeleton will ensure the full chemical stability of the molecular architecture [7]. Such a molecule will have to be directly chemisorbed to the required number of nano-metallic pads or in a very dedicated approach to surface atomic wires more able to interact with specific part of the □ molecular orbitals.

(3) Molecular orbitals (from a large molecule or defined from a specific surface atomic circuit) can be manipulated by chemically bonding on a □ conjugated board specific chemical groups able to shift the corresponding molecular states [8]. Switchable lateral group can be very active playing donor or acceptor group to modify very locally the nodes distribution of a give molecular orbital. Such an effect can be used to design single molecule logic gate (See Figure 1) without forcing the molecule to have the topology of an electrical circuit [9].

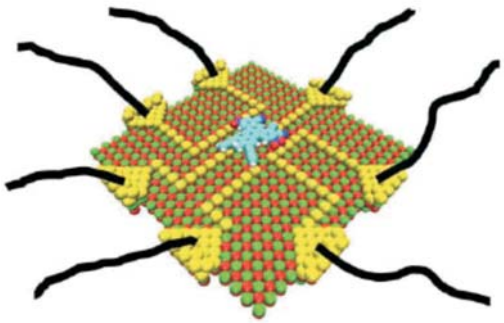

Figure 1. A possible surface implantation of a molecule logic gate. The presented molecule fi adder was designed following a Quantum Hamiltonian Computer approach [9]. The interconnection architecture is constructed using metallic atomic wires. The logic inputs are located directly on the molecular board, supposing 2 switchable chemical group current driven inputs.

Solutions (1) and (2) have been proposed long ago but are not very compatible with the quantum level where those atom circuits or molecule logic gate are supposed to work. For solution (3), a quantum Hamiltonian design of AND, NOR and even fi adder logic gates have been designed followed by proposal of chemical structure functioning on the manipulation of molecular orbitals [9].

Extreme care has to be taken here for the optimization of the chemical structure of those molecule-gates taking into account their future adsorption for example on a passivated semi-conductor surface [10]. In particular, the optimization of the electronic contact between the surface atomic wires and the molecule will be obtained by selecting with care the chemical composition of the end group of the molecule [11] for running current through the gates with the objective to reaching peak values in the range of 10 to 100 nA. All those architectures give us an indication of the richness of quantum behavior to design molecule like logic gate up to the complexity of a digital 2 by 2 full adder.

At the Working Group meeting, the question was: to what extend the complexity of such a logic function embedded in a single molecule or in a small amount of dangling bond created on purpose on a surface can be increased up for example to a N x N full adder. There is no theoretical answer yet to this question. But the interesting fact is that a careful quantum design will

certainly shift up the elementary unit of a logic circuit from the transistor level to the logic function level. For example, no gain at the gate level is required in the Hamiltonian logic gate approach. This will simplify a lot the interconnections. But at the same time, cascading the building block at the logic gate level will certainly require some power gain. This will consequently increase the complexity of the interconnection procedure in between the logic gate units. The quantum designer will have to define the most interesting building block complexity (of course beyond the transistor) to find an optimum between the computing power on board of a molecule and the required interconnects. There is no solution yet for designing dynamic memory cell at the atomic scale.

3. N-Interconnects

Creating ultra precise interconnects on a single molecule has often been a bottleneck for molecular electronics [4,12]. But there are now two well-known avenues to realize a full interconnection scheme depending if the supporting surface is a small or large electronic band gap semi-conductor. The first tentative characterization of a single molecule switch was reported already in 1988 using the HV-STM machine [13]. Since then, a lot of progresses have been accomplished using the end atom of the STM tip apex as a pointer to contact one atom [14], one molecule [3,15] and to practice single atom or molecule manipulation [16,17]. The first measurement of the conductance of a single molecule was realized in 1995 using an UHV-STM machine [3].

In parallel, nanolithography has been developed to quit the vertical STM interconnection configuration for a fully planar configuration. In year 2001, what is considered no was the nanolithography limit was reached. The world record of an inter-electrode distance of 2 nm was obtained between 2 metallic nano-electrodes fabricated on a silicon oxide [18]. But this nanotechnology technique was progressively abandoned because (1) it is limited to a maxi-mum of 2 to 3 electrodes [19] and (2) the use of resists and chemical in the process to define the nano-fabricated pattern is not clean enough with respect to the size of a single molecule and the order of the surface atoms. As a variant, break-junctions are also now used because of the very unique precision in the tuning of inter-electrode distance [12,20]. But it was analyzed by the participants of the meeting that this fantastic technique will progressively be abandoned because there is no way to determine the number of molecule in the junction, because the conformation of the molecules located in this junction is unknown and because it is difficult to foresee a multi nano-electrodes version of the break junction technique.

In 1999, a new planar nano fabrication technique, the nanostencil was introduced in an attempt to solve the surface cleanness problem [21]. Then, nanostencil was proposed as a new way to interconnect electrically a single molecule. Nanostencil has a great advantage over nano-lithography because it is supposed to preserve the atomic cleanness of the surface supporting the planar interconnection electrodes. By varying systematically all the parameter of the nanostencil technique, including the testing of a large variety of surfaces from SiO_2 to NaCl or mica, it was demonstrated that on the good surfaces, this technique reaches its limits in the 20 nm range with no possibility to master the atomic structure at the end of the so fabricated nano-pads [22].

Facing this interconnection problem, lab scale experiments were performed: the fabrication of a pseudo-planar interconnection on metal surface taking benefit from native mono atomic step edge and designing specific Lander molecules with legs to level up the molecular wire as compared to the mono atomic step edge [11,15,23]. Those low temperature UHV STM experiments unambiguously demonstrated the need for an ultra clean atomic scale mastered interaction between for example the molecular wire end and the conducting contact entity [24].

Following the Working Group discussions, it seems that all the standard planar interconnection strategies explored since the end of the 80's like e-beam nano lithography, nano-imprint and Nanostencil will soon be abandoned. A new surface science approach respecting the exact atomic order of the surface with an interconnection precision better than 0.1 nm between the atomic wire (or the molecular wire) and the atomic scale pads will have to be developed. This challenge triggers a new approach for interconnects, a formal generalization of the technique developed at Bell labs in the 50's to interconnect a bar of a Germium semiconductor material (See Figure 2 page 29). At that time, 4 probes measurement were practiced using 4

metallic tips approaching the semiconductor bar under an optical microscope. The bar was manipulated by micro metric screws together with the tips and stabilized by metallic springs [25].

In our days, atomic scale interconnection machines are starting to be built in a few labs around the world. There are basically low temperature (LT) UHV machines made of 3 LTUHV interconnect separated chambers, one for the atomic scale preparation of the supporting surface, one for single atom or molecule manipulation and one for the atomic scale to mesocale or more interconnection procedure. Depending on the surface, the navigation on the surface is still using an optical microscope completed by a NC-AFM for a large surface electronic gap (See Fig. 2). For small gap passivated semiconductor surface, the navigation is ensured by an UHV-SEM with a resolution generally around a few nanometers (See Fig. 2). For the nano interconnection step, well faceted and ultra flat metallic nano-island are now in use. Those nano-interconnect pads are positioned at will with an 0.1 nm precision on the surface using the manipulation ability of the STM [26]. For the nano to meso and more interconnection stage, one technique for small gap semiconductor is to use multiple conducting STM tips in a top or back surface approach. For large gap surfaces, the nanostencil technique can still be used at its 20 nm in width limit and in its dynamic form [27].

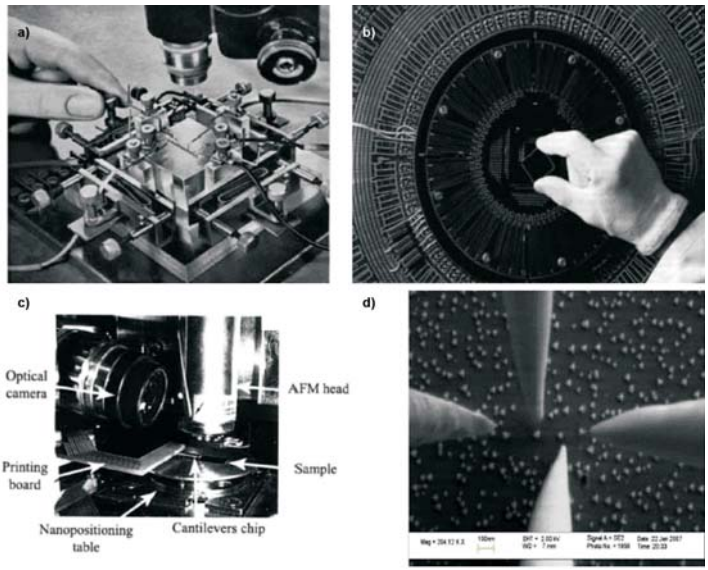

*Figure 2. History of planar multi-electrodes interconnects. (a) 1950's Bell Labs system equiped with an optical microscope and 4 electrodes for germanium interconnects [25]. (b) the 20th century multi-probes chip interconnects technology (courtesy of IBM). (c) A new generation of interconnection system involving an optical microscope plus an AFM microscope using 10 metallics cantilever positioned under the AFM head [28]. (d) A more recent version where the optical microscope had been substituted by an UHV scanning electron microscope and the metallic cantilevers substituted by nanoscale apex STM tips [26] (courtesy of the A*STAR VIP Atom tech project, Singapore).*

Those interconnection machines are so new that it is not clear how one can build up a roadmap to anticipate how many contacts it will be possible to achieve. In the case of multiple STM tips positioned under the SEM, 4 is the actual limit for stability of the interconnects (See Fig.2).For the optical microscope-NC-AFM case, 10 seems to be a good number [28]. There is here clearly a need to roadmap the computing power capacity increase embedded in a single molecule or with a surface atomic circuit and the number of possible interconnects converging towards this ultra small computing unit [19].

For example, it may happen that a well designed molecule offers too much computing power locally in regards with the maximum number of interconnects that one can physically be achieved in parallel on a surface. Then, a multiplexing like approach may be more appropriate, asking for more bandwidth and pushing the technology towards optical interconnects. Thus, efforts should be made in the future to extend experiments which aim to combine optics and local probe microscopy in an ultra clean environment with a prospect of a fully planar technology.

4. Atom and Molecule Surface science issues

The stabilization of an atomic scale computing machinery on a surface (be it self stabilized by its chemical structure or by the surface itself) requires a gigantic effort in exploring the properties of a large molecule of a surface at the atomic scale. During the Working Group meeting, a lot of questions were asked starting from the choice of the surface. Of course, the discussions were targeting lab scale logic gate handling and interconnects. For a fully packaged molecule logic gate, a more realistic choice of surfaces is actually out of the range of what can be discussed (see the corresponding section below).

Depending of the atomic scale interconnection machine to be used, a first delicate problem is the choice of the supporting surface. A list of criteria were discussed during the meeting: the electronic surface gap, the stability of the atomic surface structure, the stability of metallic nano-island on the surface. For example, we know 2 extreme cases of passivated semi-conductor surface: SiH(100) and MoS_2. SiH(100) has a surface gap around 2.1 eV. The surface H atoms can be vertically STM manipulated one at a time to create p dangling bond like surface atomic wires or Hamiltonian computing structures [5,6]. But depending on the bulk doping, those H surface atoms are not so stable with temperature which precludes a thermal growth process to shape the contacting metallic nano-island. The lamellar MoS_2 compound has a self passivated semi conducting surface with a surface gap around 1 eV.

The surface S atoms are extremely difficult to vertically STM manipulate [29]. But if manipulated, they also offer the possibility to create surface atomic wires with a band structure much more complicated that the SiH(100) [30]. The surface MoS2 surface is extremely stable up to 1200°C [31] and metallic nano-pads can easily be shaped and manipulated to construct any multi-electrode interconnections pattern with an atomic scale precision [26]. But the low surface gap of this material will certainly preclude its direct use as a supporting interconnection surface. A better exploration of the surface properties of diverse semi-conductor surfaces (See for example Figure 3 page 31) and their possible passivation is here urgently needed. Large electronic gap surface are even less explored that their semi-conductor counter parts. The nice property of those surfaces is the fact that leakage surface current between 2 metallic nano-pads adsorbed on the surface will be very low, well below the fA range, an advantage as compared with the above mentioned semi-conductor surface. The drawback is that there is no easy solution to fabricate or stabilize atomic wire on those surfaces. During the Working Group meeting, two solutions were discussed to bypass this problem: the use of molecular mold to stabilize metallic atomic wires or the use of long molecular wires between the metallic nano-pads and the central computing units. This second solution may be a good way to boost the research on long molecular wires characterized by an extremely small tunneling inverse decay rate [32].

Graphene, the new comer was also discussed in Toulouse as a mean to pass directly from the mesoscopic to the atomic scale with a "perfect" chemical like continuity between the 2 scales. This will be another choice of surface self supporting the interconnection and the computing unit. The open question is whether or not progresses in the fabrication techniques will allow an atom by atom fabrication technique respecting the absolute atomic scale precision

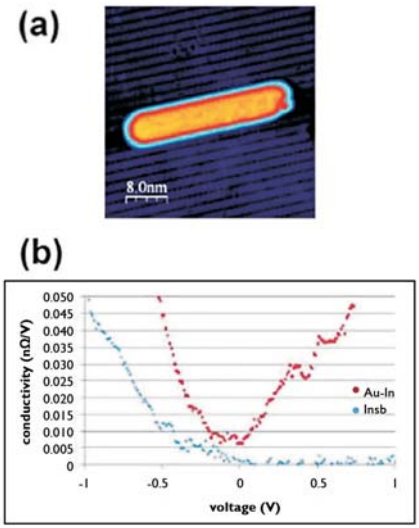

Figure 3. Exploring the surface science of interconnects: fabrication of Au nanowires on the InSb(001) surface in the UHV to be interconnected on a Fig. 2D UHV interconnection machine.(a) High resolution STM image of Au alloy nanowire formed on InSb(001) surface by a good selection of the surface annealing temperature. Bias voltage: -0.5V, tunnelling current: 25pA. (b) STS conductance measured using an

STM tip as a function of bias voltage on an Au alloy nanowire (red dots) and directly on the InSb substrate (blue dots) (Courtesy of the Jagiellonian University, Krakow).

Discussions in Toulouse about molecular surface science indicate how far we are from a very good understanding of molecular processes and behaviors of a large molecule on a surface at the atomic scale. There is here a wide range of understanding and know how which need to be acquired before creating a full atomic scale technology for molecular computing.

required for such a circuit [33]. It is also not clear how far can we go by playing with a single and large molecule adsorbed on a surface be it the one of a semi-conductor or of a bulk insulating materials. There is the difficult challenge of sublimating of a large molecular weight molecule on a surface in an ultra clean manner respecting the integrity of the molecule [34]. Maybe better to perform the chemistry in situ sublimating only the monomers and playing with them after to construct or assemble the final large molecule (See Figure 4 and [35]). It remains to be explored if such an approach can be performed for example at the surface of a semi-conductor.

5. Packaging

At the nanoICT meeting, packaging was not on the official agenda. Off site discussions about packaging indicate that we are far from being ready to study those questions simply because even the lab scale interconnection machines are just about to be assembled. Packaging is always associated with the number of interconnects which have to be stabilized with the encapsulation technology selected for the circuit [19]. There is not yet a clear path on how to create a packaging technology for surface mono-molecular electronics. A specific mono-molecular NanoICT seminar may be dedicated in the future to this very strategic problem. But it is so advance and so strategic [36] that it may turn out to be very difficult to trigger an open discussion about packaging.

6. Conclusion

The first mono-molecular nanoICT Working Group seminar was the occasion to cluster in a very Cartesian way all the 4 major issues under grounded in the mono-molecular approach of molecular electronics. In all areas of technology, the construction of a complex system by assembling elementary pieces or devices leads to a

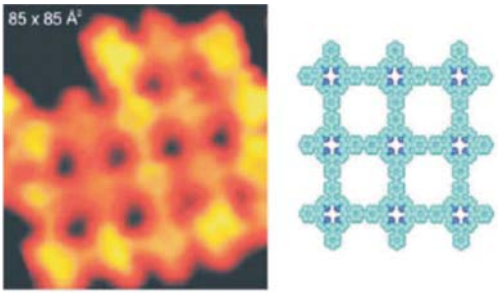

Figure 4. Playing with single molecules on a surface. Instead of sublimating a large molecule on a surface, it may be better to bring first the monomers and to make them self reacting with each others by controlling the spontaneous 2D diffusion. STM image (left) of a molecular network on a Au(111) surface with the corresponding scheme (right). The network is grown from single porphyrin (TPP) molecules monomers ("on-surface-synthesis") by forming covalent bonds between the individual building blocks [35].

Moore's law like trend when analyzing the complexity growth of the system per year, a trend which appears threatened in the near future for microelectronics. The mono-molecular approach of molecular electronics with its compulsory atomic scale technology offers way to push past possible limitations in miniaturization and to gain further increases in computing power by orders of magnitude by relying of a full development of an atom or molecule based technology for both electronics and machines. To reach this stage, each of the 4 issues well identified during this seminar will require a specific discussion and more than that a specific research and technological development program.

Acknowledgements

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3.4 BioInspired Nanomaterials

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Introduction

Over the last decades, biology has made significant advances in providing a rational understanding of the molecular mechanisms governing life's processes. New materials have emerged from life systems, which physicists and chemists have then promptly fabricated, manipulated and addressed at the molecular scale. The emblematic example is DNA technology, which affords the elaboration of programmable chemical synthesis routes to build complex architectures and functions with molecular precision, and sheds light on a new generation of robust tools.

During this same period, the semiconductor industry's development has lead to impressive performance in miniaturisation. Its current challenge though, is to develop lithographic technology for feature sizes below 20 nm and explore new classes of electronic devices based on carbon nanotubes and nanowires. A central challenge in technology is constructing multi-scale structures used to organize nanodevices and functional materials.

Bio-Inspired based information system

Nature possesses an extraordinary capacity to assemble complex nanostructures that have active and specialised functions. Our ability to precisely position distinct components providing rich functions on the nanometre scale is still limited but remains a key goal in nanotechnology and materials science.

To name but a few: DNA is emerging as an attractive tool for nanoscience and nanotechnology; Watson-Crick base pairing can be translated into binary sequences (0, 1) to organise nanomaterials in a programmable way. DNA can be used to dictate the precise positioning and connection of materials and molecules in any deliberately designed structure. Phage and cell display can be used to design new peptide sequences with dedicated functionality, binding organic to inorganic materials.

Viruses are self-assembled nanomaterials providing biological materials of well-defined size and shape. Moreover, capsids have surface properties that are well defined down to the atomic scale and viral materials are amenable to genetic engineering.

Nature uses two types of information: the genome's digital information, and environmental information such as cell-surface signals from other cells or chemical gradients. Treatment of the information at such a complex level requires multi-scale structures with appropriate integration steps. It is a formidable task to understand and copy such multi-scale systems; we face the challenges of determining the different levels of integration and engineering the interfaces from the molecular scale up to several micrometres. These challenges are well known in the fields of nanoscience and nanotechnology. For instance, the ability to precisely position distinct functional components at the nanometre scale is still limited and this is a key goal at the interface between nanoscience and materials.

State of the art

Bio-inspired fabrication methods allow the unprecedented capability to use algorithms to build elaborate, complex, architectures and functions. The bio-inspired strategy also shows capability to organise inorganic materials through biominarelisation processes that can readily design biosensors, plasmonic and nanoelectronic networks or electroactive materials.

Bio-inspired materials provide new routes to build interface properties using genetic engineering, biological combinatorial methods or targeted chemical synthesis, thus increasing the efficiency of inorganic nano objects. Another important route that should lead to significant improvement in the design of new materials and functions is the development of a new class of bio-inspired micro nanosystems that lead to new conceptions of logical functions and dynamic patterning with error corrections.

A number of European groups are involved in the use of DNA and virus technology. Since the seminal work of N.E. Seeman (http://seemanlab4.chem.nyu.edu/nanotech.html), DNA as a material for nanotechnology

[1] In April 2010 a new nanoICT Working Group, dedicated to BioICT issues was launched. This is the first version of the BioICT position paper, dealing meanly with the BioInspired Nanomaterials topic. An updated and more extended version will be published (beginning 2011).

has been widely used to connect or functionalize different nanostructures, through which versatile 2D and 3D shapes are obtained. Using DNA scaffolding to build DNA origami has further boosted the

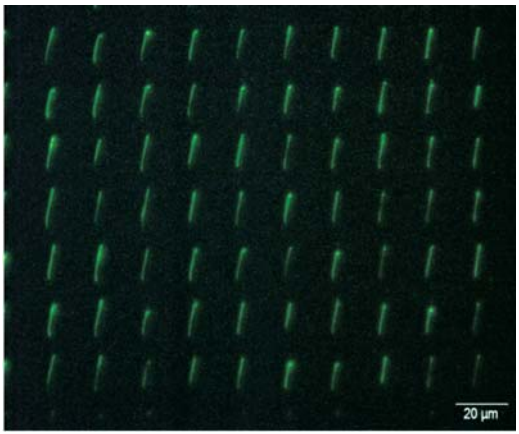


Figure 1. Stretched DNA molecules transfer-printed on a surface after directed assembly on a microstructured PDMS stamp (Courtesy Phd thesis A. Cerf, LAAS-Toulouse).

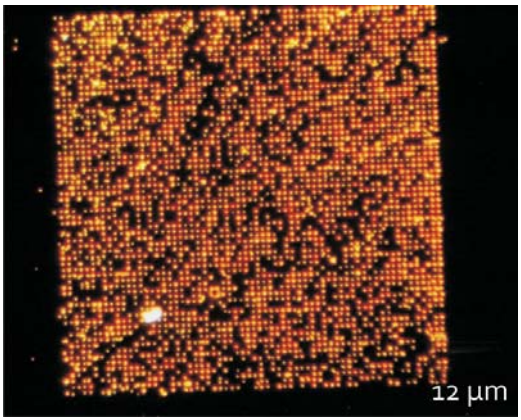
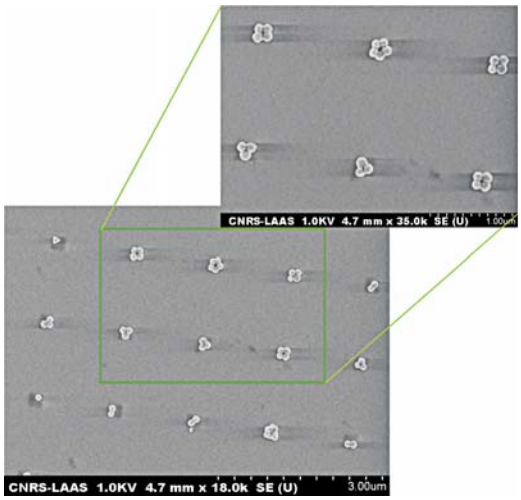


Figure 2. Dark field and SEM images of 100 nm gold nanoparticles transfer-printed on silicon after directed assembly on a nanopatterned PDMS stamp (Courtesy Phd thesis A. Cerf, LAAS-Toulouse) and A. Cerf Colloïds and surfaces (2009).

development of DNA nanotechnology (P.W.K. Rothemund (Nature, V 440, March 2006). Available 3D structures prove new routes of basic units with enough capability to already provide complex properties at their output.



DNA origami can also be used as an information-bearing seed for nucleating algorithm. Self-assembly of defined-structure geometry may introduce errors that can be reduced by controlling the competition between nucleation and growth process. Origami, as a self-supporting information seed, controls a computed structure's growth and prevents competition from the nucleation process. The key point is the encoding of the molecular or macromolecular units so that an appropriate design of short sequences can be reduced to information bits 0, 1.

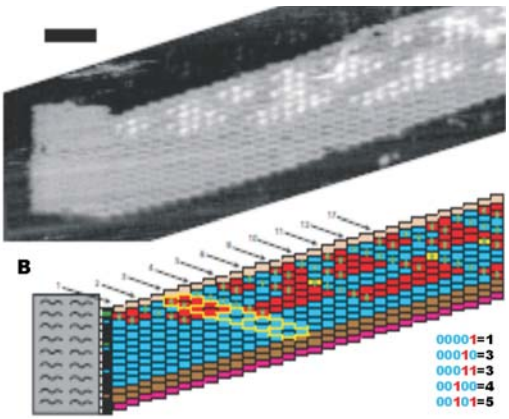


Figure 3. Algorithmic Self-Assembly of DNA Tiles: Robert D. Barish, Rebecca Schulman1, Paul W. K. Rothemund, and Erik Winfree. PNAS, April 2009, vol. 106, no. 15 6054–6059. The complexity, precision, and yield are limited by our abi-

lity to encode assembly instructions into the molecules themselves. Nucleic acids provide a platform for investigating these issues, as molecular structure and intramolecular interactions can encode growth rules. DNA tiles and DNA origami can be used to grow crystals, AFM image (A), containing a cellular automaton pattern (B).

The marriage of the top-down and bottom-up fabrication methods paves the way to arrange complex molecular nano units, to electronically address and integrate them into a functional device.

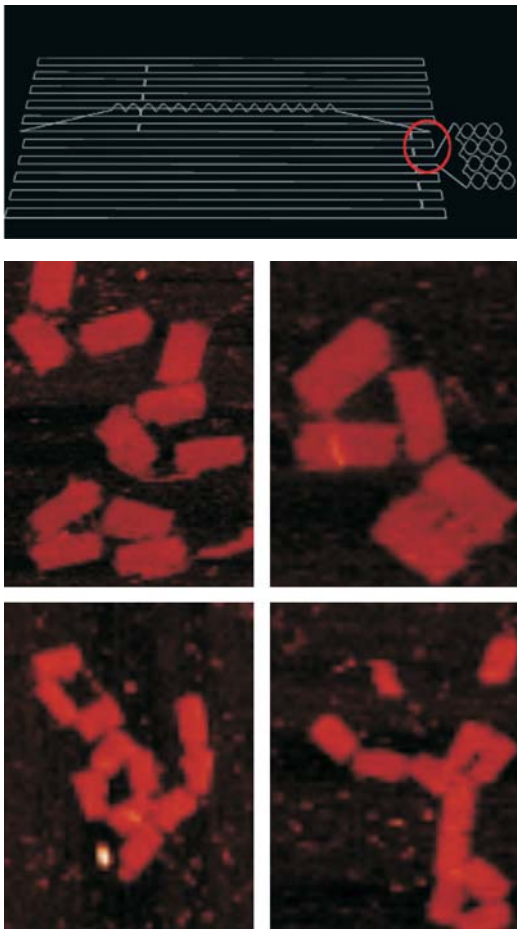


Figure 4. Assembly of bridged DNA origamis, a DNA single strand is kept unpaired to curve and bridge DNA origamis. Above scheme of the calculated structure. (courtesy JM Arbona, J. Elezgaray, JP Aimé.

Viruses are self-assembled materials with controlled arrangement at the molecular scale. Through genetic engineering, viruses provide functionalized arrangements of systems and devices. A known result is the genetically engineered M13 virus, which serves as a model system and is used as a programmable molecular building block to template inorganic materials' growth.

Combined top-down, in particular using microcontact printing technology, and bio-inspired bottom-up fabrication methods have been used to assemble nanowires, fabricate microbattery electrodes with viruses (A. Belcher) or microreactor design arrays to investigate biomolecular motor activity.

Synergie between Bio-Inspired methods and information

This fast-growing field and its mature bottom-up fabrication methods provide an almost infinite variety of bio-inspired materials and functions. Within this framework, there is a pressing need to face the challenges to design multi-scale structures with well-defined integration levels and to engineer interface properties from the molecular scale up to several micrometres.

Challenging complexity and providing concrete outcomes are at the heart of the bio-inspired fabrication method. Conception and fabrication of complex arrangements of functional materials and nanodevices is thought to be a key step towards overcoming Moore's Law. In biological systems, the same starting material has the potential to form an infinite variety of structures with dedicated functions.

Beyond achieving powerful 2D-3D bio-inspired structures, a key aim is to assemble and organise functional materials and systems at increasing levels of complexity. Designing multi-scale structures to create hierarchical order requires the cooperative development of new experimental tools that record information at different scales. The following key challenges are:

- identifying different integration levels used to process information in multi-scale structures
- theoretical modelling of equilibrium and non-

equilibrium interaction in different contexts, from molecular recognition to controlling the growth process

- a rationalized route for efficient strategies to engineer interface properties from the molecular scale up to several micrometres
- a rationalized route for instrumentation to record data at different scales

EU and outside

Definitely the Bio-inspired method is a fast growing research topic emerging principally in USA, Japan and Israel. Especially, in USA there is a wealth of creative and innovative results. Numerous functionalities emerge; dynamic patterning, elaborate 3D structures with controlled shape, precise positioning of inorganic materials and devices, control of nanoparticles arrangements... At the same time, there is an increasing efficiency in designing and fabricating short sequences with specific functions.

Several European groups are already involved in this research topic, see for instance the Danish group with the noticeable results: Dolphin and DNA Box, Oxford, Munich etc. Numerous European laboratories have developed high-throughput protocols for biomolecule selection, e.g., aptamers fabricated with the SELEX process or peptide sequences using phage and cell display methods, optimised for chemical or biological applications. Nucleic acid ligands and aptamers are characterized by high affinity and specificity for their target, a versatile combinatorial selection process and small physical size, which collectively make them attractive molecules for targeting diseases or as therapeutics. Aptamers were first conceived as a medical tool.

The other important field concerns nanostructure and nanodevice. Here again, the main interest lies in that the high affinity and specificity as well as their small size, make aptamer tools good candidates for handling interface properties. These properties will enable aptamers to facilitate innovative new nanotechnologies.

The recently EU funded COST Action "BioInspired nanotechnologies: from concepts to applications" aims to bring bio-inspired nanosystems and nanomaterials in the field of nanotechnology and to combine bio-inspired bottom up and top down fabrication methods by bridging multidisciplinary scientific fields and centres on DNA (DeoxyriboNucleic Acid) technology, affording the elaboration of programmable chemical synthesis routes to build complex architectures and functions with molecular precision, and shedding light on a new generation of robust tools.

Key challenges addressed are indentifying different integration levels used to process information in multi-scale structures, theoretical modelling of equilibrium and non-equilibrium interaction in different contexts, from molecular recognition to controlling the growth process, a rationalized route for efficient strategies to engineer interface properties from the molecular scale up to several micrometres and a rationalized route for instrumentation to record data at different scales.

3.5 Nanoelectromechanical Systems (NEMS)

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1. Introduction

Micro Electro Mechanical Systems (MEMS) have been studied and developed for more than 3 decades [1]. They bring together silicon-based microelectronics with micro-machining technology, making possible the realization of complete systems-on-a-chip. The fundamental and characteristic element on every MEMS is a mechanical (movable) component with dimensions ranging from few microns up to millimeters in some cases. These system shave been proven to be very useful for a plethora of different applications, e.g. ink-jet heads for printers [2], accelerometers for automotive applications [3], micromirrors for beam splitting [4], chemical sensors [5], etc. Following the evolution of microfabrication technologies for integrated circuits, pushing downwards the resolution limits, the dimensions of the mechanical components in MEMS were also reduced below 1 μm, yielding the first Nano Electro Mechanical Systems (NEMS) [6, 7]. This is the way NEMS appeared following the so-called "top-down approach". In parallel, the development of nanofabrication "bottom-up approaches", based on materials growth or self-assembly, has constituted another alternative to fabricate NEMS.

NEMS are characterized by small dimensions, which determine the devices functionality. However, it is sometimes difficult to decide if a given device can be defined as a NEMS or not. Therefore, we consider necessary to establish a definition for the term in this paper.

1.1 Definition

Nano Electro Mechanical System (NEMS) is a system:

- which involves electronic and mechanical elements
- whose main functionality is based on at least a mechanical degree of freedom
- whose size has the following characteristics:
  - at least two out of its three dimensions are below 1 μm OR
  - its functionality is given by a thin layer smaller than 10 nm
- which can include:
  - actuation
  - signal acquisition (sensing)
  - signal processing
  - vehicles for performing chemical, biochemical reactions and bioelectrical interactions

1.2. Interest

Since they first appeared in the literature [8, 9], several groups all around the world have been actively contributing in the field of NEMS. Besides the possibility of increased device density, the growing activity in the field has been mainly motivated by the benefits that these systems provide.

Among the interesting properties of NEMS, many can be explained using scaling laws. Let us consider a mechanical device and scale down its three dimensions:

thickness (t), width (w) and length (L). The effect of scaling on important parameters can be illustrated through simple formulas given in Table 1.

Mass	Elastic constant
$m = \rho V \propto l^3$	$k = \frac{\beta E w t^3}{L^3} \propto l$
Resonance frequency	
$\Delta F^2 = \int_{BW} S_F \, df \propto l$	
Force noise	
$S_F = \frac{2 k_B T k}{\pi Q f_{res}} \propto l^2, \quad constant\ Q$	
$f_{res} = \gamma \sqrt{\frac{E}{\rho}} \frac{t}{L^2} \propto l^{-1}$	

Table 1. Table summarizing how the properties of a mechanical system scale down with the reduction of its dimensions [10].

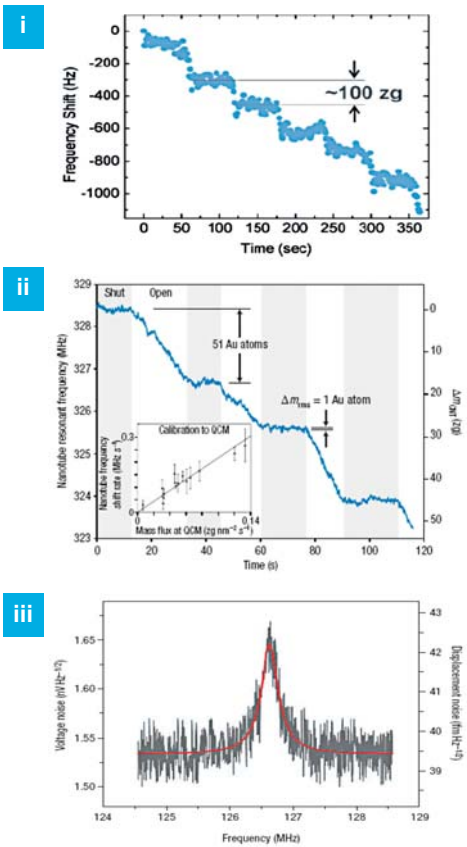
Therefore, NEMS offer [11] fundamental resonance frequencies in the microwaves [12], high mechanical quality factors [13], active masses in the femtograms (1 fg = 10^{-15}g) [14, 15], heat capacities below the yoctojoule (1 yJ = 10^{-24}J) [16, 17], ultra-low operating power level (for 1 device 1 pW = 10^{-12}W) [11], etc. All these properties make NEMS interesting for a series of different applications because they improve previous MEMS devices functionalities by orders of magnitude.

2. Applications

As it can be understood from the discussion above, the natural applications of NEMS can be mainly divided into three different groups: sensors, electronics (signal processing) and new tools for fundamental studies.

2.I. Sensors

Mass and force sensors have been the most studied because they allow the detection of different species after proper connection to chemistry/biology by means of proper functionalization. For mass sensing, the race has been pushing down the limits of detection passing through the attogram (1 ag = 10^{-18}g) [14, 18], the zeptogram (1 zg = 10^{-21}g) (Figure 1.i, [15]) and finally ending with the detection of a single individual atom using a carbon nanotube (CNT) (Figure 1.ii, [19]). From a more applied point of view, nanomechanical resonators have been used for (bio)chemical detection [20] and it has already been possible to detect a single virus [21]. However, one of the most promising applications is still under development and this is the "Single-Molecule Mass Spectrometry (NEMS-MS)" [11]. Regarding force sensing, the lower resolution limit attained by a NEMS up to date is within the femtonewton range at room temperature and atmospheric pressure (Figure 1.iii, [22]). However, the geometries that are proved to be more sensitive to force are much longer than standard NEMS [23, 24] and in some cases the search for higher measurement stability requires the systems to be much thicker [25-27]. Using those systems, a single base-mismatch in between two different DNA-strands of 18 bases has been detected [25] and also, as shown in Figure 1.iv [28], label-free detection of interferon-induced genes has been achieved.



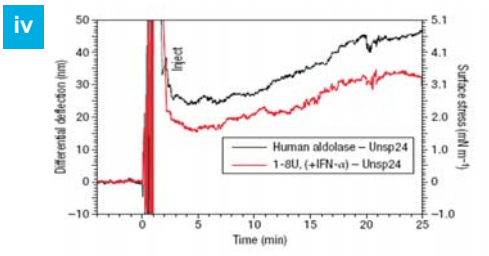


Figure 1. i) Resonance frequency shift of a nanosized free-standing beam while N_2 molecules are deposited on the structure in an "on/off" configuration. The device is operated at cryogenic temperatures. Each step in the data corresponds to approximately a 100 zg mass (2000 N_2 molecules). The root mean square frequency fluctuations of the system correspond to a mass resolution of 20 zg for the 1 s averaging time employed. Extracted from [15].

ii) Resonance frequency shift of a CNT-based nanomechanical resonator as a function of time while gold atoms are being deposited in an "on/off" configuration. The device is operated at room temperature, and presents a mass sensitivity of 1.3 • 10^{25} kg/$Hz^{1/2}$, i.e. 0.40 gold atoms • $Hz^{-1/2}$. Extracted from [19].

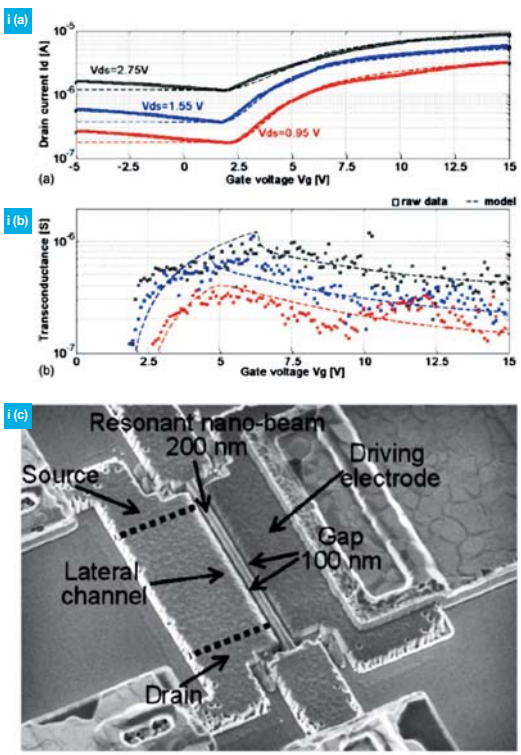
iii) Output voltage noise spectrum a 127 MHz self-sensing undriven cantilever measured at 1 atm and 300 K (black trace). A d.c. bias of 100 mV is used during the measurement. The red line is a Lorentzian fit to thermomechanical noise combined with uncorrelated white background noise. Off-resonance, the displacement sensitivity attained is 39 fm/$Hz^{1/2}$. Extracted from [22].

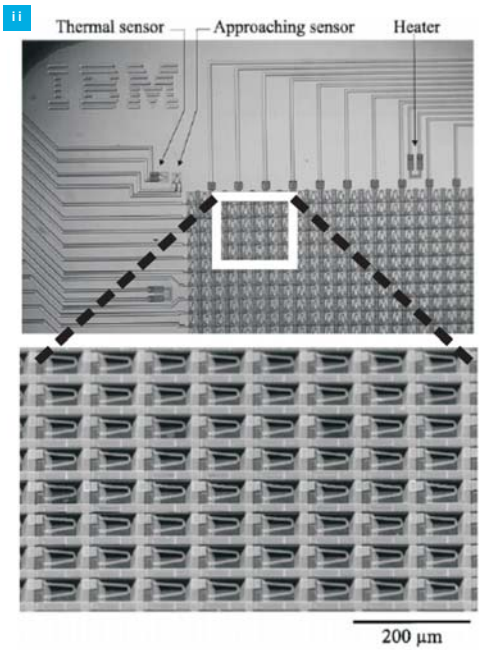
iv) Label-free gene fishing of an interferon-induced gene. The red line (ME15+) indicates the response of the cantilever coated with an interferon-a-sensitive human 1-8U gene fragment. The black line represents the differential mechanical response of the cantilever sensitized with the human aldolase A oligonucleotide. Extracted from [28].

2.2. Electronics

The trends in Integrated Circuits (IC) technology [29] can be divided into three groups: "More Moore" (referring to the continuous reduction of dimensions of MOS transistors with classical gate/source/drain architecture), "More than Moore" (including a series of additions to current and future CMOS technologies like Bulk Acoustic Resonators (BAR), Surface Acoustic Wave (SAW), metal contact switches, etc.) and "Beyond CMOS" that basically involves NEMS integration with CMOS.

The main advantage to include mechanical parts (both NEMS and MEMS) in circuits is on one hand, that the quality factors of mechanical oscillators are much higher than of electrical oscillators. This is highly demanded for filtering and communication applications [30, 31] and even more taking into account that they can be easily tuned [32, 33]. On the other hand, it is possible to build mechanical transistors and diodes [34] with a much lower power consumption when they are inactive [35]. When moving into the NEMS regime [36, 37] (Figure 2.i), the obvious advantage of a higher integration allows more density for the devices, their high frequencies increase the circuit speed and their ultra-low operating power reduce the power consumption when the devices are active. As a consequence, a reduction in power consumption keeping a fast behaviour is accomplished by integrating NEMS with CMOS.





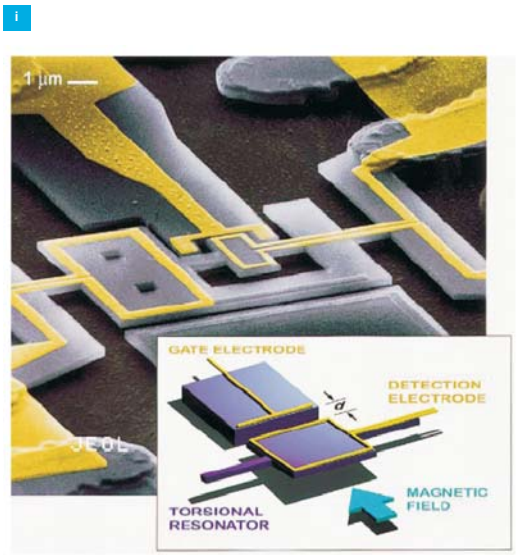


Figure 2. i) Fabrication and modeling of a lateral resonant gate FET (NEMS-FET). (a) I_D (V_G) characteristics and (b) transconductance g_M(V_D) of the transistor shown in a SEM micrograph in (c). Extracted from [37].
ii) Optical picture and SEM micrograph zoom of a micro fabricated 32x32=1024 2D cantilever array chip from IBM Zürich. It has been designed for ultrahigh-density, high-speed data storage applications using thermomechanical writing and readout in thin polymer film storage media. Extracted from [38].

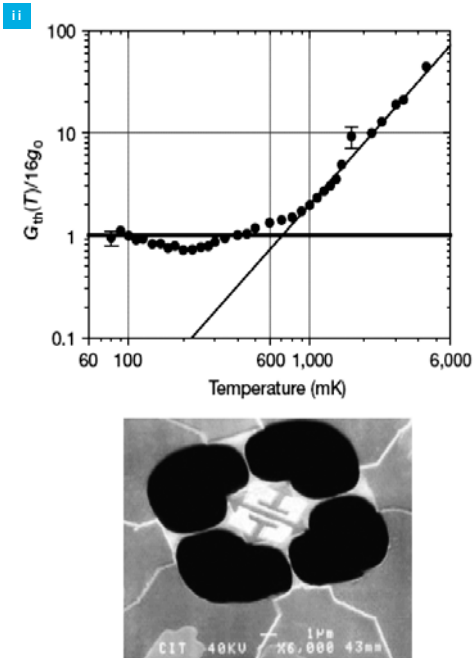


Figure 3. i) Nanometer-scale charge detector. The inset schematically depicts its principal components: torsional mechanical resonator, detection electrode, and gate electrode used to couple charge to the mechanical element. In this de-

A different approach is the one pursued by IBM within the Millipede project (Figure 2.ii, [38-42]) in which an array of small scanning probes is used to read and write bits of information from a substrate (data storage).

2.3. Fundamental studies

Another group of applications have a more fundamental origin. By their properties, NEMS constitute themselves new tools for scientific purposes. They can help in exploring scientific phenomena previously unobservable by other means. In particular, the fact that NEMS with given dimensions are mesoscopic systems could lead to the observation of quantum effects.

vice the fundamental resonance frequency of the structure is 2.61 MHz, with a quality factor measured to be Q=6500. A charge sensitivity of 0.1 e/Hz$^{1/2}$ is achieved, with a thermal noise limit of the order of 10^{-6} e/Hz$^{1/2}$ comparable with charge detection capabilities of cryogenic single-electron transistors, but responding at higher temperatures (>4.2 K) and over a larger bandwidth than other techniques. Extracted from [43].

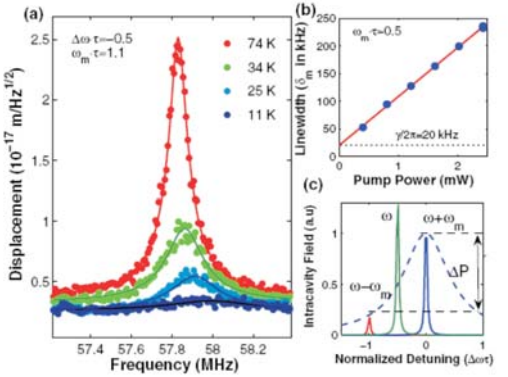
ii) Thermal conductance data for a fabricated mesoscopic phonon system consisting in a free-standing structure. A quantized limiting value for the thermal conductance, G_{th}, at very low temperatures is observed at 16 occupied modes, 16 g_0. For temperatures above T_{co}=0.8K, a cubic power-law behavior is observed, consistent with a mean free path of 0.9 μm. For temperatures below Tco, a saturation in Gth is observed at a value near the expected quantum of thermal conductance for phonon transport in a ballistic, one-dimensional channel: at low temperatures, G_{th} approaches a maximum value of $g_0 = \frac{\pi^2 k_B^2 T}{3h}$ *, the universal quantum of thermal conductance. Extracted from [17].*

Initially, NEMS were aimed as an instrument to determine the quantum for the electrical (Figure 3.i, [43]) and thermal conductance (Figure 3.ii, [17, 44-46]). Currently, quantum electromechanical systems (QEMS) are aimed [47-52] which could represent a new source of experiments and a number of applications that cannot be envisaged at the moment.

In the last years a quite complete theory on cavity optomechanics has been developed which has been accompanied by several experiments demonstrating cooling of resonators down to their ground level by dynamical backaction (Figure 4.i, [53-57]). An additional topic of extreme interest is the study of non-linear [58, 59] and/or complex systems [59-63], which can yield applications of localized energy modes [64, 65], as can be a selectivity increase [66, 67], or directly the oscillators synchronization (Figure 4.ii, [68]).

There are more examples on the use of NEMS as new tools for science: in [69], a specific type of NEMS mass sensor serves as transduction platform for the study of physical-chemical phenomena which are currently unobservable with any other tool. In [70], it is shown that Casimir forces, which are very difficult to observe experimentally, cannot be neglected anymore in very small NEMS and could be experimentally observed.

i



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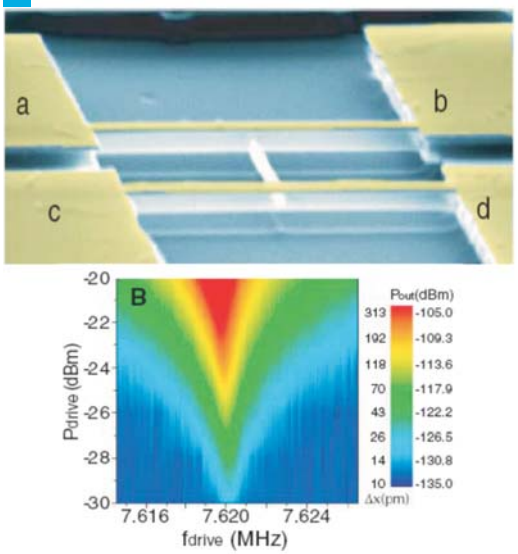

Figure 4. i) Cooling of a 58 MHz micromechanical resonator from room temperature to 11 K is demonstrated using cavity enhanced radiation pressure. (a) Normalized, measured noise spectra around the mechanical resonance frequency and varying power (0.25, 0.75, 1.25, and 1.75 mW). The effective temperatures were inferred using mechanical damping, with the lowest attained temperature being 11 K. (b) Increase in the linewidth (damping) of the 57.8 MHz mode as a function of launched power, exhibiting the expected linear behavior. (c) Physical origin of the observed cooling mechanism due to the asymmetry in the motional sidebands. Extracted from [56].

ii) SEM micrograph of the fabricated device (A) consisting in two parallel resonating beams whose movement is recorded by magnetomotive detection technique and an additional transversal beam coupling both oscillations. (B) Synchronization at subharmonic driving. A signal generator drives one beam (at frequencies close to $f_{res}/2$), and the response of the second beam is measured with a spectrum analyzer (at f_{res}). The contours represent the response in dBm. The synchronized regions become visible in the contour plots when the response exceeds the noise level of −136 dBm. One of the beams is driven at a frequency f0/n while the response of the second beam is recorded. This could be fundamentally important to neurocomputing with mechanical oscillator networks and nanomechanical signal processing for microwave communication. Extracted from [68].

3. Challenges

The wide range of applications and the huge interest of NEMS have been demonstrated up to now. However, together with the plethora of interesting properties, a multitude of questions and challenges arise and constitute hot topics in NEMS research.

3.I. High Quality factor

Achieving a high quality factor in a NEMS is of great importance because it means low energy dissipation, higher sensitivity to external forces, reduction of the minimum operating power level, etc.

The energy losses of a resonator have internal and external sources [71, 72]. The latter includes losses due to gas damping, clamping losses and coupling losses related to the transducing scheme. Air damping affects the vibration because the mechanical structure must displace some material in order to perform its movement. That is the reason why this contribution decreases when the pressure decreases [73]. In addition, a resonator can lose energy via acoustic coupling to its clamps [74], which can be minimized by engineering them, e.g. free-free beams present higher quality factors than clamped-clamped [75, 76] ones. The last contribution to the external losses can come from the transducers, so this contribution will be different depending on the read-out technique and it has to be studied individually as it has been done for magnetomotive detection [77] or for SET-based detection [78]. Internal losses can also be classified in two groups: losses generated in a perfect defectless crystal and losses due to impurities and/or defects in the bulk crystal lattice structure and in surfaces. Within the former group, Thermo Elastic Damping (TED) [79] and Akhiezer effect [80] are setting a top limit for the Q. Surface defects are shown to be much more important than bulk ones as suggested by the quality factor decrease when increasing the surface to volume ratio [11, 81]. In addition, experiments led in ultra high vacuum (UHV) have shown that surface oxides, defects and adsorbates increase energy dissipation but, on the opposite, annealing under UHV increased the Q in one order of magnitude [71, 82, 83].

More recently, however, Craighead's group has shown that it is possible to increase the quality factor of a doubly clamped beam by increasing the tensile stress of its material (Figure 5, [84, 85]), in this case silicon nitride. Moreover, silicon nitride has additional advantages such as chemical inertness (difficult to oxidize) and high robustness (difficult to break).

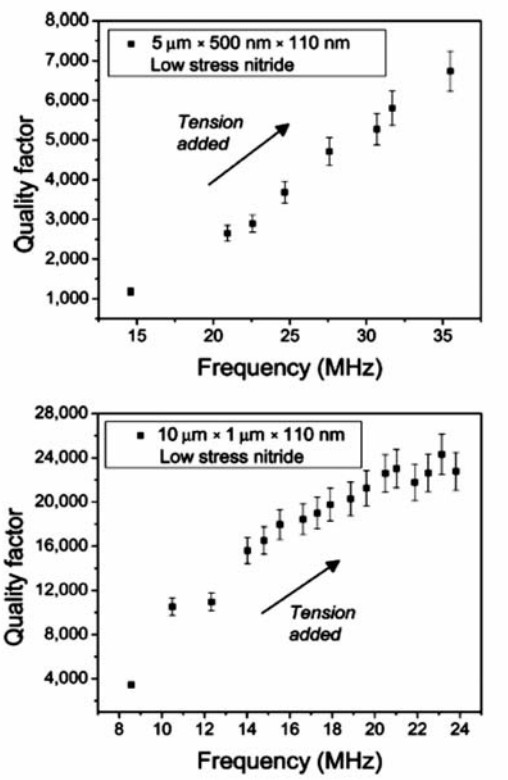

Figure 5. Results of added stress on low-stress silicon nitride beams. A 5μm x 500nm x 110nm device with initial f and Q of 14.6 MHz and 1200 respectively was stretched to an increased f and Q of 35.5 MHz and 6700. A 10μm x 1 μm x 110nm device, with an initial f and Q of 8.6 MHz and 3400, was stretched to an increased f and Q of 23.8 MHz and 23000. The arrows indicate the direction of the experiments in which stress was added to increase both frequency and quality factor. Extracted from [85].

3.2. Modeling

On the modeling side, the major issues involve multi-scale problems, inclusion of quantum effects and incorporating the electric environment on individual device models (i.e. circuit modeling). The first problem is exemplified by "sticking" which is anatomic scale phenomenon with a typical timescale in the femtosecond range (1 fs = 10^{-15}s): the typical operational time scale of a device is in the nanosecond range (1 ns = 10^{-9}s), and incorporating these two in a secure way is currently undoable from the point of view of simulation time. Even on a larger length scale, there are problems with the large fields in the small length scales: classical expressions such as $Q^2/2C$ are meaningless if C is too small. In addition, the basic theory and models only stand for simple beams or cantilevers. For more complex geometries, only Finite Element Modeling (FEM) is available.

Dissipation mechanisms, electro/mechanical modeling and circuit architecture modeling are also important issues that need to be addressed and solved.
Finally, it would also be interesting to incorporate quantum effects in device models (e.g. describing the coupling between two closely-located nanoscale objects simply through capacitances is certainly incorrect but the only way to do it currently).

3.3. Transduction in the nanoscale

Actuation and detection (transduction) are two of the major issues when considering a mechanical system. By transduction we refer to the conversion of one type of energy to another type, e.g. converting the mechanical energy of an oscillator into an electronic signal that can be interpreted by subsequent circuitry.

Transduction has already been a "hot spot" for MEMS technology and different techniques became popular, e.g. optical detection (laser beam deflection, interferometry...) and electrical detection (capacitive, piezoresistive, piezoelectric, gate effect...). However, when moving down to NEMS, the transduction techniques are not as efficient because of the size reduction [86]. The optimal transduction technique should present actuation and read-out that strongly interact with the mechanical element but with really weak couplings between each other, a large operation bandwidth and ultrahigh sensitivity [11].

Optical detection is affected by diffraction effects, which limit the smallest size of the mechanical device. Some authors have shown successful extension of Michelson or Fabry-Pérot interferometers into the NEMS domain [87], but the technique however is mainly convenient for NEMS-based force sensors (or surface stress) because their sizes are larger than the wavelength of the laser. On the other hand, optical actuation by means of photothermal effect or radiation pressure has been demonstrated [88-90], which makes this technique more interesting provided that a fully integrated scheme is accomplished.

A transduction scheme that behaves properly for NEMS, both for detection and actuation is the magnetomotive technique [77], which involves the application of an external magnetic field and an AC current through the mechanical device. Therefore a Lorentz force arises, which will drive the mechanical element and, in addition, generates an electromotive force in the circuit that can be transduced as a read-out voltage. Highly sensitive measurements with very low noise have been made using this technique, e.g. zeptogram detection [15], hydrogen detection [91] and modes synchronization [68]. However, there are major drawbacks for this technique: (i) it cannot be integrated and (ii) very low temperatures and very high magnetic fields are required.

Piezoresistive detection is affected by the reduction of the resistors dimensions, which implies a huge resistance, meaning high Johnson noise and high losses by nonmatching impedance. This issue is more important if we take into account that the piezoresistivity response of Si or Ge decreases with dopants concentration [92]. However, high resolution measurements have been performed using resonating piezoresistive structures with silicon resistors [23, 93]. It was at the beginning of 2007 when Roukes'group published some results which

meant a cornerstone for this type of detection [22], using metallic resistors with a very low piezoresistive coefficient as transducers. In this case they were overcoming the initial issue of a low sensitivity with an ultra low noise and proper matching impedance, finally yielding an unprecedented resolution for a NEMS operating at room temperature and atmospheric pressure. On the other hand, elec-trothermal actuation using small metallic resistors has also been demonstrated [94] up to several MHz (1 MHz = 10^6Hz) thanks to the small thermal mass of these devices.

However, this technique features a major drawback in the sense that the resulting power dissipation is high and locally elevates the temperature which can be problematic for mass sensing and other applications. In forthcoming years, very small structures may feature novel interesting properties that could result in improved transduction schemes [95], as it recently happened for Si nanowires (Si-NWs, below 200 nm diameter) and their newly discovered giant piezoresistive effect [96].

Capacitive transduction, which is really convenient for MEMS as it allows a simple two ports detection and actuation scheme, is really affected by the size reduction, mainly because the dynamical capacitance changes, i.e. changes in the capacitance due to the motion of the resonator, are very low (10^{-18}F) and therefore are obscured by parasitic capacitances, that are some orders of magnitude higher. Some specialized measurement techniques have been developed [13, 97-99] in order to cancel the effect of those parasitic capacitances. Some other solutions involve the use of geometries allowing high capacitive coupling but still preserving NEMS properties [100] or using the resonator not only as a capacitor's plate but also as, e.g. the gate of a MOS transistor [35, 37]. Monotlihic integration of capacitive NEMS with CMOS circuitry greatly enhances the detection efficiency [101,102].

Less effort has been devoted to piezoelectric transduction, but it has also been explored both for sensing and actuating NEMS. The read-out is based on the measurement of the polarization fields caused by the vibration of the lever. Those changes in polarization can be detected by working at the location where the variation is the largest as the gate of a transistor [103]. In addition, this technique can be used to drive resonators, as has been recently demonstrated [104] by Roukes group.

Apart from the aforementioned techniques, it is possible to find several other techniques that are less conventional but that have proven to be useful or interesting in some cases and whose potential in some cases is still unknown. Atomic Force Microscope has been used to detect the vibration amplitude of some systems with an unprecedented spatial resolution [105-108], although this is mainly limited to research samples. Detection of motion based on tunneling effect has also been used in many cases, in some cases pursuing monolithic integration [109] and in some other cases just seeking for the best transduction technique. This has been particularly successful in the case of CNTs, where a nanotube-radio has been built [110] and with which the detection of a single gold atom has been performed [19]. As for the actuation, an alternative technique could be Kelvin polarization force [111], which can be used on insulating materials, unlike electrostatic actuation.

3.4. Fabrication

As it has already been introduced, two different approaches can be chosen for NEMS fabrication, i.e. top-downand bottom-up. In the first case, there are three basic fabrication steps: the deposition of material (easy to go for thin layers down to 10-20 nm), the removal of material (by anisotropic Reactive Ion Etching, RIE, whose loss of lateral dimensions can be minimized down to the same amount of 10-20 nm) and the definition of the zones where the material is going to be deposited and/or removed. This last step is called lithography and the most standard isoptical UV. Due to diffraction effects and to other particular considerations of each mask aligner, the lateral resolution achieved using this technique can barely reach 1 μm.

Therefore, as soon as one of the lateral dimensions of the structure goes into the submicrometer range, complications arise because nano-lithographic processes are needed. These lithographic processes (see Figure 6) can be either serial (more flexible) or parallel (higher through-put). Different examples can be EBL [6, 7], Direct Laser Writing lithography [112], AFM lithography [113], etc. For the serial approach and DUV lithography [36, 37], NIL [114], nano-Stencil lithography [115], etc.,

for the parallel approach. Each of the lithographic processes mentioned present advantages and disadvantages which are discussed in detail here. However, if an eventual mass production is pursued, serial processes should be discarded.

In fact, the major challenge from the fabrication point of view is not the selection of the optimum lithographic process but the achievement of a reproducible and stable fabrication process with a fair control of the final mechanical properties of the fabricated devices. As an example of how difficult it can be to attain such reproducibility, one can take the example of the most controlled fabrication processes, i.e. CMOS circuitry fabrication. In this case, transistors and circuits are generally working in a digital mode and therefore two states only have to be distinguished (0 or 1), and consequently there is a relatively large tolerance with the individual properties of each transistor. On the other hand, a very small variation in the length of a cantilever, e.g. 5 %, would become a variation of the resonant frequency of a 10%, which might result unacceptable in some applications.

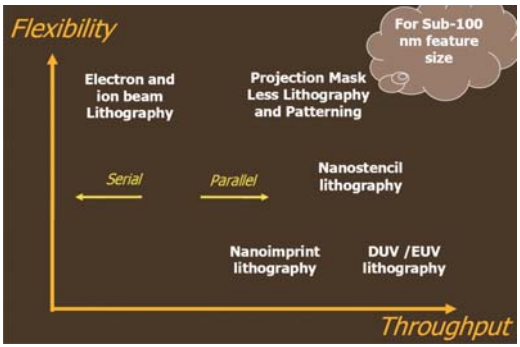

Figure 6. Scheme taken from [123] summarizing the different lithographic techniques for nano-patterning definition.

For the bottom up approach the aforementioned problems also apply in some cases, as for example the growth of nanowires or nanotubes out of catalytic nanoparticles whose size must be controlled prior to growth. However, the main problem still remains the integration of the nanostructures with connections to the macro-world or even circuitry. Two approaches are followed to accomplish this integration. The first one involves the deposition of the catalytic particles on a substrate where the circuits (or similar) are already present, the growth of the CNTs [116] or the NWs [117-119] being subsequently performed. The second one involves the growth of the nano-elements in a separate substrate and then, with the use of electrical fields, placing them in between two electrodes [120-122].

3.5. System Integration

Maybe the most important issue that NEMS are facing now and will be facing in the near future is how to turn these promising devices into effective, real systems. Most of the works we have referenced up to now can be considered as handcrafted and just facing the applications from a research point of view. There are still a lot of steps to overcome in order to make these 'stand-alone'resonators (with discrete electronics around them) evolve towards complete systems that can be produced in masse for an eventual commercialized application. Integration of NEMS with CMOS seems to be one of the most promising approaches. One approach can consist inusing CMOS steps to define the resonators and at the end finishing with a post-processing step to release the mechanical structures [36, 37, 124].

Industrial foundries are generally reluctant to this so-called In-IC approach since it can perturb the stability and the 'cleanliness' of the CMOS process. However, in a near future, this method could progressively become more applicable because of the increasing convergence between nano-transistors and NEMS in terms of size.

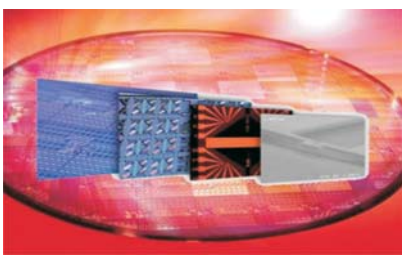

Figure 7. Picture of the first 200 mm wafer fabricated within the "Alliance for NEMS-VLSI" [125]. In one single wafer, 2.5 million NEMS are included, which represents more than the total amount of NEMS fabricated during the previous 15 years. The process consists in a 4 lithographic levels with a hybrid DUV and EBL approach and all the devices present thermoelectric actuation and piezoresistive detection [22, 94]. Extracted from [126].

The other approach consists in post-processing pre-fabricated CMOS substrates in order to fully define the mechanical structures [113, 115]: this solution can be useful to reduce fabrication costs if an advanced CMOS is not available or required.

Up to now, the biggest step for the integration of NEMS as a system has been achieved by the collaboration between LETI-CEA in France and the California Institute of Technology (Caltech) in the US [125, 126] which are directly aiming at the large integration of NEMS into a system (Figure 7).

4. Conclusions

We have shown that NEMS have unique and useful properties that make them suitable for a plethora of different applications in various fields, ranging from Information and Communication Technologies (ICT) until bio-chemical detection, including some applications that are not yet known but that for sure will emerge together with the development of these systems. They have the potential to become a revolution for the market in the same way that MEMS have caused an enormous impact during the last 20 years. However, there are some important issues to be solved before NEMS can have actual applicability, e.g. integration of the mechanical part with circuitry into a complete system, reduction of fabrication costs in order to make them competitive against existing sensors, etc.

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3.6 Semiconductor nanowires: Status of the field - research and applications

Introduction

List of experts / Contributors: With the core of this report based on the final publishable report from the EU/IST funded NODE-project, basically all 12 partners of this program have contributed in different ways. Most significant have been the over-all coordination by C. Thelander and L. Samuelson (Lund University) and the site leaders of the 12 partners: L-F. Feiner (Philips), W. Riess (IBM), G. Curatola (NXP), L. Ledebo (QuMat), W. Weber (NamLab, previously Qimonda), J. Eymery (CEA), U. Gösele (MPI), P. Vereecken (IMEC), L. P. Kouwenhoven (TU Delft), A. Forchel (Univ. Würzburg), A. Tredicucci (SNS-Pisa). Other people that have contributed are V. Zwiller (TU Delft), J-C Harmand and P. Caroff (LPN-CNRS), J. Johansson, C. Prinz, J. Tegenfeldt, K. Deppert and H. Linke (Lund Univ.). Many others have directly and indirectly contributed to this report.

Keywords: Nanowire, growth, processing, physics, characterization, devices, integration, energy, biology.

Institutions acronyms:
LU: Lund University; **PRE:** Philips Research Laboratory Eindhoven; **MPI:** Max-Planck-Institut; **IBM:** IBM Zurich; **WV:** University Wurzburg; **QM:** QuMat; **TUD:** Technical University of Delft; **NL:** NamLab, previously Qimonda; **IMEC:** Interuniversity Microelectronics Center; **SNS:** Scuola Normale Superiore di Pisa; **CEA:** Commissariat à l´Énergie Atomique; **CNRS/ IEMS:** Centre National de la Recherche Cientifique / Institut d´Electronique, de Microelectronique et de Nanotechnologie.

The field of semiconductor nanowires (NWs) has during the last five years developed very rapidly. Within the European frame-work the strongest efforts have been in the development of nanowire-based electronics, i.e. nanowire transistors, as performed in the largest Integrated Project within "Emerging Nanoelectronics", called "Nanowire-based One-Dimensional Electronics (NODE)". Considering the rather high maturity of the research field reached through NODE, we use the final publishable report as the core of this report. We also attach as an appendix a summary of impressions from the dissemination workshop that was organized at the conclusion of NODE, when the "NODE Workshop on Nanowire Electronics" was organized in Lund in September 2009. Here we also summarize the input and recommendations as provided by the invited experts: W. Hänsch (IBM), M. Passlack (TSMC), J. Knoch (TU Dortmund), T. Mikolajick (NAMLAB), H. de Man (IMEC), and L. Tilly (Ericsson).

Other central areas of nanowire research and applications deal with fundamental studies of nanowire growth, as very actively pursued through the arrangements of a series of four European Workshops on Growth on Nanowires, most recently the 4th arranged in Paris in October 2009. We include as an appendix a summary of the status as revealed from this workshop (written by J-C Harmand and F. Glas). Incorporated in this article is also a status of the field description provided by J. Johansson and P. Caroff.

In order to provide a more detailed description of the level of understanding and control of physical properties of nanowires, a special chapter has been provided for this by L. P. Kouwenhoven and V. Zwiller. This chapter also deals in more detail with the opportunities for opto-electronic devices based on NW technology.

Another important area of NW research relates to their application for Energy harvesting as implemented in solar cells and thermoelectrics. For the use of NWs in photovoltaics was recently started an EU-project cal-led AMON-RA. We enclose two short descriptions of Nanowires for energy, provided by K. Deppert.

An increasingly important aspect of nanowire research deals with their use in biology and in medical applications. We include here also a description of the state of the art as provided by C. Prinz and J. Tegenfeldt. For each of these areas we try to provide some of the key references but these are far from complete lists of references.

1. Overview of nanowire electronics[1]

The integrated project "NODE" developed and evaluated technologies for growth and processing of semiconductor nanowire devices for their possible impact as key add-on technologies to standard semiconductor fabrication. The partners in NODE worked on generating a deepened understanding of the physics phenomena of one-dimensional semiconductor materials and nanowire-based devices, and on developing new functionalities not found in traditional higher-dimensional device structures.

[1] Based on the NODE project executive summary

A set of key device families based on semiconductor nanowires were studied in detail; such as tunneling devices, and field-effect transistors. Also unique opportunities that may be offered by nanowires in different areas are explored, e.g. memory applications. NODE maked a dedicated effort to evaluate the potential for integration of nanowire-specific processing methods and to assess the compatibility with requirements from conventional semiconductor processing, as well as evaluating novel architectural device concepts and their implementation scenarios. This chapter is based on the NODE project executive summary. Detailed information about objectives and main achievements of the NODE project are available in Annex 2.

1.1. Nanowire growth

1.1.1. General growth control

Controlling the crystal structure of InAs nanowires (LU)
Gold-particle seeded nanowires fabricated in materials with zinc blende as the bulk crystal structure are often observed to have wurtzite crystal structure. The general trend is that thin wires are wurtzite and thick wires are

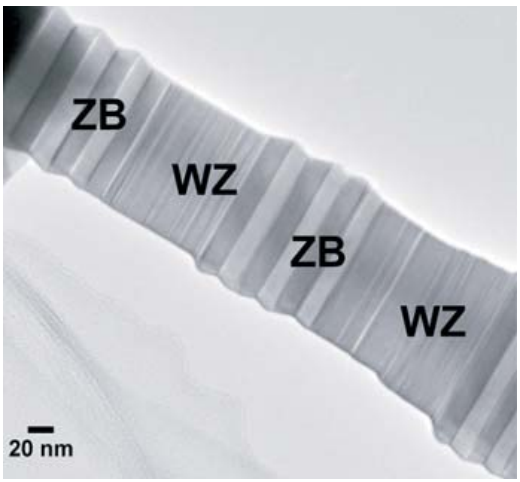

Figure 1. Polytypic superlattice, with alternating zinc blende and wurtzite structure, along an InAs nanowire.

zinc blende. That is, there is a cross-over diameter for the preferential polytype. This cross-over diameter is temperature dependent. By carefully varying the temperature during growth we were able to fabricate superlattices with alternating zinc blende and wurtzite structure. [1]

Crystal phase and twin superlattices (PRE)
The crystal phase of III-Vs NWs can be determined by the dopant precursor flows during growth. In InP the use of Zn-precursor favors the ZB phase, whereas the use of S-precursor favors the Wz phase. Moreover, highly regular twin superlattices can be induced in the ZB phase by tuning the Zn concentration, wire diameter and supersaturation. The effect was explained in a model based on surface energy arguments. [2]

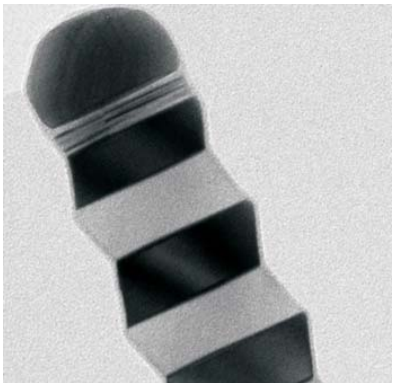

Figure 2. TEM image of the top part of an InP NW, closely below the Au catalyst particle, showing the highly regular twin superlattice structure.

Synergetic growth (PRE)
A counter-intuitive effect controlling the influence of wire spacing on growth rate was uncovered, synergetic

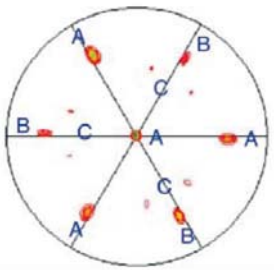

Figure 3. GaP wires next to a thick wire are taller than the second-nearest wires, which are taller than those in the middle of the field (furthest from the thick wire), showing that the growth rate of one wire is enhanced by the presence of another one and dependent on the catalytic alloy amount.

growth, which implies that at smaller spacing the competition for available material, reducing the growth rate, is counteracted by the increase in surface density of catalyst metal particles on neighboring nanowires, providing more decomposed material. [3]

I.I.2. Heterostructures

Epitaxial Ge/Si nanowires (MPI)
Epitaxial Ge/Si hetero-structure nanowires on Si (100) substrates were prepared in AAO templates. Usually, the Si atoms dissolved in the Au/Si eutectic catalyst act as a reservoir for Si, and the interface to Ge is smeared out. This new approach of the growth inside the AAO templates, allowed to produce a sharp interface of Ge/Si without changing the diameter of the nanowire. [4]

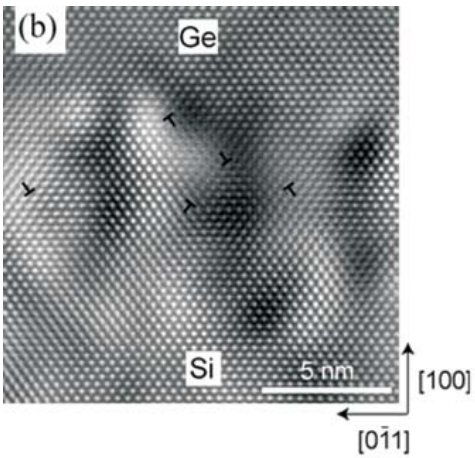

Figure 4. Cross-section TEM ima-ge of the Ge-Si interface.

Morphology of axial heterostructures (LU)
An extensive investigation of the epitaxial growth of Au-assisted axial heterostructure nanowires composed of group IV and III–V materials have been carried out and derived a model to explain the overall morphology of such wires. [5]

By analogy with 2D epitaxial growth, this model relates the wire morphology (i.e., whether it is kinked or straight) to the relationship of the interface energies between the two materials and the particle. This model suggests that, for any pair of materials, it should be easier to form a straight wire with one interface direction than the other, and this was demonstrated for the material combinations presented here.

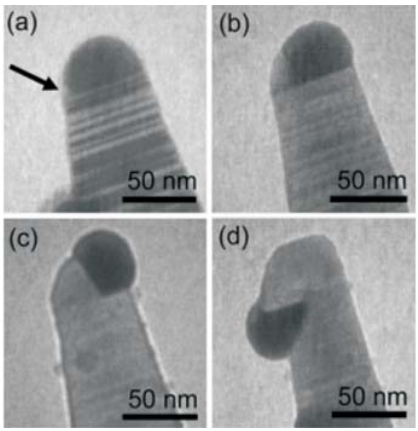

Figure 5. Images recorded during the growth of Ge on GaP nanowires by UHV-CVD.

I.I.3. Doping

Decoupling the radial from the axial growth rate by in situ etching (LU)
It was shown that in-situ etching can be used to decouple the axial from the radial nanowire growth mechanism, independent of other growth parameters. Thereby a wide range of growth parameters can be explored to improve the nanowire properties without concern of tapering or excess structural defects formed during radial growth. We used HCl as the etching agent during InP nanowire growth, and etched nanowires show improved crystal quality as compared to non etched and tapered NWs. These results will make way for devices relying on doping in axial structures, where any radial overgrowth would lead to short circuiting of a device.

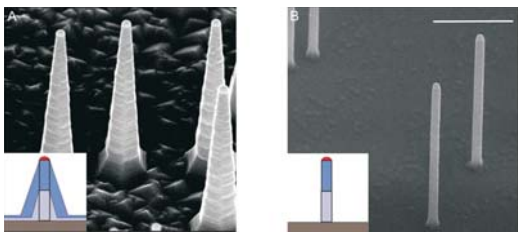

Figure 6. a) Tapered reference InP nanowires grown at a temperature of 450º C, b) Non tapered nanowires grown with HCl in the gas phase under otherwise identical growth conditions to a).

P-type doping and p-n junctions in InP NWs (PRE)
Sulphur was identified as a suitable candidate for n-type doping of InP in MOVPE using H_2S as a precursor. It was

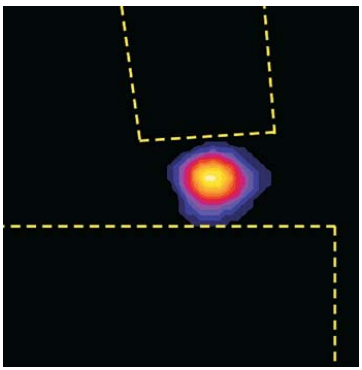

Figure 7. Optical microscope image of electroluminescent light coming from an InP NW LED, as collected by a CCD camera (the dashed lines show the positions of the electrodes).

further established that Zn-doping can be effectively used to achieve p-type doping in InP, using trimethylzinc as a precursor. The combination of S and Zn permits realization of p-n junctions in InP, showing good electrical diode characteristics in thin (20 nm-diameter) nanowires. The diodes exhibit LED behavior, testifying the high quality of the p-n junctions. [6]

Remote p-type doping of InAs NWs (PRE)
Obtaining quantitative control of doping levels in nanowires grown by the vapor-liquid-solid (VLS) mechanism is especially challenging for the case of p-type doping of InAs wires because of the Fermi level pinning around 0.1 eV above the conduction band. It was shown that growing a Zn-doped shell of InP epitaxially on a core InAs NW yields remote p-type doping: shielding with a p-doped InP shell compensates for the built-in potential and donates free holes to the InAs core. The effect of shielding critically depends on the thickness of the InP capping layer and the dopant concentration in the shell. [7]

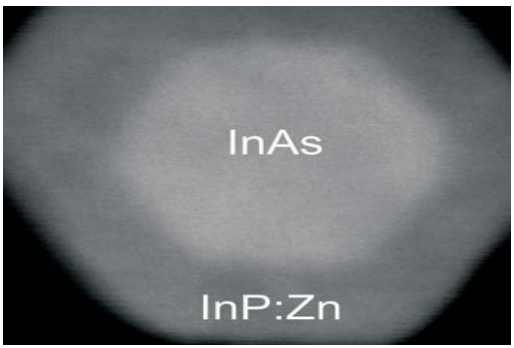

Figure 8. Dark-field TEM image of the InAs(core)/InP:Zn (shell) NW.

I.1.4. Si integration

Al as catalyst for Si nanowires (MPI)
Replacement of Au by other catalysts was one of the main efforts of this work. The metal Al was successfully used as a catalyst at low growth temperature in the VSS mode for growth of freestanding Si nanowires. The template-assisted growth using AAO and Al catalyst allowed to grow (100) oriented Si nanowires. [8]

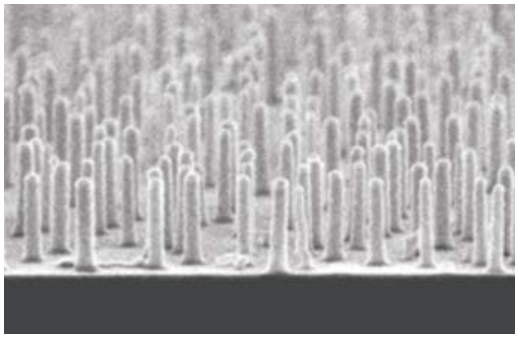

Figure 9. Si nanowires grown by use of a Al catalyst.

Epitaxial growth of III-V NWs on Si and Ge (PRE)
The growth of GaAs, GaP, InAs, and InP nanowires on Si and Ge substrates was investigated extensively , and high-quality epitaxial growth was demonstrated for these materials systems. It was shown that the orientation of the epitaxial nanowires depends on the substrate-wire lattice mismatch. [9]

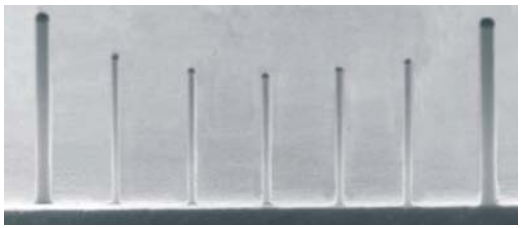

Figure 10. X-ray diffraction pole measurements on InP wires grown on Si(111), showing the presence of InP(111) reflections originating from the wires.

Au-free InAs nanowires on silicon (LU)
Narrow bandgap materials, such as InAs, could have great impact on future nano-electronics if integrated with Si, but integration has so far been hard to realize. InAs nanowires can be grown directly on silicon substrates using a method employing self-assembled organic coatings to create oxide-based growth templates. [10]

The method was subsequently modified to also allow for position-control, which is required for vertical device implementation.

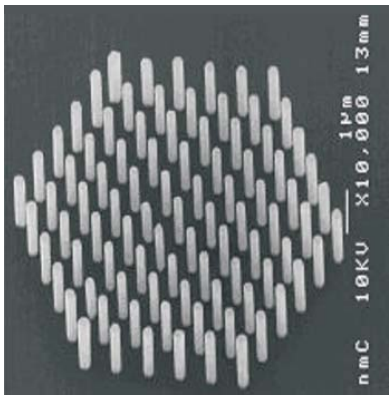

Figure 11. Epitaxial InAs nanowires grown on a Si(111) substrate from holes etched in a SiO_2 film.

1.2. Nanoprocessing

1.2.1. Surface passivation and gate dielectrics

Lateral nanowire n-MOSFETs (IBM)
Fully depleted lateral n-channel MOSFET devices were fabricated using implantation for source and drain regions. Strong inversion and clear saturation currents are observed in FETs from intrinsic NWs with p-implanted source/drain regions, whereas NWFETs with Schottky contacts only operate in accumulation mode. The effect of surface preparation on the electrical characteristics were studied and revealed that encapsulating the devices in a protective oxide yields significantly increased on currents and steeper sub-threshold swings. [11] This analysis reveals the strong influence of the electrostatics on the transport properties and shows that the extraction of device parameters using conventional models may not be valid.

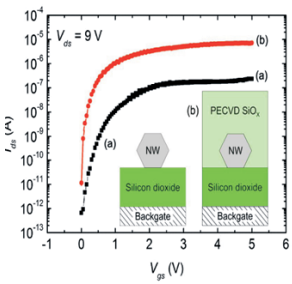

Figure 12. Transfer characteristic of a lateral nanowire n-MOSFET as fabricated surrounded by air (black) and encapsulated in SiO_2.

Chemical passivation of nanowires (WU)
The large surface to volume ratio of nanowires makes them very sensitive to surface effects such as nonradiative recombination centers or trapped charges. Surface passivation of GaAs nanowires by difference chemical treatments has been investigated and an improvement of the luminescence efficiency by a factor of 40 compared to as-grown wires could be achieved.

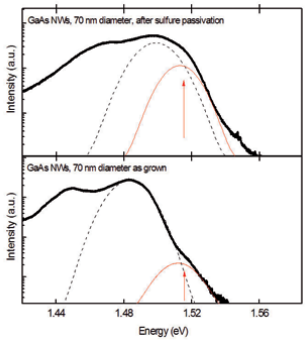

Figure 13. Photoluminescence spectrum of an as grown (bottom) and a passivated wire (top)

1.2.2. Contacts and gates for nanowire FETs

50 nm L_g Wrap Gate InAs MOSFET (QM)
Wrap Gated, or gate all around devices show the best control of the channel potential. InAs high-κ (HfO_2)

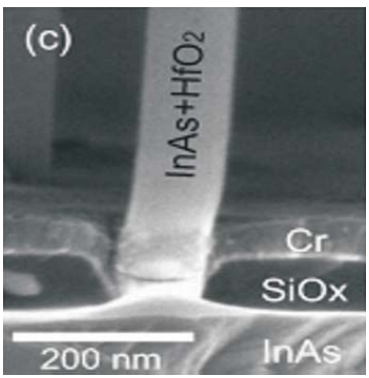

Figure 14. Cross section of the MOSFET, showing the 50 nm Cr gate around the InAs nanowire.

oxide nanowire field effect transistor, were successfully fabricated with a 50 nm long wrap gate. The first transistors were based on InAs wires grown on a n+ InAs substrate. The high mobility and injection velocity of the InAs channel leads to a good drive current and excellent transconductance. [12]

Schottky barrier FETs (IBM)

The use of thin Si_3N_4 interface layers between the silicon and metal contacts were shown to give Ohmic contacts whereas without the Si_3N_4 a normal Schottky contact was achieved. Furthermore, it was demonstrated that the Si_3N_4 interface layer gives Schottky barrier FETs with suppressed ambipolar behaviour due to a reduction in metal induced gap states. [13]

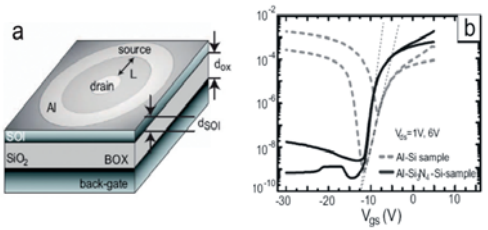

Figure 15. Schematic of a Schottky barrier pseudo-MOSFET and the corresponding transfer characteristics with and without an interface layer.

Multiple gates for nanowire devices (TUD)

Nanowires with multiple gates on horizontal nanowires have been developed to create electrical quantum dots in InAs/ InP nanowires. These devices are used to investigate quantum effects in coupled quantum dots nanowires. [14]

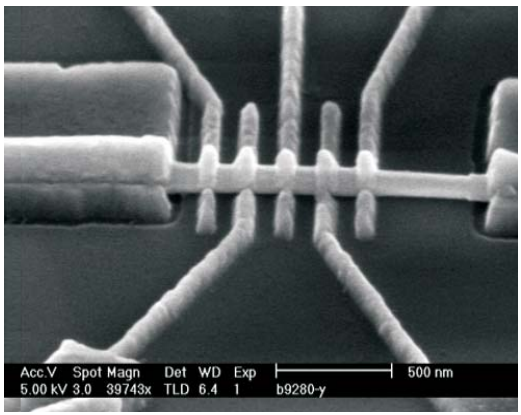

Figure 16. Horizontal InAs/InP nanowire with multiple gates.

Nanowire FET with gated Schottky contact (WU, NL)

Gated Schottky contacts allow a control over the polarity of the injected carriers, allowing to switch the operation of a nanowire FET from n-type to p-type. Such devices can be used to realize complementary logic without doping the nanowires.

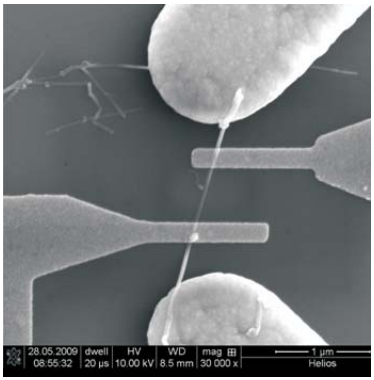

Figure 17. Si-nanowire FET with two gated Schottky contacts.

Wrap-around gate vertical Si nanowire Tunnel-FETs (IMEC)

The NODE project successfully developed a CMOS compatible process flow to fabricate vertical Si nanowire Tunnel-FETs using state-of-the-art processing tools onto 200mm wafers. An advanced gate stack using high-κ (HfO_2) oxide and metal gate (TiN) was implemented.

The top contact was obtained by isotropic dry etch of the gate stack at the top of the wire using a gate

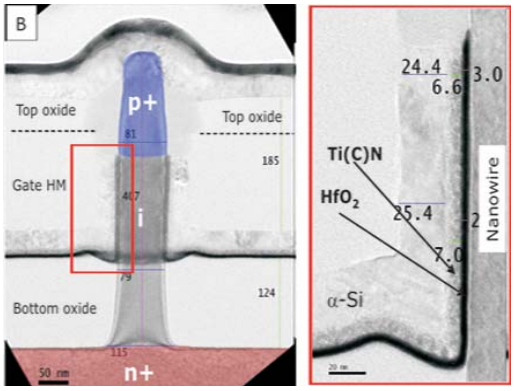

Figure 18. Cross section of the vertical TFET featuring 3nm HfO_2, 7nm TiN and 25nm a-Si gate stack around the nanowires.

hardmask. The gate is isolated from the substrate by a thick oxide layer. It is also isolated from the top contact by a nitride spacer and oxide layer. A capping layer connects multiple wires together. Top contact doping is achieved through epitaxial layer or tilted implants.

1.2.3. Processing of vertical nanowire devices

InAs Wrap Gated MOSFETs for RF and circuit applications (QM/LU)

For RF and circuit applications, the transistors need to be integrated on an highly resistive, or insulating substrate. Technology for growing, and locally contacting InAs nanowires on a semi insulating InP substrate has been developed.

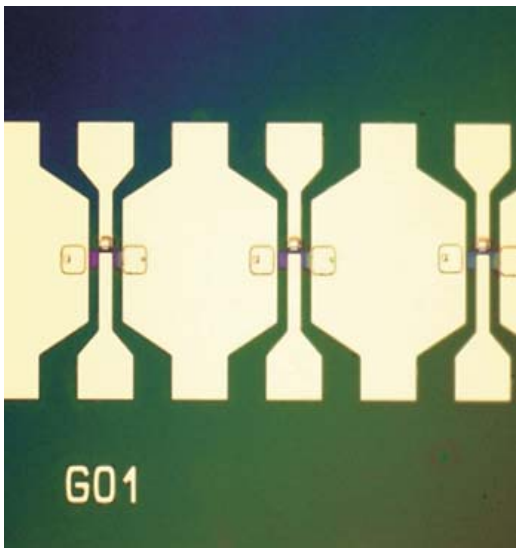

Figure 19. Top view of a fully processed RF-compatible vertical nanowire transistor structure.

The technology is based on a local ohmic substrate contact, which wraps around the base of the nanowires. This allows for RF characterization of the InAs MOSFETs, with first results of f_t=7 GHz and f_{max}=22 GHz. [15]

Vertical Impact Ionization MOS FETs (IBM-ZRL)

A process for vertical silicon nanowire FETs was developed. Using this process vertical impact ionization FETs with sub-threshold swings down to 5 mV/dec. were demonstrated. [16]

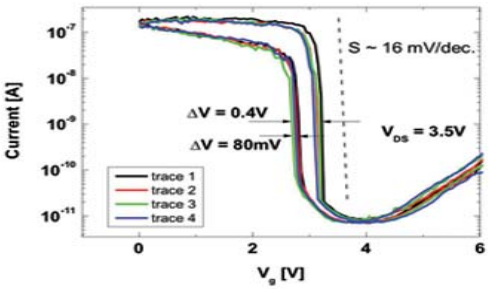

Figure 20. Stability of the transfer characteristics of a vertical IMOS FET.

Nanowires based spin memory (TUD)

The NODE project created a spin memory in a single quantum dot embedded in an InP nanowire. The preparation of a given spin state by tuning excitation polarization or excitation energy demonstrated the potential of this system to form a quantum interface between photons and electrons.

For this purpose, transparent contacts on vertical nanowires have been developed for FET devices and are currently under investigation. [17]

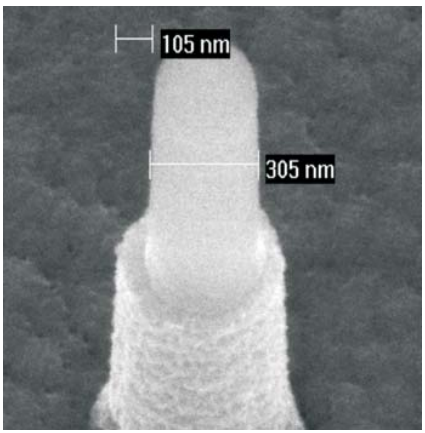

Figure 21. Vertical nanowire surrounded by a dielectric and a wrap gate.

SiO_2 template development for catalyst-free nanowire growth (IMEC)

A process was developed to fabricate hole patterns on top of silicon for constrained growth of Si nanowires, without the use of catalyst. The template was prepared by patterning a plasma–enhanced chemical-vapor deposited (PE CVD) Si_3N_4/SiO_2 25nm/300nm film

stack with openings or holes to expose the underlying Si. The patterning was performed through 193nm lithography and etching of the SiO_2 with Motif®, an advanced dry etch technique capable of shrinking printed feature sizes thanks to the deposition of a polymeric coating on top of the developed resist. Particular care was dedicated to cleaning of the side walls and the silicon bottom substrate to avoid defects creation during subsequent growth. To achieve suitable Si purity for epitaxial growth, a special sequence of process steps was needed to avoid Si contamination by carbon residues from etch.

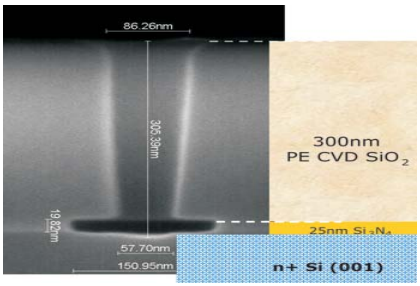

Figure 22. Cross-section of a via hole after plasma etch and hot phosphor opening of the Si_3N_4 bottom layer.

1.3. Physics and characterization

1.3.1. Electrical properties

Room temperature transport (SNS)

Room temperature transport properties of bare InAs and InAs/InP core shell nanowires [18] have been studied and a three dimensional electrostatic model was developed to compute the NW FET capacitance for a more accurate mobility determination. The measured values ranged in the 1-2 thousand cm^2/Vs for the thinnest wires (< 40 nm), while reached about 3 thousand for thicker wires. Remarkably all the wires showed relatively low values of electronic charge in the few $10^{16}cm^{-3}$ range.

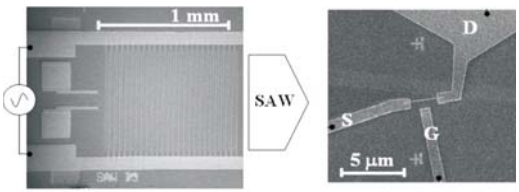

Figure 23. Sketch of the device and set-up for the induction of acoustoelectric current in NW FETs.

The highly Se-doped wires revealed an attendant strong increase in charge density up to ~ $1x10^{19}cm^{-3}$; as expected the impurities introduced brought along a decrease in the mobility, which varied in the 4-6 hundred cm^2/Vs range for wire diameters of 40-50 nm. In parallel, NW devices were fabricated for charge pumping through surface acoustic waves (SAW) [19]. The NW FETs were implemented on top a $LiNbO_3$ substrate with piezoelectric transducers. An acoustoelectric current peak in the wire was identified when driving the transducer near its resonance frequency. This type of devices is quite interesting both for analog signal processing and for the implementation of single-photon sources under quantized charge pumping. Furthermore, it yields a new direct method to measure the carrier mobility by observing the bias point at which the acoustoelectric peak in the current changes of sign, signaling that drift and acoustic wave velocity are the same.

Diameter dependence of tapered InAs nanowires [20] (TUD, PRE)

Electrical conductance through InAs nanowires is relevant for electronic applications as well as for fundamental quantum experiments. Nominally undoped, slightly tapered InAs nanowires were used to study the diameter dependence of their conductance.

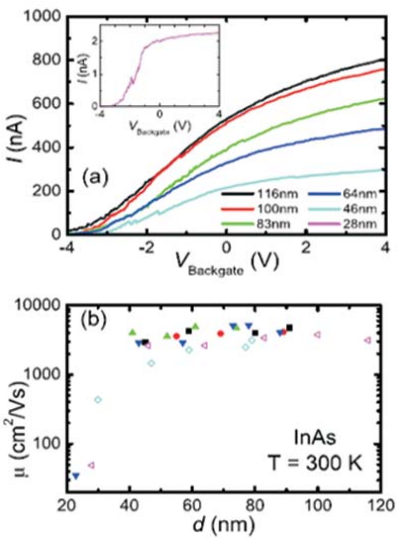

Figure 24. (a) the backgate sweeps for different sections within the same nanowire. The inset shows the data for the section with the smallest diameter. (b) the mobility determined from backgate sweeps. Different symbols correspond to the different devices studied.

Contacting multiple sections of each wire, we can study the diameter dependence within individual wires without the need to compare different nanowire batches. At room temperature we find a diameter-independent conductivity for diameters larger than 40nm, indicative of three-dimensional diffusive transport. For smaller diameters, the resistance increases considerably, in coincidence with a strong suppression of the mobility. From an analysis of the effective charge carrier density, we find indications for a surface accumulation layer.

Surface passivation of InAs nanowires by an ultrathin InP shell [21] (TUD, PRE)

We report the growth and characterization of InAs nanowires capped with a 0.5-1nm epitaxial InP shell. The low temperature field-effect mobility is increased by a factor 2-5 compared to bare InAs nanowires. The highest low temperature peak electron mobilities obtained for nanowires to this date, exceeding 20 000 cm^2/Vs we also reported. The electron density in the nanowires, determined at zero gate voltage, is reduced by an order of magnitude compared to uncapped InAs nanowires. For smaller diameter nanowires, an increase in electron density was found which can be related to the presence of an accumulation layer at the InAs/InP interface. However, compared to the surface accumulation layer in uncapped InAs, this electron density is much reduced.

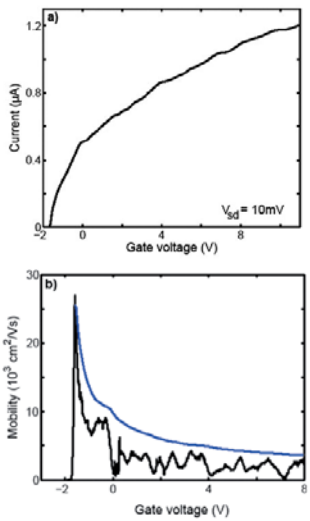

Figure 25. (a) pinch-off curve and (b) extracted field-effect (black) and effective mobilities (blue) of a high mobility core/shell nanowire.

We suggest that the increase in the observed field-effect mobility can be attributed to an increase of conduction through the inner part of the nanowire and a reduction of the contribution of electrons from the low mobility accumulation layer. Furthermore it was found that by growing an InP shell around an InAs core, surface roughness scattering and ionized impurity scattering in the accumulation layer is reduced.

1.3.2. Optical studies

Raman and mid-IR spectroscopy (SNS)

A micro-Raman set-up was developed and applied to InAs/InP core-shell structure, as a way to study the strain introduced in the structure and verify the reduced impact of surface states in the capped wires. A clear line width reduction was observed in wires with thick InP shells where less interaction with the surface was expected and a blue shift of the resonances with increasing shell thickness was also detected, which gives indication of the amount of strain in the InAs material.

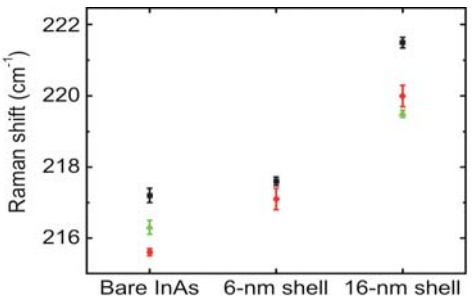

Figure 26. Energy position of the main transverse mode for NWs with different InP shells. Colours are used to distinguish among different wires in the same sample.

Micro photoluminescence studies of single InP nanowires (WU)

The optical study of single nanowires provides important information about physical properties such as size quantization effects. Individual NWs show narrow emission lines with linewidths as low as 2.3 meV which reflects the high structural quality of the nanowires. Blueshifts of the NW emission energy between 25 and 56 meV with respect to bulk InP are related to radial carrier confinement in nanowires with diameters between 15 nm and 50 nm. Time resolved investigations reveal a low surface recombination velocity of 6×10^2 cm/s. [22]

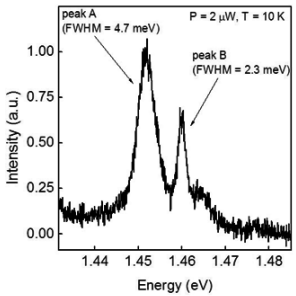

Figure 27. Micro photoluminescence spectrum showing emission from two InP nanowires with narrow linewidths of 4.7 meV and 2.3 meV, respectively.

Study of surface capping of InP nanowires (WU, LU, QM)

Time resolved photo-luminescence spectroscopy was applied to optimize the atomic layer deposition (ALD) of high-κ dielectrics (HfO_2, Al_2O_3) onto InP NWs – a process which typically leads to detrimental surface states. Applying a core/shell growth technique the InP surface quality could be significantly improved in terms of the surface recombination velocity S0 which was reduced to S0 = 9.0×10^3 cm/s in comparison with S0 = 1.5×10^4 cm/s obtained for an untreated reference sample without surface treatment prior to ALD.

In an alternative approach, in-situ post-growth annealing in H_2S atmosphere prior to ALD resulted in a nearly fourfold decrease of S_0. These results clearly show the importance of a proper surface treatment prior to oxide capping of III/V NWs for transistor applications.

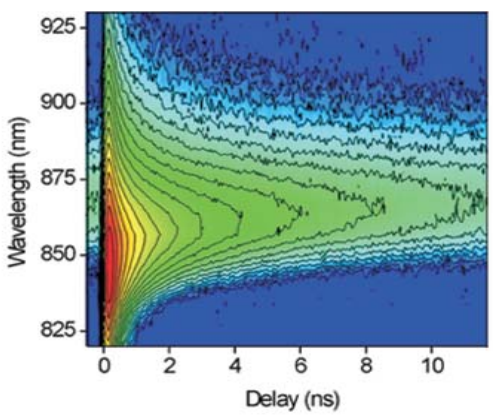

Figure 28. Spectrally and temporally resolved intensity map of the PL emission from HfO_2 capped InP NWs.

I.3.3. X-ray characterization

Study of radial and longitudinal heterostructures (CEA, LU, QuMat)

Quantitative structural information about epitaxial arrays of VLS-NWs have been reported for a InAs/InP longitudinal [23] and core-shell [24] heterostructure grown InAs (111)B substrates. Grazing incidence X-ray diffraction allows the separation of the nanowire contribution from the substrate overgrowth and gives averaged information about crystallographic phases, stacking defects, epitaxial relationships with orientation distributions, and strain. The strain profiles have been compared to atomistic and finite element calculations performed at CEA, and Grazing Incidence Small Angles Scattering has been used to extract the shape, diameter and variability of the NWs.

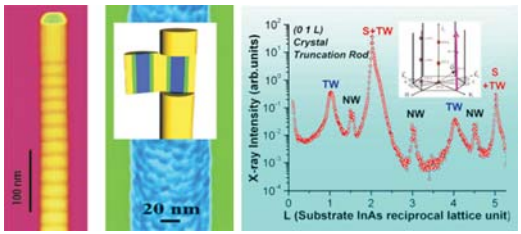

Figure 29. Longitudinal and radial heterostructures measured by Grazing Incidence X-ray Techniques and example of a truncation rod measurement showing the [111] stacking in a longitudinal InAs/InP heterostructure.

Single object studies (CEA)

The measurement of single NWs with coherent imaging techniques has been developed. This new technique gains insights into the shape of the objects [25], but also into the strain distribution inside one object. Original structural results obtained on sSOI lines with micro-

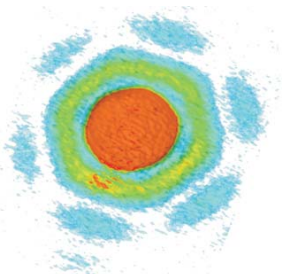

Figure 30. Coherent diffraction of single 95 nm Si nanowire (111) Bragg reflection. The "ab initio" analysis of this pattern allows reconstructing the shape of the NW.

focussed beams have been obtained (unpublished results) as well as the application of this technique to VLS grown samples.

1.3.4. Modelling

Band structure calculations (CEA, LU).
The band structure of group IV and various III-V NWs has actually been investigated in the whole 2-40 nm diameter range. The size dependence of the bandgap energy, subband splittings and effective masses has been discussed in detail [26] and used in collaboration with Lund for the modelling of InAs NW field-effect transistors. [27] Finally, the CEA has investigated the effects of strains on the electronic properties of III-V nanowire heterostructures (e.g., the reduction of the barrier height in tunnel devices). [28]

Transport properties (CEA)
The transport properties of ultimate silicon nanowires with diameters <6 nm has been modeled using quantum Kubo-Greenwood and Green function methods. The impact of surface roughness [29] and dopant impurities on the mobility has been studied. The CEA has shown, in particular, that the impurity-limited contribution to the mobility could be larger in wrap-gate nanowires than in bulk due to the efficient screening of ionized impurities by the gate. Also, the resistance of single impurities can be very dependent on their radial position in the nanowire, leading to significant variability in ultimate devices.

Effect of dielectric environment on the electrical properties (CEA, CNRS/IEMN, LU)
It was shown that the dielectric confinement can be responsible for a significant decrease of the doping efficiency in nanowires. [30] Dopant impurities are progressively "unscreened" by image charge effects when reducing wire diameter, which leads to an increase of their binding energies and decrease of their activity. These predictions have been confirmed by recent experiments by the IBM group. The binding energies of shallow impurities are however very sensitive to the dielectric environment of the nanowires, and can be decreased by embedding the wires in high-κ oxides or wrap-gates. Modelling has confirmed that many electronic properties of semiconductor nanowires are driven more by dielectric than quantum confinement, even in the sub 10 nm range, showing the importance of the "electrostatic" engineering of nanowire devices.

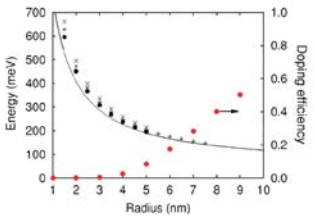

Figure 31. Binding energy of various donors (black symbols, left axis) as a function of the radius R of silicon NWs in vacuum, and room temperature doping efficiency of P donors (red symbols, right axis). The doping efficiency rapidly decreases below R = 10 nm.

1.4. Nanowire devices

1.4.1. InAs FETs

Vertical InAs transistors (LU/QM)
Fabrication of vertical InAs nanowire wrap-gate field-effect transistor arrays with a gate length of 50 nm has been developed. [31] The wrap gate is defined by evaporation of 50-nm Cr onto a 10-nm-thick HfO_2 gate dielectric, where the gate is also separated from the source contact with a 100-nm SiO_X spacer layer. For a drain voltage of 0.5 V, a normalized transconductance of 0.5 S/mm, a subthreshold slope around 90 mV/dec., and a threshold voltage just above 0 V were observed.

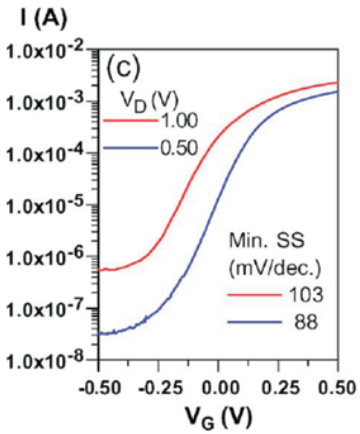

Figure 32. Sub-threshold I-V characteristics of an array of 55 vertical InAs nanowires.

RF characterization of vertical InAs transistors (LU/ QM)

Lund and Qimonda have developed an RF compatible vertical InAs nanowire process, with InAs wires grown on S.I. InP substrates. By combining 70 wires in parallel in a 50Ω waveguide pad geometry, S-parameters (50MHz-20 GHz) for vertical InAs nanowire MOSFETs were measured. A maximum f_t of 7GHz and f_{max}=22GHz [32] was obtained. Small signal modelling allowed for the first extraction of intrinsic device elements forming a hybrid-π equivalent circuit.

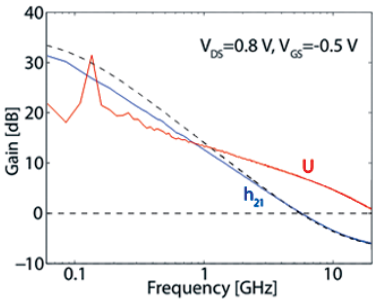

Figure 33. Measured and modelled RF gains for a 90 nm gate length InAs MOSFET.

1.4.2. Other InAs- and III/V-based devices

Nanowire-based multiple quantum dot memory (LU)

We demonstrate an alternative memory concept in which a storage island is connected to a nanowire containing a stack of nine InAs quantum dots, each separated by thin InP tunnel barriers. [33] Transport through the quantum dot structure is suppressed for a particular biasing window due to misalignment of the energy levels. This leads to hysteresis in the charging & discharging of the storage island.

The memory operates for temperatures up to around 150 K and has write times down to at least 15 ns. A comparison is made to a nanowire memory based on a single, thick InP barrier.

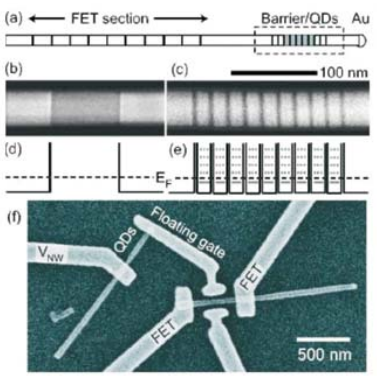

Figure 34. Design and implementation of a multiple quantum dot memory based on nanowires.

Nanowire capacitors (LU)

Vertical InAs nanowire capacitors have been developed based on arrays of nanowires, high-k deposition, and metal deposition. [34] The capacitors show a large modulation of the capacitance with the gate bias, and a limited hysteresis at 0.5 V voltage swing. Via modeling of the charge distribution in the nanowires as a function of the applied voltage, the regions of accumulation, depletion, and inversion have been identified. Finally, the carrier concentration has been determined.

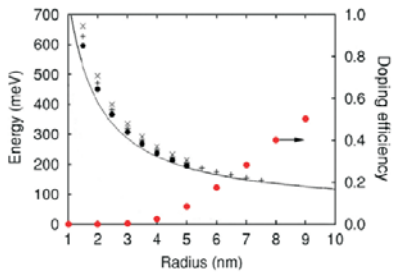

Figure 35. Measured CV profile at 20 MHz.

1.4.3. Si FETs

Doping limits in silicon nanowires (IBM)

The control over doping levels was demonstrated for in-situ doped silicon nanowires using phosphine as the

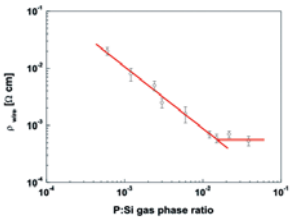

Figure 36. Experimental data of nanowire resistivity vs phosphine concentration. Donor densities up to the solid solubility limit of phosphorous in silicon was achieved.

doping source. It was found that the maximum attainable doping is $1\times10^{20}cm^{-3}$ limited by the solid solubility limit of phosphorous in silicon at the growth temperature ($450^{0}C$). [35]

Doping deactivation (IBM)

It was demonstrated experimentally that dopants inside scaled semiconductors experience a smaller screening as a function of decreasing size leading to a deactivation of the dopants. This effect is caused by a dielectric mismatch between the semiconductor and the surrounding medium. [36]

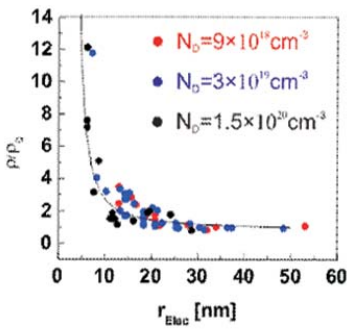

Figure 37. How the resistivity of silicon nanowires increases with decreasing diameter due to doping deactivation caused by a dielectric mismatch between the nanowire core and the surroundings.

Silicon nanowire tunnel FETs (IBM)

Tunnel FETs based on silicon nanowires were demonstrated for the first time. The FET structure was grown by the VLS method and doping was incorporated in-situ. The devices were fabricated in a lateral fashion with both a top and bottom gate. The data obtained on the FETs matched the expected sub-threshold slopes as modeled by a simple WKB approximation. [37]

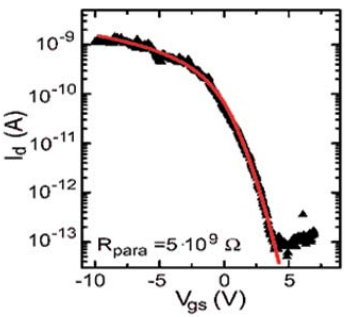

Figure 38. Transfer characteristics of a Si NW tunnel FET with top gate. The red line is calculated using the WKB approximation.

State-of-the-art all-silicon tunnel FETs (IBM)

All-silicon nanowire tunnel FETs with high on-currents were demonstrated. The use of a high-k gate dielectric markedly improves the TFET performance in terms of average slope SS (SS measured between $10^{-7}\mu A/\mu m$ and $10^{-3}\mu A/\mu m$ is 120mV/ dec.) and on-current, I_{on} ($0.3\mu A/\mu m$). The performance of the devices is close to what can be expected from all-silicon tunnel FETs. [38]

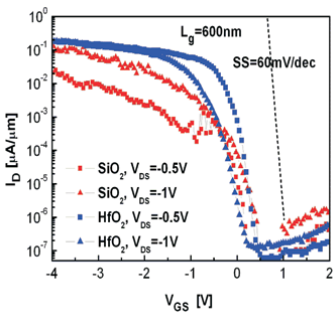

Figure 39. Transfer characteristics of silicon nanowire tunnel FETs with SiO_2 (red) and HfO_2 (blue) gate dielectrics.

Dopant-free polarity control of Si nanowire Schottky FETs (NL)

The accurate and reproducible adjustment of the charge carrier concentration in nanometer-scale semiconductors is challenging. As an alternative to transistors containing doping profiles, dopant-free nanowire transistors have been devised. The source and drain regions are replaced by metal contacts that exhibit a sharp interface to the active region. The current flow is controlled by locally adjusting the electric field at the metal/silicon interface. Independent control of each contact results in transistors that can operate either as p- or n-type. [39]

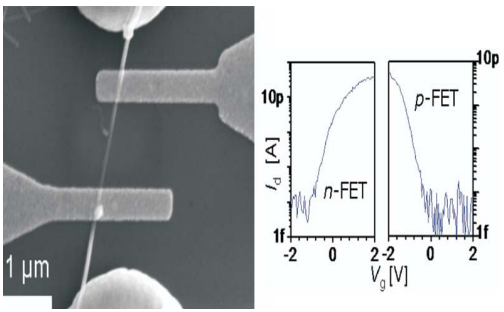

Figure 40. Silicon nanowire FET with two independent top gates, each coupling to a metal/semiconductor junction. The FET can be programmed as p- and n- type.

Complementary logic circuits built from undoped Si nanowire Schottky FETs (NL)
To reduce the static power consumption of digital circuits complementary logic is required. This is enabled by the interconnection between p- and n- type transistors. Complementary nanowire based inverter circuits that do not require doping were developed and characterized. The results show that all logic functions can be performed at low power consumption without dopants. The entire thermal budget for processing is kept below 400°C, enabling a possible future replacement of low mobility organic printed circuits on flexible electronics.

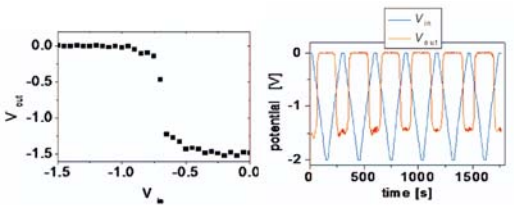

Figure 41. Silicon nanowire inverter characteristics; top: transfer characteristics, bottom: time resolved response.

I.5. Benchmarking and integration

I.5.I. Process upscaling of nanowire growth and devices

Wafer-scale nanowire growth (IMEC)
At first, catalyst-based growth of silicon vertical nanowire using none-gold catalyst systems was considered. Aluminum, which had been shown promising on coupon level tests (UHV-CVD at MPI), proved not up-scalable in the absence of UHV conditions. Indium particles did produce high-yield Si nanowires in PE-CVD but the growth was difficult to control. In view of the many limitations related to Vapor-Solid Liquid growth of silicon nanowires, a seedless (catalyst-free) constrained approach for growing Si and SiGe nanowires onto Si (100) substrates was developed. The growth approach takes advantage of the advances in Selective Epitaxial Growth (SEG) technology to fill the holes without the presence of catalytic metal particles. Nanowires with an intrinsic Si segment (channel) and p+ -doped (B) segment of either Si, $Si_{0.85}Ge_{0.15}$ or $Si_{0.75}Ge_{0.25}$ (source) were successfully grown on top of n+-doped (100) substrates. [40]

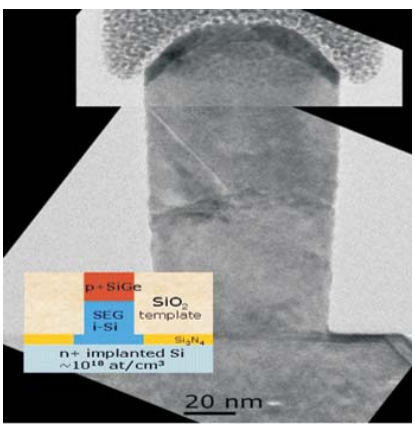

Figure 42. TEM micrograph of a 60nm wide Si/SiGe heterojunction nanowire.

Large-scale nanowire device integration (IMEC)
IMEC developed an integration flow together with the necessary process modules to fabricate vertical nanowire tunnel-FET devices with wrap-around gates. The nanowires were made by a top-down etch process, however, the integration flow is compatible with a bottom-up approach based on grown nanowires.

Next to the wrap-around gate configuration which provides the best gate control over the channel, a vertical TFET architecture allows a more readily implementation of heterostructures which are needed to boost the tunneling current (see modeling part).

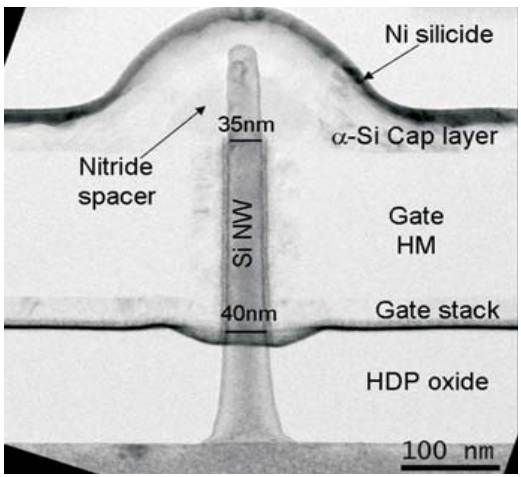

Figure 43. TEM cross-section of the final vertical 35nm NW TFET device (no top oxide isolation) with an advanced a-Si/TiN/HfO_2 gate stack

Functional vertical nanowire TFET devices were built on a 200mm wafer platform. [41] Vertical integration implied, among other, the implementation of bottom and top isolation layers, and a amorphous Si capping layer which simultaneously connects the TiN metal gate.

Vertical nanowire TFET device (IMEC)
Functional Si nanowire n- and p-TFETs were demonstrated and measured electrically at IMEC using a Kleindiek nanoprober apparatus mounted in a HRSEM. The experimental data are inline with literature data of all-Si Tunnel-FETs. To contributors knowledge, these devices are the first large-scale integrated vertical nanowire devices with state-of-the art high-k metal gate stack. [42]

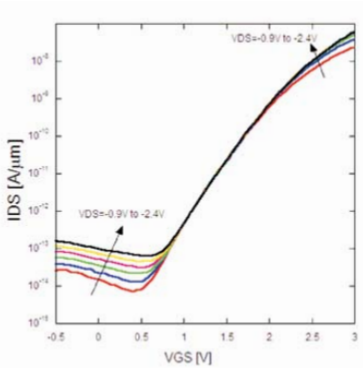

Figure 44. Input I_{ds}-V_{gs} characteristics of the n- TFET device with an epi grown P^+ source and a nanowire size of 50 nm on design.

1.5.2. Vertical device architectures and benchmarking

Short-gate and shifted-gate TFET device concepts (IMEC)
It was shown with the help of simulation that the position of the gate can impact the TFET device performance. The advantage of the short-gate TFET are the reduced ambipolar behavior, enhanced switching speed and relaxed processing requirements. [43] When the gate is shifted towards the source-channel a modest increase in on-current can be achieved.

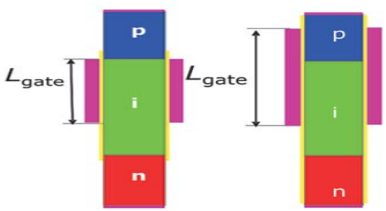

Figure 45. Sschematic representation of the short-gate(left) and shifted-gate (right) concepts.

Heterojunction-source TFET (IMEC)
It was shown that the on-current of the TFET device can be increased considerably by placing a foreign source material on top of the Si nanowire channel. Germanium and InGaAs were identified as the source materials of choice for an n-type and p-type TFET device, respectively. The advantage of remaining the Si channel is obvious as conventional Si processing can be used for the gate-stack fabrication. For this work new models needed developed commercial device simulators failed to correctly predict the performance of heterostructure TFETs. [44, 45] Together, the Ge-source for n-type and InGaAs source for p-type, enable a complementary silicon-based TFET suitable for competitive low-power applications. These heterostructure TFET configurations (Ge-Si, InA-Si and $In_{0.6}Ga_{0.4}As$-Si) and their corresponding *I-V* characteristics have been used as input for the circuit simulations by NXP.

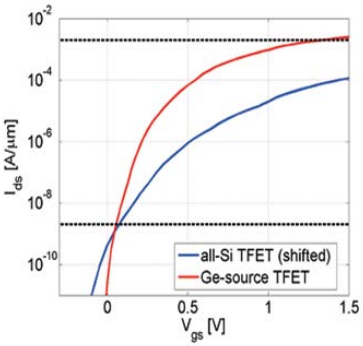

Figure 46. Comparison of I_{ds}–V_{gs} characteristics of all-Si TFET (short gate) and the proposed heterostructure Ge-source Si-TFET, indicating the boost of the current with nearly 2 orders of magnitude to the same level as Si MOSFETs (dashed curves).

1.5.3. Nanowire MOSFETs in the quantum capacitance limit

Quantum capacitance limit for conventional FETs (IBM)
Scaling of NW transistors was investigated by modeling. The important implication of the analysis is that NW with very small diameter enable ultimately scaled transistor devices in a wrap-gate architecture since

electrostatic integrity is preserved down to smallest dimensions. However, besides this pure geometrical argument the present study shows that NWs offer an additional scaling benefit. In the case of 1D transport, devices can be scaled towards the Quantum Capacitance Limit (QCL) which shows a clear scaling advantage in terms of the power delay product, i.e. the energy needed for switching the transistors. As a result, NWs exhibiting 1D transport are a premier choice as channel material for high performance, ultimately scaled FET devices. [46]

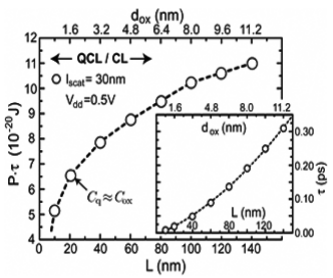

Figure 47. Power delay product and gate delay (inset) versus gate length and oxide thickness for conventional FETs as the transition from classical limit to the quantum capacitance limit is made.

Tunnel FETs in the quantum capacitance limit

Nanowire tunnel FETs versus nanowire MOSFETs (IBM).

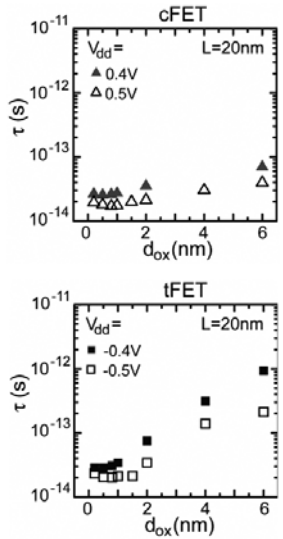

Figure 48. Gate delay versus oxide thickness for nanowire MOSFETs and tunnel FETs.

Modeling of nanowire MOSFETs and tunnel FETs using non-equilibrium Greens functions was used to calculate gate delays as a function of scaling oxide thickness. It was demonstrated that when FETs are scaled to the quantum capacitance limit the tunnel FETs exhibit the same on-state performance as MOSFETs using the gate delay as the performance metric. The on-current is an order of magnitude lower for the TFETs though.

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2. Overview of nanowire growth

Nanowires can be grown by a variety of methods, but the most common method by far is particle-assisted growth [1, 2] in metal-organic vapor phase epitaxy (MOVPE) or molecular beam epitaxy. This technique uses metal seed particles, most often gold, which act as nucleation centers [3] and direct the growth. The size, number and position of the resulting nanowires are determined by the seed particles, potentially allowing for a high degree of control over the final structures. In this section, patterned growth, heterostructures, doping, crystal structure control, and metal free growth will be briefly reviewed.

The gold seed particles can be deposited in a few different ways. Deposition of aerosol or colloid particles results in more or less randomly positioned nanowires. However, most applications require precise control of the nanowires, both in terms of position and size. Defining the gold particles by electron beam lithography, followed by gold evaporation and lift off, allows for this [4], see Fig. 1.

Formation of heterostructures is at the core of nanowire technology and novel device structures. Three major categories can be identified: axial, radial, and substrate/nanowire heterostructures, e. g. III–V nanowires on Si substrates.

First, axial structures can be formed if the growth precursors are alternated during growth. This results in a variation of the composition along the wire. Furthermore, it is well understood that nanowires represent an ideal system for the growth of axial heterostructures, since mismatched materials can be grown epitaxially on each other without misfit dislocations. This is possible because strain can be relieved by coherent expansion of the lattice outwards (along the wire diameter), avoiding dislocations. Axial heterostructure nanowires were first demonstrated in 1994 for the GaAs–InAs system [5].

Further development of this material system led to reports of high-quality interfaces despite the large lattice mismatch [6]. For the InAs–InP system, atomically sharp interfaces were also reported [7]. Nanowire heterostructure superlattices have been demonstrated for a variety of material systems, with lattice mismatch as high as 3% [8]. Much recent work has focused on attaining sharp heterointerfaces for various material and growth systems. As well, the development of heterostructure

nanowires involving ternary compounds such as GaAsP [9], InAsP [10] and InGaAs [11], further increases the potential for applications.

Second, radial structures, also known as core-shell structures, can be formed. In the lateral case, heterostructures are achieved by first growing nanowires by conventional particle-assisted growth, then by changing the growth parameters so that bulk growth is favored. In this way growth on the side facets of the wire will dominate, and shells will form [12].

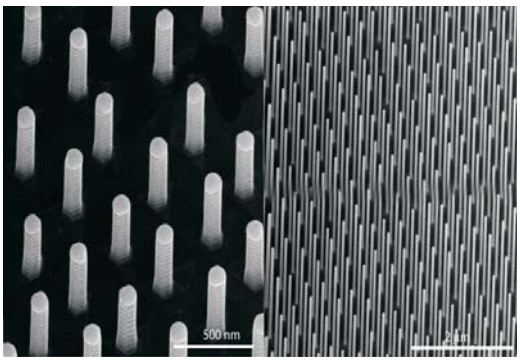

Figure 1. Scanning electron micrographs of gold particle-assisted, MOVPE grown, InAs nanowires in regular arrays, where the positions of the gold particles have been defined by electron beam lithography.

The third category, substrate/nanowire heterostructures, resembles the axial heterostructure with the difference that the substrate is less compliant. Compared to planar heteroepitaxy, the critical thickness for dislocation-free growth becomes considerable larger when strain can be relaxed also radially. This effect enables epitaxy of III–V nanowires on Si [13].

For electronics and optoelectronics applications it is necessary to control the conductivity and to be able to fabricate pn-junctions in nanowires. Thus it is of high importance to be able to dope the nanowires; pn-junctions in nanowires have been reported for nitride [14] and other III–V [15, 16] nanowires, even though the incorporation mechanism during particle-assisted growth is not well understood.

Semiconductor nanowires composed of III-V materials such as InAs typically suffer from frequent stacking defects. Although most of these materials exhibit zinc blende (ZB) structure in bulk, nanowires may also be composed of the related wurtzite (WZ) structure. If

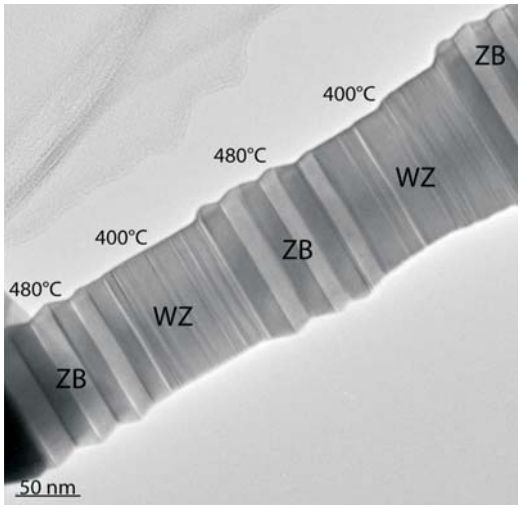

Figure 2. Transmission electron micrograph of a ZB-WZ polytypic superlattice in an InAs nanowire. The structure was achieved by periodically varying the growth temperature.

nanowire growth is not carefully controlled, the resulting structure may consist of a mixture of these two phases, together with twin planes, stacking faults and other polytypes. Various theoretical and experimental works have indicated that uncontrolled structural mixing may be detrimental to electronic and optical properties, and structural variations due to random intermixing may lead to unacceptable variability in material properties. On the other hand, the ability to select between ZB and WZ and to mix these structures in a controlled way may give access to new and exciting physics and applications.

It has recently been shown that the crystal structure of InAs nanowires can be tuned between pure WZ and pure ZB by careful control of experimental parameters, where temperature and nanowire diameter are the most significant [17]. This knowledge enabled the fabrication of twin plane superlattices and ZB–WZ polytypic superlattices in nanowires, see Fig. 2. Twin plane superlattices has also been controllably produced in InP nanowires by the introduction of dopants [18].

Finally, a successful method to grow perfect ZB nanowires that has been reported for GaAs nanowires is to use a two temperature method, where the growth is initiated at high temperature. After this, the temperature is decreased and the main parts of the nanowires are grown at a lower temperature in order to not overcome the energy barrier for twin formation

[19]. Quite surprisingly, the same group has recently reported that nanowires free from planar defects can be achieved by growth at high rate [20].

If semiconductor nanowires will be integrated in CMOS compatible processes, as suggested as one possible path to continue the downscaling of electronics, it is necessary to avoid growth from gold particles. Either, other more CMOS compatible metals have to be utilized as seed particles, or particle free nanowire growth has to be relized. Particle free growth from mask openings has been realized in InP [21], GaAs [22], and GaN [23]. Metal free growth has also been realized by growth from self-assembled nucleation templates on organically coated surfaces [24].

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3. Overview transport/optical properties of nanowires[2]

Nanometer-sized quasi 1-dimensional systems, such as semiconducting nanowires (NWs), are attractive building blocks for bottom-up nanotechnology including optoelectronics [1, 2] and manipulation of isolated electron spins [3, 4, 5]. Defect-free nanowire heterojunctions, both longitudinal [6] and radial [7, 8, 9], can be grown due to the small nanowire radius, which allows strain from lattice mismatch to be relaxed radially outwards.

Not only junctions between various different group III-V or IV elements, but even group III-V/IV junctions were reported [10, 11]. InAs is an attractive material because its small bandgap results in a low effective electron mass, giving rise to high bulk electron mobilities (at room temperature 22 700 cm^2/Vs [12] and at low temperature in planar structures over 600 000 cm^2/Vs [13]).

For bulk InAs, it is well known that the surface contains a large number of states that lie above the conduction band minimum and can contribute electrons to form a surface accumulation layer with a typical downward band bending between 0 and 0.26 eV [14]. Because of the large surface charge density, the Fermi level for InAs is pinned in the conduction band, which makes it easy to fabricate ohmic contacts without a Schottky barrier.

This InAs contact property enabled the observation of the superconductivity proximity effect in nanowires [15]. A surface accumulation layer combined with the large surface to volume ratio for InAs nanowires could promise good sensitivity for InAs nanowire sensor applications.

As a fraction of the surface states contributes electrons to the accumulation layer, the InAs surface contains a large number of ionized impurities. Electrons in the accumulation layer therefore experience much stronger ionized impurity scattering than electrons in the inner InAs region. Furthermore, because of the proximity to the surface, surface roughness scattering is also strong. This means that electrons in the surface layer have a strongly reduced mobility compared to electrons in the inner material, typically $\mu_{surface} \sim 4000\ cm^2/Vs$ [12, 14].

For microns thick planar structures of InAs, conduction is dominated by the electrons flowing through the inner region and mobilities are high. The electron mobility is strongly reduced for sub-micron sized InAs structures [12, 14], because of the higher surface-to-bulk ratio. At the same time, the total electron density will increase for smaller thicknesses.

Indications of a surface accumulation layer in InAs nanowires have been observed in [16], where smaller nanowire diameters show an increase in total electron density, consistent with the observations on accumulation layers in bulk InAs [12]. For InN nanowires, magneto-resistance measurements showed Altshuler - Aronov - Spivak (AAS) oscillations, suggestive of shell-like conduction through nanowires [17].

Conduction through InAs nanowires with typical diameters under 200 nm can be expected to be strongly influenced by the presence of a surface accumulation layer. The strong ionized impurity and surface roughness scattering in the surface accumulation layer could explain why InAs nanowires typically have low temperature mobilities of 1000-4000 cm^2/Vs [15, 18, 19, 20]. There have been two reports of InAs nanowires yielding mobilities exceeding 16000 cm^2/Vs [21, 22].

The surface band bending that causes the accumulation layer for InAs is a crystal surface property and the strength of the accumulation is known to be dependent on the surface orientation and termination [14]. Reducing the depth of the band bending will result in a higher relative contribution from the inner electrons to the total conduction and an increase in electron mobility.

An alternative approach to increase electron mobility would be to reduce the scattering in the surface channel by reducing the surface roughness and the scattering on surface states by surface passivation. Natural III-V oxides are soft, hygroscopic, compositionally and structurally inhomogeneous [23,24].

We have extracted the electron mobility from the gate dependence of the current using a simulated nanowire capacitance to the gate. Low temperature mobility has increased by a factor of 2-5 compared to bare InAs nanowires [9]. We also have found among the highest low temperature peak electron mobilities reported to this date, exceeding 25000 cm^2/Vs.

2 Val Zwiller, and L P Kouwenhoven, Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands

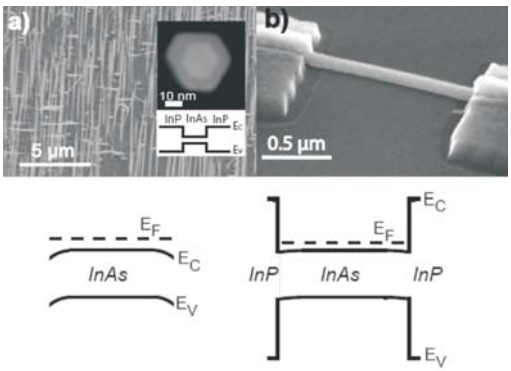

Figure 1. (a) Scanning electron microscope (SEM) image of InAs/InP core/shell nanowires grown on an InP substrate. Inset shows a high angle annular diffraction TEM image of a representative InAs/InP core/shell nanowire. The wire diameter is roughly 20 nm and the shell thickness 7-10 nm. The schematic shows the bandgap alignment for InAs sandwitched between InP. (b) SEM image of a typical nanowire device with Ti/Al contacts as used in our measurements. (c) Schematic of the bandgap bending of an InAs nanowire (a) and an InAs/InP core/shell nanowire.

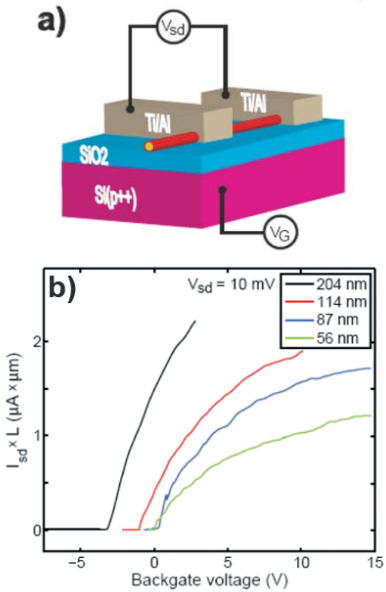

Figure 2. (a) Schematic of a Ti/Al contacted nanowire on a heavily doped Si substrate with SiO2 dielectric. (b) Current through the nanowire as a function of backgate voltage for several NW diameters. Such measurements are used to determine the electron mobility.

To create active photonic elements, the first key step is to incorporate a single quantum dot in a nanowire [25]. Semiconductor quantum dots are well known sources of single [26, 27] and entangled photons [28, 29, 30] and are naturally integrated with modern semiconductor electronics. Incorporation in semiconducting nanowires brings additional unique features such as natural alignment of vertically stacked quantum dots to design quantum dot molecules and an inherent one-dimensional channel for charge carriers. Furthermore, the unprecedented material and design freedom makes them very attractive for novel opto-electronic devices and quantum information processing.

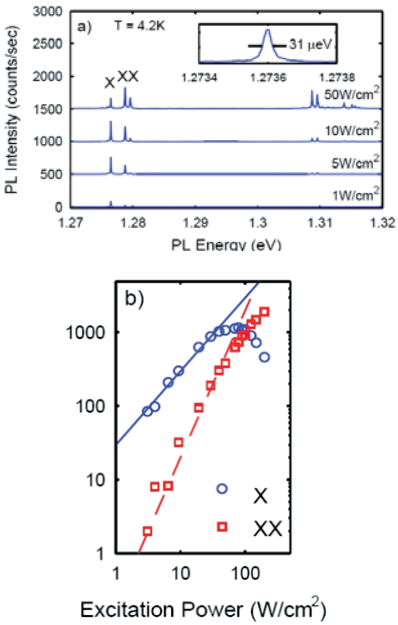

Figure 3. (a) Power dependence of the photoluminescence from a single quantum dot in a nanowire under continuous excitation at 532 nm. (b) Integrated power dependence of two narrow emission lines attributed to the exciton and biexciton. Samples grown by the Bakkers group.

Access to intrinsic spin and polarization properties of a quantum dot in a nanowire is challenging because of the limited quality of nanowire quantum dots, partly because the quantum dot is located very close to the sample surface. Moreover, the nanowire geometry strongly affects the polarization of photons emitted or absorbed by a nanowire quantum dot, and is thus an important obstacle for applications based on intrinsic spin or

polarization properties of quantum dots such as electron spin memory or generation of entangled photons. It has been shown that photoluminescence of homogeneous nanowires is highly linearly polarized with a polarization direction parallel to the nanowire elongation.

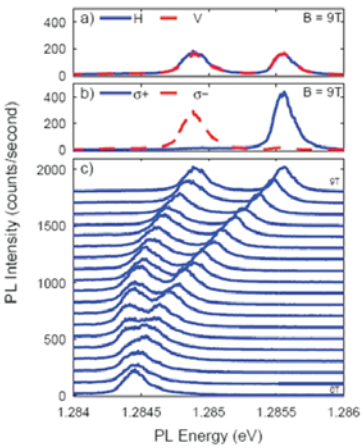

Figure 4. (a) and (b) Polarization sensitive photoluminescence of a standing nanowire quantum dot at 9 T. The solid (dashed) curve in (a) represents vertical (horizontal) linearly polarized exciton emission, denoted by H (V). The solid (dashed) curve in (b) represents left- (right-) hand circularly polarized exciton emission. (b) PL of a standing nanowire quantum dot under external magnetic field. Magnetic field is varied between 0 and 9 T in steps of 0.5 T. Sample grown by the Bakkers group (Philips).

In fig. **3a** we show a typical excitation power dependence revealing a usual exciton-biexciton behavior and a p-shell at 30 meV higher energy. The inset shows the narrowest emission we have observed to date with a FWHM of 31 μeV, limited by our spectral resolution. The integrated photoluminescence intensities of the exciton and biexciton as a function of excitation power, represented in fig. **3b**, show that the exciton (biexciton) increases linearly (quadratically) with excitation power and saturates at high excitation powers. This behaviour is typical for the exciton and biexciton under continuous excitation.

The nanowire geometry is not the only source of polarization anisotropy. Calculations by Niquet and Mojica [31] show that the polarization properties are strongly affected by the aspect ratio of the quantum dot dimensions, due to strain originating from the lattice mismatch between the nanowire and the quantum dot. However, in our case the strain is negligible due to the low phosphorus content and the main contribution to polarization anisotropy stems from the nanowire geometry.

Standing nanowires enable the extraction of any polarization with equal probability. This enables the observation of Zeeman splitting, provided that the emission linewidth is narrow enough. In fig. **4a** we show a magnetic field dependence of the exciton emission measured on a standing InP nanowire containing an InAsP quantum dot. The nanowire was grown by MOVPE using colloidal gold particles as catalysts by the Bakkers group. Polarization studies at 9 T show circular polarization (fig. **4b**) and no linear polarization (fig **4a**).

One challenge is to obtain good ohmic contacts to the p doped side of a nanowire LED. In figure **5** the device-layout, the nanowire LED emission and the electrostatic potential distribution along the device are shown. The junction is readily visible by transmission electron microscopy, the modification in doping brings about a modification of the nanowire diameter. Electrostatic force measurements are shown on the right of Fig. **5**, under a reverse bias of 1.5 V, a prominent drop in potential is observed at the expected position of the pn junciton.

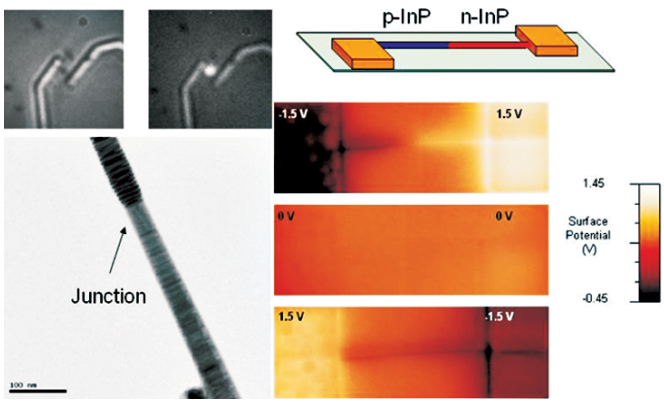

Figure 5. Single nanowire light emitting diode. Left: microscope image of the nanowire LED without and with forward bias. Bottom left: TEM image of a pn junction in an InP nanowire. Right: electrostatic force measurements under forward (top) and reverse (bottom) bias.

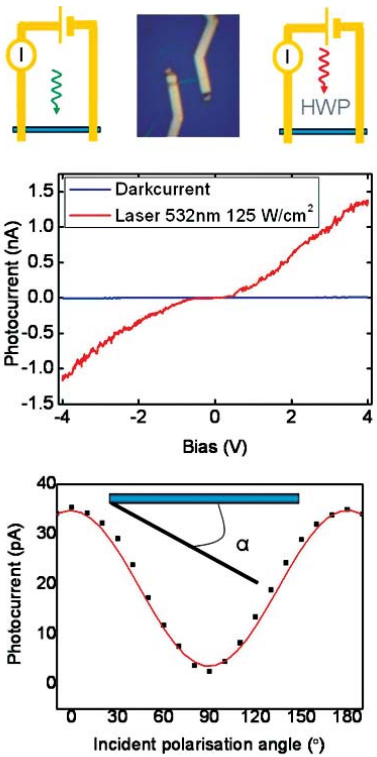

Figure 6. Photocurrent measurement on a single nanowire. Left: photocurrent as a function of applied bias. Right: photocurrent as a function of laser polarization.

Under zero and 1.5 V forward bias, no potential drop is observed on the pn junction, this demonstrates the presence of a pn junction in the contacted nanowire and shows that the contacts are ohmic. An electrically contacted nanowire can also be used for photodetection, as shown in figure **6**. Fig. **6** left shows the photocurrent intensity as a function of applied bias in the dark and under illumination. Fig. 6 right shows the polarization dependence of the photocurrent for a lying nanowire as a function of the laser linear polarization angle. The observed photocurrent polarization is in agreement with the polarization ratio measured by photoluminescence.

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4. Nanowires for energy applications

Several possibilities exist for the use of nanowires in the energy sector. This includes three categories: a) energy saving, b) energy harvesting, and c) energy storage. Within category a) we see two main research areas: lower power-consuming electronics and low-power illumination by solid-state lighting.

Nanowire FETs are regarded as one of the emerging nanoelectronic devices [1]. Low-power memory cells (so-called tunneling SRAMs) have already been demonstrated [2] as well as low-power tunnel FETs [3]. Additionally,vertically wrap-gated InAs nanowire devices with subthreshold slope around 90 mV/dec have been realized [4]. Besides electronic devices with lower power consumption, the thrive goes towards solid-state lighting devices for replacement of incandescent light bulbs and fluorescent lamps. A number of groups are working to realize this goal using nanowire structures. As early as 1994, light-emitting diode structures of GaAs nanowires with pn-junctions had been reported by the group of K. Hiruma at Hitachi [5]. First ten years later, similar devices had been demonstrated in nitride nanowire structures [6]. The fabrication of InP-InAsP nanowire LED structures where the electron-hole recombination is restricted to a quantum-dot-sized InAsP section has also been reported making these devices promising

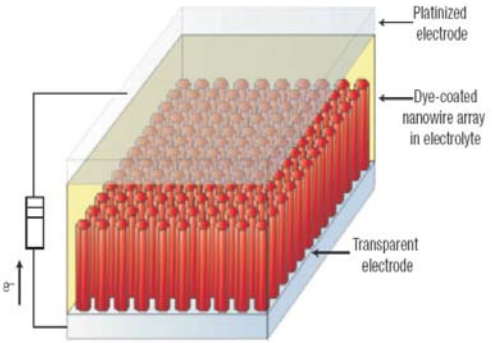

Figure 1. Schematic of a nanowire array for solar cell application.

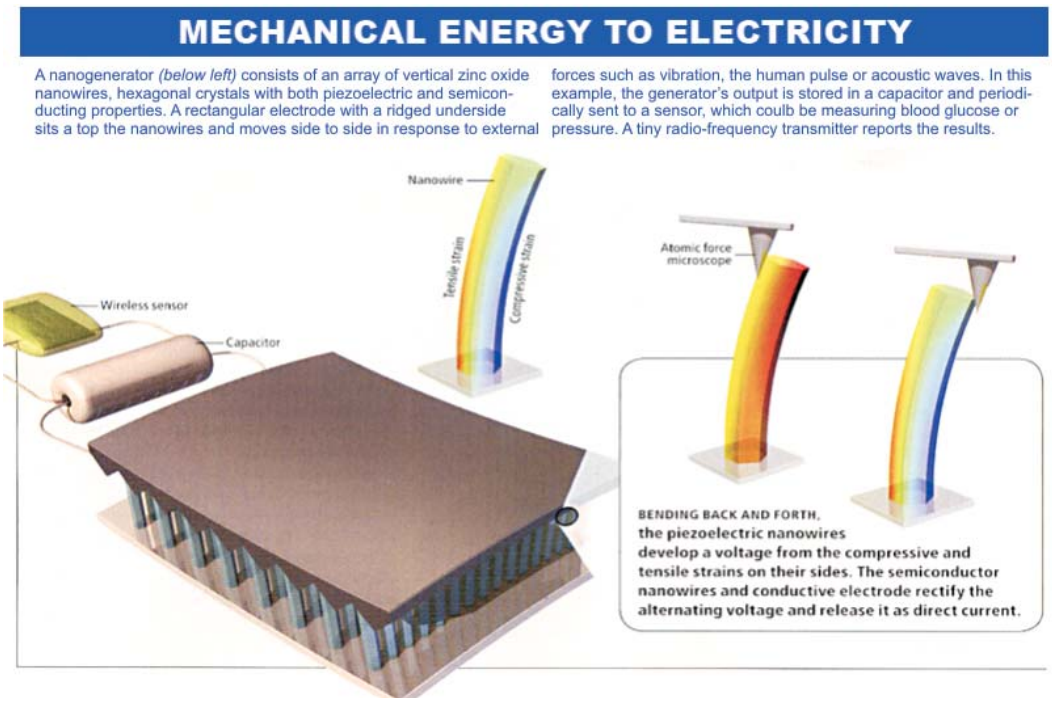

Figure 2. Schematic of piezoelectric energy conversion with nanowires.

candidates for electrically driven quantum optics experiments [7].

Arrays of nanowire light-emitting structures in the GaAs-InGaP were realized in cooperation between academic and industrial research in 2008 [8]. High brightness GaN nanowire LEDs emitting in the UV-blue region have been demonstrated [9] andnitride-based LED arrays have recently been reported [10].

Three research areas can be identified within category b) energy harvesting: conversion of light, heat or movement into electricity. For harvesting of light several nanowire materials have been and are investigated. P. Yangs group at Berkeley realized a dye-sensitized solar cell architecture in which the traditional nanoparticle film is replaced by a dense array of oriented and crystalline ZnO nanowires [11].

Using silicon, by a simple chemical etching techniquenanowire solar cell structures have been realized with poor performance [12] and p-i-n coaxial silicon nanowire solar cells have been reported with a conversion efficiency of 3.4% under illumination of one sun by the Lieber group from Harvard [13].
Silicon wires embedded in a polymeric film with potential to achieve high efficiency have recently been demonstrated [14]and even global players like General Electric Inc. show interest in silicon nanowire solar cells [15]. Solar cells have been realized with arrays of CdS nanowires grown on Al substrates and embedded in CdTe matrix showing a conversion efficiency of 6% [16].

Periodically aligned InP nanowires with pn-junctions have been reported with solar power conversion efficiency of 3.4% [17]. Other efforts on III-V nanowire solar cell structures are conducted within the EU-project AMON-RA [www.amonra.eu], where so far pn-junctions in InP nanowires have been demonstrated [18]. Some effort is going on to realize thermoelectric devices with nanowire structures, so far, mainly on a theroretical level [19]. However, first experimental studies have been conducted [20]. An interesting approach is the conversion of mechanical energy in electricity using the piezoelectric properties of ZnO nanowires [21].

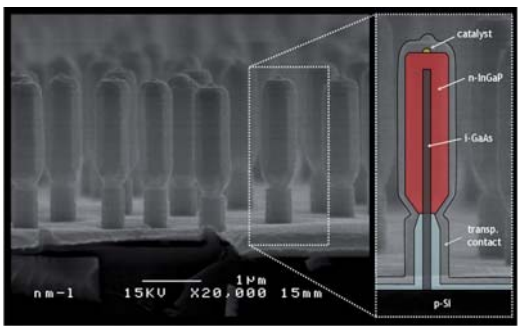

Figure 3. Nanowire array with light-emitting structures.

For the last category where nanowires could be used in the energy sector, energy storage, we are not aware of any ongoing research.

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5. Overview of nanowires for biology/ medicine

Nanowires have a size scale that overlaps with fundamental building blocks of cells. That makes them particularly suitable for biological and medical applications. Here we list a few examples of promising applications in our field of interest.

Neural network on a chip

Neural networks on a chip have many applications in neuroscience. The ability to control the cell position and the connections between cells can yield new knowledge on interactions between neurons and is a crucial component in the development of next-generation prostheses. Axonal guidance can be achieved using chemical or topographical modifications on the surface [1, 2]. Parallel rows of nanowires have proven to provide an excellent way of controlling cell growth and guidance of regenerating axons [3]. The rows of wires act as fences, confining the axons. The small radii of the wires prevent the axons from climbing the nanowires as the growth cone always encounters the wires at a 90° angle in contrast to micro structured walls, where fibers can reach the top of the wall by climbing at an intermediate angle.

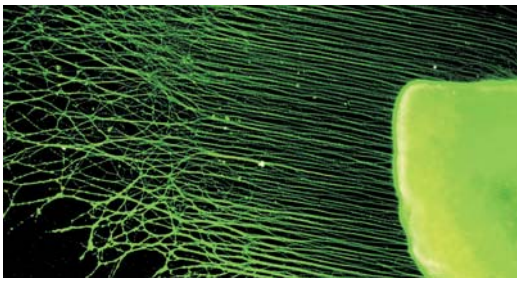

Figure 1. Fluorescence microcopy image of a superior cervical ganglion growing on a 1 x 1 mm² area with rows of GaP nanowires. The axons are guided with high fidelity by the rows of nanowires.

To be able to independently address two populations of axons on a chip surface, the different populations must be fully separated. This can be achieved by a ratchet pattern consisting of short rows of nanowires that rectify the axonal outgrowth [4].
Nanowires may thus provide a basis for advanced control of neuronal growth on a chip, where a large range of functionalities can be implemented, including chemical sensors and electrodes to investigate neuronal function at high temporal and spatial resolution.

Cellular force measurements using nanowire arrays

Cellular mechanotransduction is a rapidly growing field with recent studies showing that external and internal forces can alter cellular signaling and function [5, 6]. There are many ways to measure cellular forces in vitro. Optical tweezers and micropipettes are capable of probing picoNewton forces. While being very sensitive, these techniques can only measure forces at a few points simultaneously in a cell. With an elastic substrate cellular forces can be measured in an ensemble of cells [7]. This method, as well as its derived method based on elastomer micro-pillar arrays can measure forces from nanoNewton

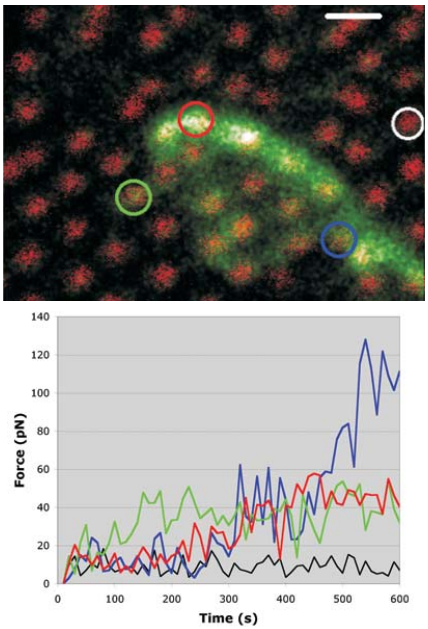

Figure 2. Cellular force measurements using nanowire arrays. (LEFT) Confocal fluorescence image of a growth cone on 40 nm diameter 5 µm long nanowires. Scale bar 1 µm. (RIGHT) Forces exerted on the nanowires highlighted in the left images. The forces range from 20 to 130 pN.

up to hundreds of nanoNewton [8, 9]. However, the spatial resolution of these methods is limited by the size of the pillars and/or markers to 2 µm at the very best. Nanowires, on the other hand, with their high aspect ratio

and small diameter have a great potential for detecting small forces with high spatial resolution, limited by the achievable density of the nanowires to about 1 µm. Using an array of 40 nm diameter and 5 µm long nanowires, force measurement down to 20 pN has been demonstrated on growth cone lamelipodia [10], consistent with data obtained using optical tweezers on the same system [11]. The results show that nanowire arrays can be used as a sensitive force probe that has the advantage of allowing simultaneous measurements with high probe density and high spatial resolution.

Hollow nanowires

The controlled transfer of specific molecules into (and out of) cells is a fundamental tool in cell biology. Electroporation is widely used in bulk and on single cells. However, it merely opens up a conduit for diffusional transport into or out of the cell. Microinjection have been developed to provide a more controlled and selective transport into single cells [12]. Large needles require very slow movement of the needles to allow the adaptation of the cytoskeleton [13, 14]. Decreasing the size of the needle to the nanoscale minimizes any deleterious effect on the cell. Furthermore, arrays of needles can be defined on a flat substrate for massively parallel single-cell experiments. One example involves the binding of plasmid DNA to the nanoneedles and the subsequent impalfection of cells with a gfp-coding plasmid [15]. Another example involves hollow nanowires that are filled with the molecule of interest and used similarly [16]. In both cases the wires are preloaded and used only once and furthermore rely on passive release in the cytosol. Hollow nanowires connected to an external fluidics system avoid these limitations. By combining such nanowires with a microfluidic system for cell capture, an array of individually addressed cells can be created with potential applications in systems biology, neurobiology, tissue engineering and stem cell differentiation.

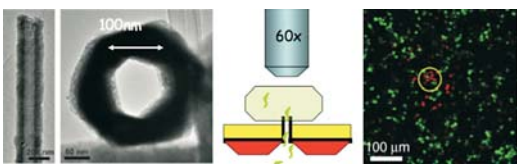

Figure 3. Hollow nanowires for molecular transport. (LEFT) Initially GaAs/Al_2O_3 core/shell nanowires are grown. Subsequently the GaAs core is etched resulting in a hollow Al_2O_3 nanowire. (CENTER) Schematic of a cell impaled by a nanowire with molecules diffusing from the bottom reservoir. (RIGHT) Macrophages expressing GFP on a surface. Where the hollow nanowires establish a connection across the device, membrane impermeable propidium is injected by diffusion into the cells.

Nanowire-based biosensors

Semi-conductor nanowire field effect transistors are a very sensitive tool for detection of biomolecules. The binding of analyte molecules to immobilized DNA or antibody probes may result in a change in the surface charge, thereby changing the nanowire conductance. This method has been used successfully to detect single viruses, cancer markers, and proteins [17-19].

Nanowire-based electrodes for neural interfaces

The development of neural interface is a rapidly growing field. Standard neural electrodes have sizes in the micrometer range and their implantation triggers a strong inflammatory response that often makes it necessary to remove the electrode. It has been shown that carbon nanotubes at the surface of neural electrodes improve the electrical properties of the electrodes and elicit a lower tissue inflammatory response [20]. Carbon nanotubes form a very strong seal with the neurons, which is also expected to be the case using nanowires. Nanowire field effect transistor arrays have been used to form nanoscale junctions with axons and dendrites of neurons cultured on the array. The nanowire transistors

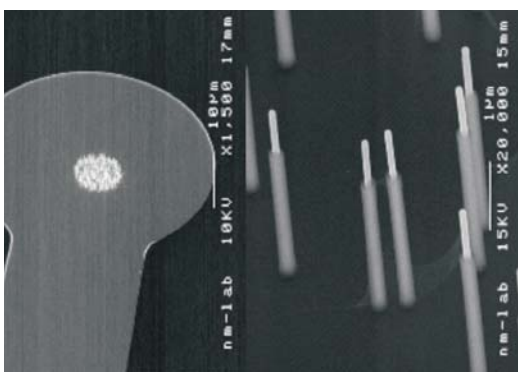

Figure 4. Scanning electron micrograph of nanowire-based electrodes.

could stimulate and inhibit neuronal signals, as well as measuring their amplitude and firing rate [21].
It has been shown that neurons can grow and thrive on vertical nanowire substrates [15, 22]. The cell survival was higher on nanowire substrates compared to controls (growth on flat surfaces) despite the fact that the cells were penetrated by the nanowires. This suggests that nanowire-based electrodes will form tighter junctions with the neurons and therefore will record or stimulate more efficiently. In this context, new electrodes consisting of vertical nanowires on the surface of a microelectrode are being developed for brain implantation purposes. Such nano-electrodes could communicate with multiple individual neurons in the brain on a long-term basis. The possible applications are diverse, ranging from fundamental studies of mechanisms of learning to therapeutic treatment of Parkinson's disease.

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Annex I

I. Report from the NODE workshop on nanowire electronics

During the days September 23-24, 2009, was organized in Lund the "NODE Workshop on Nanowire Electronics" which was both a dissemination event of the four years of the Integrated Project NODE ("Nanowire-based One-Dimensional Electronics"), and an opportunity for this research field to obtain sharp feed-back from a set of highly knowledgeable invited key-note speakers.

The focus was on four key issues for the field: one session on "Wrap-gate Transistors", for which we were pleased to have as external key-note speakers Wilfried Hänsch from IBM Yorktown Heights, talking primarily about planar wrap-gate transistors and circuits, and Matthias Passlack from TSMC-Europe in Leuven, talking primarily about comparisons between traditional CMOS and the opportunities from integration of III-V wrap-gate transistors with silicon technology. Added to these presentations where two reports from the NODE research, by Claes Thelander from Lund and Mikael Björk from IBM Zurich.

In the second focused sesson, on "Ultra-low Power Devices" the key-note presentation was given by Joachim Knoch from TU Dortmund, talking primarily on the potential of Tunnel FETs for ultra-low power applications, with a special focus on what can be achieved in terms of ultra-steep sub-threshold slopes. Two internal NODE presentation were also made here, by Anne Verhulst at IMEC Leuven and Heike Riel from IBM Zurich.

In the third focused session, we looked at opportunities for "Other Nanowire Applications", which primarily in the program meant applications for Memories and RF-applications. The external key-note speaker, Thomas Mickolajick from Freiberg University focused on Memory applications and how nanowire technology can come to contribute to this development. From the NODE research was reported by Walter Weber from the Namlab in Dresden and by Erik Lind from QuMat Technology.

In the fourth of the focused sessions, on "Integration Issues", Hugo De Man from IMEC, Leuven gave an overview of the field and pointed out the challenges that a new technology has to face to compete with CMOS. He also stressed the value of not limiting the assessment of what nanowires can bring to only ICs, but also to focus on the "More than Moore" opportunities offered. In this session, the state-of-the-art as has been reached in NODE was reported by Philippe Vereecken from IMEC Leuven.

The concluding session was based on a panel discussion with contributions from Lars Tilly (Ericsson Research), Wilfried Hänsch (IBM), Hugo De Man (IMEC) and Matthias Passlack (TSMC), and was introduced and moderated by Lars-Erik Wernersson from Lund. Many different topics were covered, including the pull from systems industry, like mobile phone applications, the issues of integration of a new technology with main-stream silicon technology, and comparisons between the situation for this field of R&D in Europe in a comparison with the USA, where quite different traditions and conditions lead to a more optimal development of the field.

- **Hugo De Man:** "As a conclusion I propose that, if we want to investigate nanowire TFETs as a possible low power device after ultimately scaled CMOS, a *multidisciplinary* project on *Systemability of future technologies* should be launched where process, physics team up with circuit and system people. Otherwise we get stuck in the famous *'European Research Paradox'* where we complain about the fact that excellent research does not lead to true innovation i.e. its translation of it in industrially relevant results." - - - " Finally perhaps a bit too much focus is on nanowires as a successor for CMOS logic or RF circuits. As was noted by TSMC there is also the trend towards *More than Moore* technologies that will play a dominant role in the world of *Ambient Intelligence* by complementing the intelligent CMOS part with nomadic communication and nanotech interfaces to the living and non-living world. Thereby *novel functionality* such as sensors, actuators, optical interfaces, resonators etc. is needed. Nanowires can provide novel solutions in this field."

- **Matthias Passlack:** "Feature size scaling which has been driving CMOS throughout the last decades will increasingly be complemented by other advance-ments on the device and system level.

Transistor trends include use of high-k dielectrics, multi- and wrap around gate architectures, strained layers, heterostructures, and new channel materials. III-V semiconductors with their high carrier (electron) mobility, direct bandgap functionality, and flexibility for heterostructure design have recently garnered increasing attention. The III-V nanowire appears to be a universal vehicle addressing many of the above aspects including high electron mobility channel, wrap around gate, direct bandgap, and heterostructure design. Moreover, nanowires provide new avenues for high crystal quality in highly lattice-mismatched systems such as III-V semiconductors on silicon substrate. For example, III-V nanowires could be the efficiency RF components and light emission devices monolithically integrated on a silicon substrate."

2. Report on the Nanowire Growth Workshop 2009 (NWG2009)

Introduction

NWG2009 (Paris, 26-27 october 2009: http://sites.google.com/site/nwg42009/) was the 4th edition of an international meeting highly focused on semiconductor nanowire growth. The workshop was first held in Lund (2006 and 2007) and then in Duisburg (2008). This year, the workshop was organized in Paris and lasted two days. It brought together 116 researchers from 19 countries.

The workshop program comprised six invited talks, 19 orals and 48 poster presentations. This sizable and active participation indicates that many issues are still to be addressed to improve the control of nanowire growth, which is much more complex than two-dimensional layer growth. In return, the researchers expect much more flexibility to fabricate original nano-objects which will allow investigating the physics of one-dimensional systems or designing new devices with improved performances.

Steering committee of Nanowire Growth Workshop

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NWG2009 organizing committee

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Marcoussis, France

Keywords

Nanowires; Crystal growth; Elementary semiconductors; Compound semiconductors; III-V on Si Cristalline structure; Catalyst; Structural properties; Crystal defects; Morphology; Surface energies; Doping, p-n junctions; Growth modeling; Self-assembling

Program of NWG2009

Invited speakers

S. Kodambaka, Department of Materials Science and Engineering, University of California Los Angeles, Los Angeles, USA

Growth of silicon nanowires using AuAl alloy catalysts

V. Schmidt, Max-Planck-Institut für Mikrostrukturphysik, Halle, Germany
Aspects of silicon nanowires growth

K. Kishino, Department of Engineering and Applied Sciences, Sophia Nanotechnology Research Center, Sophia University, Tokyo, Japan
Blue to red emission InGaN-based nanocolumns and related technology

R. R. LaPierre, Centre for Emerging Device Technologies, McMaster University, Hamilton, Canada
Fundamental issues in MBE-grown nanowires for device applications

M. Galicka, Institute of Physics, Polish Academy of Sciences, Warsaw, Poland
III-V nanowires of wurtzite structure

P. Caroff, Institut d'Electronique, de Microélectronique, et de Nanotechnologie, Villeneuve d'Ascq, France
Tuning crystal structure in III-V nanowires

Oral contributions

F. Li, Department of Materials, University of Oxford, Oxford, United Kingdom
Doping-dependent nanofaceting on silicon nanowire surfaces

T. Xu, Institut d'Electronique, de Microélectronique et de Nanotechnologie, Villeneuve d'Ascq, France
Atomic scale structure of <III>-oriented Si nanowire

N. J. Quitoriano, Mining and Materials Engineering Department, McGill University, Montreal, Canada
Engineering Si and Ge nanowire growth direction

I. Zardo, Walter Schottky Institut, Technische Universität München, Garching, Germany
Silicon nanowires growth using gallium and indium as catalysts

K. Naji, Institut des Nanosciences de Lyon, Ecole Centrale de Lyon, Ecully, France
Defect free InP NWs on SrTiO3 substrates grown by VLS-assisted molecular beam epitaxy
T. Gotschke, Institute of Bio- and Nanosystems, Forschungszentrum Jülich, Jülich, Germany
Doping effects of MBE-grown InN NWs by means of Si and Mg

M. Knelangen, Paul-Drude-Institut für Festkörperelektronik, Berlin, Germany
Strain relaxation and nucleation mechanisms of self-induced GaN nanowires

E. Bellet-Amalric, Nanophysics and Semiconductors Group, INAC and Institut Néel, Grenoble, France
Insertion of CdSe quantum dots in ZnSe Nanowires: MBE growth and microstructure analysis

A. Hayashida, Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo, Japan ***Fabrication of a GaAs quantum well embedded in AlGaAs/GaAs hetero-structure nanowires by selective-are MOVPE***

M. T. Borgström, Solid State Physics, Lund University, Lund, Sweden
Decoupled axial and radial nanowire growth by in-situ etching

V. G. Dubrovskii, St.-Petersburg Physics and Technology Centre for Research and Education, Russian Academy of Sciences, St.-Petersburg, Russia
Self-consistent theory of nanowire growth and crystal structure

J. Johansson, Solid State Physics, Lund University, Lund, Sweden
Wurtzite–zinc blende transition in InAs nanowires

B. Mandl, Institute for Semiconductor and Solid State Physics, University Linz, Austria
Time dependence of Au-free InAs nanowire growth

R. E. Algra, Materials Innovation Institute, Delft, The Netherlands
Correlated twins in nanowires

H. Shtrikman, Braun Center for Submicron Research, Weizmann Institute of Science, Rehovot, Israel
High quality InAs nanowires grown by VLS assisted MBE

H. J. Joyce, Department of Electronic Materials Engineering, Australian National University, Canberra, Australia
Optimising GaAs and other III–V nanowires

E. Gil, Laboratoire des Sciences et Matériaux pour l'Electronique et d'Automatique, Université Blaise Pascal, Clermont-Ferrand, France
Rodlike GaAs nanowires with exceptional length

Summary and highlights of the workshop

NWG2009 was the 4th edition of an international meeting highly focused on semiconductor nanowire growth. The workshop was first held in Lund (2006 and 2007) and then in Duisburg (2008). This year, the workshop was organized in Paris and lasted two days. It brought together 116 researchers from 19 countries.

The workshop program comprised six invited talks, 19 orals and 48 poster presentations. This sizable and active participation indicates that many issues are still to be addressed to improve the control of nanowire growth, which is much more complex than two-dimensional layer growth. In return, the researchers expect much more flexibility to fabricate original nano-objects which will allow investigating the physics of one-dimensional systems or designing new devices with improved performances.

Gold remains the most popular catalyst used to assist semiconductor nanowire formation. Alternative metals have been presented which can modify the growth kinetics, the nanowire morphologies and their structure. In particular, catalyzing Si/Ge nanowire growth with (Au,Al) alloy particles tends to favour the vapour-solid-solid (VSS) mode, which produces sharper interfaces in Si/Ge heterostructures (S. Kodambaka, University of California, Los Angeles, USA). An overview of the expected growth mode - vapour-liquid-solid (VLS) or VSS - for a large panel of metallic catalysts has been presented by V. Schmidt (Max-Planck-Institute für Mikrostrukturphysik, Halle, Germany).

An interesting influence of the proximity of oxides on nanowire growth has been demonstrated. N. J. Quitoriano (Hewlett-Packard Laboratories, Palo Alto, USA) showed that nanowire growth can be guided by the SiO_x surface of pre-patterned silicon-on-insulator (SOI) substrates. The Si or Ge NWs grow along <111> directions until they get in contact with the SiO surface where they pursue their growth along <110> directions, parallel and in contact with this surface. This guided growth suddenly kinks if the contact with SiO_x ceases. Growth of InP nanowires along <001> has also been shown to be possible if initiated on a $SrTiO_3$ epitaxial layer deposited on Si (001) (K. Naji, Université de Lyon/ECL, Ecully, France).

T. Xu (IEMN, Lille, France) reported scanning tunneling microscopy investigations performed on Si nanowire sidewalls. The sawtooth side facets systematically show Au-induced reconstructions, Au being the catalyst material.

Impressive realization of organized arrays of InGaN-based nanocolumns obtained by selective area growth on masked surfaces has been achieved by K. Kishino's group (Sophia Nanotechnology Research center, Tokyo, Japan). Development of light emitting diodes fabricated from these nanocolumns is going on rapidly.

M. T. Borgstrom (Lund University, Sweden) has shown that using HCl gas during the vapor phase epitaxy of InP nanowires helps to decouple axial and radial growth. A very selective axial growth has been demonstrated.
It was clearly established that attempts to dope nanowires often result in unexpected effects on the morphology: faceting of the sidewalls for B-doped Si nanowires (F. Li, University of Oxford, UK); increase of volume and density for Mg–doped InN nanowires (T. Gotschke, Research Center Jülich, Germany).

Many presentations focused on the possibility to control the nanowire crystal phase (wurtzite or zinc blende) in compounds semiconductors, , or at least to obtain stacking fault-free nanowires. These studies have identified, both experimentally and theoretically, specific conditions meeting such objectives, but it appears that a perfect control remains very challenging. In InAs nanowires, crystal phase transition from wurtzite to zinc blende was observed above a critical diameter (100 nm) which depends on growth temperature (J. Johansson, Lund University, Sweden). Slower growth

rates were shown to be favorable to stabilize the pure wurtzite structure (H. Shtrikman, Weizmann Institute of Science, Israel). It was predicted (and also observed) that zinc blende can be obtained not only at very low supersaturation, but also at very high supersaturation (V. Dubrovskii, St Petersburg Physics and Technology Centre RAS, Russia). Alternatively, the control of periodic arrays of twin boundaries in single-phase has been achieved (R. Algra, Materials Innovation Institute, Delft, The Netherlands). The workshop ended with an original presentation by E. Gil (LASMEA, Clermont-Ferrand, France) reporting exceptional GaAs nanowire growth rates elaborated by hydride vapor phase epitaxy (40 µm length in 15 min) with long segments (tens of µm) of pure and twin-free cubic structure.

Conclusion

In conclusion, the NWG2009 workshop has provided a forum for presenting the most recent advances on nanowire growth mechanisms, contributing actively to the progress of this challenging topic. Since many nanowire growth issues are still very topical, the NWG workshop has to be maintained. The steering committee has decided that it should continue with a similar format (number of participants limited to about 150 people, about 2 days duration) in 2010. The topics of NWG2010 should keep highly focused on nanowire growth in order to avoid overlapping with other conferences (ICON, MRS meetings, MBE or MOCVD conferences ...), where the applications of nanowires can be presented and discussed in more details.

Acknowledgements

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- Hong Kong Univ Sci & Technol, Inst Nano Sci & Technol, Hong Kong
- Chinese Acad Sci, Inst Phys, Beijing
- Tsing Hua Univ, Dept Phys, Beijing
- Univ Sci & Technol China, Struct Res Lab, Anhua
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- Pohang Univ Sci & Technol, Dept Mat Sci & Technol, Pohang, South Korea
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- Ecole Polytech Fed Lausanne, Inst Mat, Lausanne, Switzerland
- Institute for Semiconductor and Solid State Physics, University Linz

Potential applications of nanowires
Semiconductor families, applications, and industrial actors

Popularity of semiconductor families in nanowire research

33 %	ZnO
28 %	Si, SiGe, SiC
17 %	III-Vs (excluding nitrides)
12 %	II-VI (excluding ZnO)
10 %	GaN and other nitrides

Fields of nanowire applications

The potential applications which are the most investigated today are:

- Nano-electronics (transistors, spintronics)
- Light emitting devices (LEDs lasers), photodetector
- Photovoltaics
- Field emission
- Biological and chemical sensors
- NEMS and MEMS

Main industrial companies involved in the development of nanowire-based products:

- Samsung
- Hewlett Packard
- Nanosys Inc
- Philips
- IBM
- Sharp
- Qunano AB

Annex II

I. NODE project objectives and main achievements

Overview of the general project objectives

Materials growth and processing technologies of semiconductor nanowire devices were developed and evaluated for their possible impact as key add-on technologies to standard semiconductor fabrication. The goal was also to reach a deepened understanding of the physics of one-dimensional semiconductor materials and nanowire-based devices, and to develop new functionalities not found in traditional higher-dimensional device structures.
NODE studied in detail a set of key device families based on semiconductor nanowires, such as tunneling devices, and field-effect transistors, as well as explored unique opportunities that may be offered by nanowires in areas for storage applications. NODE also made a dedicated effort to evaluate the potential for integration of nanowire-specific processing methods and to assess the compatibility with requirements from conventional semiconductor processing, as well as evaluate novel architectural device concepts and their implementation scenarios. More specifically the main objectives of NODE were:

- To build and evaluate electronic devices based on semiconductor nanowires:

  > NW-based transistors with increased frequency response and decreased power consumption

  > Nanowire logic elements

  > Explore potential for novel device designs using nanowires

- To assess nanowire growth and related nanostructuring in terms of up-scalability and Si-integration potential

Achievements

The research in NODE in many cases represented the state-of-the art in its field. The NODE partners are currently in the research forefront in areas such as (i) understanding of nanowire growth mechanisms, (ii)

control of nanowire growth and nanowire doping (iii) characterization of the structural properties of nanowires (iv) processing of vertical nanowires structures (v) device research and development along the two tracks: InAs nanowire wrap-gate FETs and Si nanowire tunnel FETs, using both etched (fully-CMOS compatible) and bottom-up grown nanowires.

Since the project included partners with strong background in research related to CMOS-integration, NODE had a strong focus on finding CMOS-compatible growth methods and processing conditions. Important sub-projects have therefore been to develop growth methods where gold is not required, and catalyst-free techniques have been developed for both InAs- and Si-nanowires, and Al, Pd, Ag seeding of Si nanowires has been demonstrated. A particular effort was also made on investigating the effect of gold on Si nanowires during growth and processing.

Design, fabrication and characterization of the first reported vertical RF-compatible nanowire transistors were carried out, demonstrated with InAs wrap-gate nanowires. Steep slope devices based on Si-nanowires were implemented, where also the first functional Si nanowire tunnel-FETs processed on 200mm wafers on a CMOS platform were demonstrated. Finally, multi-gated Si nanowire Schottky barrier FETs were realized, where an inverter function was demonstrated.

The NODE project has had a very high output in publications, and in total over 100 articles has been published at the end of the project. This clearly shows that considerable progress was made in the project and that the research was competitive on an international level. The NODE partners have applied for at least 48 patents related to nanowire research and development, not including patent applications submitted within the last 18 months that are not yet publicly posted.

2. NODE papers published in refereed journals

Publications 1–94 are already published, 95–96 are accepted for publication, and 97–103 are submitted to refereed journals.

1. “Structural properties of <111> B-oriented III–V nanowires” J. Johansson et al., Nature Materials 5, 574 (2006)

2. “On the formation of Si nanowires by molecular beam epitaxy” P. Werner et al., Int. J. Mat. Res. 97, 1008 (2006)

3. “Supercurrent reversal in quantum dots” J. A. van Dam et al., Nature 442, 667 (2006)

4. “Electronic and optical properties of InAs/GaAs nanowire superlattices” Y.M. Niquet, Phys. Rev. B 74, 155304 (2006)

5. “Nanowire-based one dimensional electronics” C. Thelander et al., MATERIALS TODAY 9, 28 (2006)

6. “Position-controlled interconnected InAs nanowire networks” Dick KA, Deppert K, Karlsson LS, et al. NANO LETTERS 6, 2842 (2006)

7. “Optimization of Au-assisted InAs nanowires grown by MOVPE” Dick KA, Deppert K, Samuelson L, et al. JOURNAL OF CRYSTAL GROWTH 297, 326 (2006)

8. “Phase segregation in AlInP shells on GaAs nanowires” Skold N, Wagner JB, Karlsson G, et al. NANO LETTERS 6, 2743 (2006)

9. “Nanowire-based multiple quantum dot memory” Nilsson HA, Thelander C, Froberg LE, et al. APPLIED PHYSICS LETTERS 89, 163101 (2006)

10. “Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor” Lind E, Persson AI, Samuelson L, et al. NANO LETTERS 6, 1842 (2006)

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Annex 2
List of nanoICT registered groups & Statistics

Annex 2 - List of nanoICT registered groups & statistics

Annex 2.1 List of nanoICT registered groups

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Commissariat à l'Energie Atomique (Grenoble)	CEA-Grenoble www.cea.fr	France	Baptist, Robert robert.baptist@cea.fr
Universitat Autonoma de Barcelona	Electronic Circuits and Systems Group www.uab.es	Spain	Barniol, Nuria nuria.barniol@uab.cat
AMO GmbH - Gesellschaft für amgewandte Mikro und optoelektronik mit beschränkter Haftung	www.amo.de	Germany	Baus, Matthias baus@amo.de
Leiden University	Nanophysics lorentz.leidenuniv.nl/beenakker	Netherlands	Beenakker, Carlo beenakker @lorentz.leidenuniv.nl
Italian National Institute of Nuclear Physic Laboratori Nazionali di Frascati	Nanotechnology www.lnf.infn.it/	Italy	Bellucci, Stefano Stefano.Bellucci@lnf.infn.it
CIC nanoGUNE Consolider	Nanomagnetism www.nanogune.eu	Spain	Berger, Andreas a.berger@nanogune.eu
CIC nanoGUNE Consolider	Self-Assembly www.nanogune.eu	Spain	Bittner, Alexander a.bittner@nanogune.eu
University of Copenhagen	Nano-Science Center, NanoChemistry nano.ku.dk/	Denmark	Bjørnholm, Thomas rb@nano.ku.dk
QuantumWise A/S	quantumwise.com	Denmark	Blom, Anders info@quantumwise.com
Commissariat à l'Energie Atomique	CEA Nanoscience Program www.cea.fr	France	Bourgoin, Jean-Philippe Jean-Philippe.Bourgoin @cea.fr
Technical University of Denmark	Theoretical Nanoelectronics www.nanotech.dtu.dk/TNE	Denmark	Brandbyge, Mads Mads.Brandbyge @nanotech.dtu.dk
Institut pluridisciplinaire de recherche sur lenvironnement et les matériaux	iprem-ecp.univ-pau.fr/live/	France	Brown, Ross ross.brown@univ-pau.fr

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Institution	Group / Web	Country	Contact Person / Email
Ecole Polytechnique Fédérale de Lausanne	Microsystems laboratory - I lmis1.epfl.ch	Switzerland	Brugger, Juergen juergen.brugger@epfl.ch
TU Kaiserslautern		Germany	Burkard, Hillebrands hilleb@physik.uni-kl.de
University of Geneva	Mesoscopic physics group http://mpej.unige.ch/~buttiker/	Switzerland	Buttiker, Markus Markus.Buttiker@unige.ch
Consorzio Interuniversitario Nazionale per la Scienza e Technologia dei Materiali	Laboratory of Molecular Magnetism www.instm.it	Italy	Caneschi, Andrea andrea.caneschi@unifi.it
Centre National de la Recherche Scientifique Ecole Supérieure de Physique et de Chimie Industrielles - ParisTech	Institut Langevin and Laboratoire Photons et Matière www.espci.fr	France	Carminati, Rémi remi.carminati@espci.fr
Universitat Autonoma de Barcelona	Nanoelectronica Computacional www.uab.cat/grup-recerca/nanocomp	Spain	Cartoixa, Xavier Xavier.Cartoixa@uab.es
Università di Firenze	European Laboratory for Nonlinear Spectroscopy www.lens.unifi.it	Italy	Cataliotti, Francesco fsc@lens.unifi.it
University Paris Sud		France	Chappert, Claude chappert@ief.u-psud.fr
Université catholique de Louvain	Unité de Physico-Chimie et de Physique des Matériaux (PCPM) www.uclouvain.be	Belgium	Charlier, Jean-Chris. jean-christophe.charlier @uclouvain.be
Biotecgen SRL	Biotecgen www.biotecgen.it	Italy	Chiesa, Maurizio m.chiesa@biotecgen.it
University of Vigo	New Materials Group www.laser.uvigo.es	Spain	Chiussi, Stefano schiussi@uvigo.es
Commissariat à l'Energie Atomique	INAC/SPINTEC www.spintec.fr	France	Chshiev, Mairbek mair.chshiev@cea.fr
University of Calabria	Microelectronics and Microsystems Laboratory www.unical.it/portale/strutture/dipartimenti/deis/	Italy	Cocorullo, Giuseppe crupi@unical.it
University of Mons-Hainaut	Laboratory for Chemistry of Novel Materials www.umh.ac.be/morris	Belgium	Cornil, Jérôme Jerome@averell.umh.ac.be
Fundacion Phantoms	Nanotechnology www.phantomsnet.net	Spain	Correia, Antonio antonio@phantomsnet.net
Dresden University of Technology	Chair of materials science and nanotechnology, Prof. Dr. Gianaurelio Cuniberti nano.tu-dresden.de	Germany	Cuniberti, Gianaurelio office@nano.tu-dresden.de
Technical University of Denmark	DyNEMS group www.nanotech.dtu.dk	Denmark	Davis, Zachary J. zachary.davis @nanotech.dtu.dk
University of Sheffield	Semiconductor materials and devices www.sheffield.ac.uk	United Kingdom	De Souza, Maria Merlyne m.desouza @sheffield.ac.uk
Commissariat à l Energie Atomique	LEM (Laboratoire d Electronique Moélculaire) iramis.cea.fr/spec/lem	France	Derycke, Vincent vincent.derycke@cea.fr

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Université de la Méditerranée	CNRS-CINaM www.cinam.univ-mrs.fr	France	Didier, Tonneau tonneau@cinam.univ-mrs.fr
University of Paris-Sud - CNRS	Nanoelectronics Group www.ief.u-psud.fr/	France	Dollfus, Philippe philippe.dollfus@u-psud.fr
Universitry of Castilla la Mancha, UCLM	Femtoscience and single molecule microscopy	Spain	Douhal, Abderrazzak abderrazzak.douhal@uclm.es
Universidad del Pais Vasco and Donostia International Physics Center	Condensed Matter Physics www.ehu.es/	Spain	Echenique, Pedro wapetlap@ehu.es sqbsapod@ehu.es
Institut de Ciència de Materials de Barcelona- CSIC	Materials Magnètics i Òxids funcionals www.icmab.es/dmag/	Spain	Fontcuberta, Josep fontcuberta@icmab.es
Ecole Polytechnique Federale de Lausanne	Laboratory of Semiconductor Materials lmsc.epfl.ch	Switzerland	Fontcuberta, Anna anna.fontcuberta-morral@epfl.ch
Universidad de Granada	Nanoelectronics electronica.ugr.es	Spain	Gamiz, Francisco fgamiz@ugr.es
Fundación I+D en Nanotecnología (FideNa)	www.fidena.es	Spain	Garcia, Oscar info@fidena.es
Instituto de Cerámica y Vidrio-CSIC	Surface Plasmon in Nanostructures www.icv.csic.es/	Spain	García, Miguel Angel magarcia@icv.csic.es
Instituto de Microelectronica de Madrid - CSIC	Magnetic nanostructures and Magnetoplasmonics www.imm-cnm.csic.es	Spain	Garcia-Martin, Antonio antonio@imm.cnm.csic.es
International Centre of Biodynamics	www.biodyn.ro	Romania	Gheorghiu, Eugen egheorghiu@biodyn.ro
Nanotec Electronica	Nanotec Electronica www.nanotec.es/	Spain	Gil, Adriana adriana.gil@nanotec.es
Tyndall National Institute	Electronic Theory Group www.tyndall.ie	Ireland	Greer, Jim jim.greer@tyndall.ie
Dresden University of Technology	http://nano.tu-dresden.de/	Germany	Gutiérrez, Rafael rafael.gutierrez@tu-dresden.de
CEA	PTA www.pta-grenoble.fr	France	Haccart, Thibault thibault.haccart@cea.fr
CEA Grenoble	SiNaPS - Nano Silicon Lab. www-inac.cea.fr/	France	Hadji, Emmanuel emmanuel.hadji@cea.fr
CNRS	Laboratoire de Photonique et de Nanostructures www.lpn.cnrs.fr/en/Commun/	France	Harmand, Jean-Christ. jean-christophe.harmand@lpn.cnrs.fr
CSEM SA	CSEM Nanotechnology & Life Sciences www.csem.ch	Switzerland	Heinzelmann, Harry harry.heinzelmann@csem.ch
ETH Zurich	Micro and Nanosystems	Switzerland	Hierold, Christofer hierold@micro.mavt.ethz.ch

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Institution	Group / Web	Country	Contact Person / Email
CIC nanoGUNE Consolider	Nanooptics www.nanogune.eu	Spain	Hillenbrand, Rainer r.hillenbrand@ nanogune.eu
CIC nanoGUNE Consolider	Nanodevices www.nanogune.eu	Spain	Hueso, Luis l.hueso@nanogune.eu
Swedish Defence Reserach Agency FOI	Antennas and Electromagnetic Compatibility www.foi.se/FOI/templates/Page____7265.aspx	Sweden	Höijer, Magnus magnus@foi.se
University of Melbourne	Microanalytical Research Centre www.ph.unimelb.edu.au/~dnj	Australia	Jamieson, David d.jamieson @unimelb.edu.au
University of the Basque country	Solid state an materials chemistry	Spain	Jimenez, Dorleta djimenezdeab001 @ikasle.ehu.es
CNRS (Toulouse)	Nanoscience Group www.cemes.fr	France	Joachim, Christian joachim@cemes.fr
Bundeswehr University	Institute for Microelectronics and Circuits www.unibw.de/eit4_1	Germany	Jungemann, Christoph christoph.jungemann @unibw.de
Eberhard Karls Universität Tübingen	Nanostructures and Mesoscopic Physics www.uni-tuebingen.de/nano/index.html	Germany	Kern, Dieter dieter.kern @uni-tuebingen.de
Chalmers University of Technology	Division of Condensed Matter Theory www.chalmers.se	Sweden	Kinaret, Jari jari.kinaret@chalmers.se
Jacobs University Bremen	Theoretical Physics and Biophysics Group www.jacobs-university.de/ses/ukleinekathoefer	Germany	Kleinekathöfer, Ulrich u.kleinekathoefer @jacobs-university.de
Eindhoven University of Technology	Physics of Nanostructures www.fna.phys.tue.nl	Netherlands	Koopmans, Bert b.koopmans@tue.nl
University Paris Sud	IEF - Silicon-based photonics silicon-photonics.ief.u-psud.fr/	France	Laurent, Vivien laurent.vivien@u-psud.fr
Joined research team between THALES R&T and Ecole Polytechnique	Nanocarb	France	Legagneux, Pierre pierre.legagneux @thalesgroup.com
Fraunhofer Institute Material and Beam Technology IWS	www.iws.fraunhofer.de	Germany	Leson, Andreas birgit.schaub @iws.fraunhofer.de
CNRS	NanoBioSystems www.laas.fr/NBS/en/	France	Liviu, NICU nicu@laas.fr
Instituto de Ciencia de Materiales de Madrid	Photonic Crystals Group luxrerum.icmm.csic.es/	Spain	Lopez, Cefe cefe@icmm.csic.es
Universidad Complutense de Madrid	Aperiodic Structures in Condensed Matter	Spain	Macia, Enrique emaciaba@fis.ucm.es
University of Pisa	Nanoelectronics Group www.unipi.it/	Italy	Macucci, Massimo macucci @mercurio.iet.unipi.it
NANOTIMES	NanoTimes www.nanotimes.fr	France	Magoga, Michael gaston.nicolessi @nanotimes.fr

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Institution	Group / Web	Country	Contact Person / Email
CEA	Laboratory of Inorganic and Biological Chemistry inac.cea.fr/scib	France	Maldavi, Pascale pascale.maldivi@cea.fr
University of Minho	Physics of Nano-Crystalline Materials www.uminho.pt/	Portugal	Martín Sánchez, Javier javier.martin.nano @gmail.com
Parc de Recerca UAB	parc.uab.cat	Spain	Martinez, Ana Belén parc.recerca@uab.cat
Universidad de Salamanca	Semiconductor Devices Research Group www.usal.es/gelec/	Spain	Mateos, Javier javierm@usal.es
Fundacion CIDETEC	Nanotecnology Unit www.cidetec.es	Spain	Mecerreyes, David dmecerreyes@cidetec.es
University of Cambridge	EDM www-g.eng.cam.ac.uk/edm/	United Kingdom	Milne, Bill wim@eng.cam.ac.uk
Lund University	nano.lth.se	Sweden	Montelius, Lars fredrik.boxberg@ftf.lth.se
CIC nanoGUNE Consolider	nanobiotechnology www.nanogune.eu	Spain	Nabiev, Igor i.nabiev@naogune.eu
Universität Hamburg	Multifunctional Nanostructures www.physnet.uni-hamburg.de/institute/IAP/ Group_K/multifunctional_nanostructures.htm	Germany	Nielsch, Kornelius knielsch @physnet.uni-hamburg.de
University of Copenhagen	Mogens Brøndsted Nielsen (SINGLE project)	Denmark	Nielsen, Mogens mbn@kiku.dk
CSIC	Teoria y simulación de materiales www.icmm.csic.es/mnv/	Spain	Nieto Vesperinas, Man. mnieto@icmm.csic.es
Centro de Investigación en Nanociencia y Nanotecnología	Theory and Simulation www.cin2.es/groups/theory	Spain	Ordejon, Pablo pablo.ordejon@cin2.es
University of Copenhagen	NanoTheory www.nbi.ku.dk/paaske	Denmark	Paaske, Jens paaske@fys.ku.dk
CEA Saclay	Chemistry of Surfaces and Interfaces iramis.cea.fr/spcsi/index.php	France	Palacin, Serge serge.palacin@cea.fr
CNR Istituto Nanoscienze	www.nano.cnr.it/	Italy	Pellegrini, Vittorio vp@sns.it
Consejo Superior de Investigaciones Científicas	Nanofabrication and Functional Properties of Nanostructres www.imb-cnm.csic.es/index.php?option=com_	Spain	Perez-Murano, Francesc Francesc.Perez @imb-cnm.csic.es
CNRS	Unité Mixte de Physique CNRS/Thales www.trt.thalesgroup.com/ump-cnrs-thales/	France	Petroff, Frederic frederic.petroff @thalesgroup.com
Instituto de Microelectronica de Madrid	Molecular Beam Epitaxy www.imm-cnm.csic.es/mbe	Spain	Postigo, Pablo Aitor aitor@imm.cnm.csic.es
Johannes Gutenberg-Universität	Nanofibre Photonics and Quantum Optics www.quantum.physik.uni-mainz.de/ en/fibres/index.html	Germany	Rauschenbeutel, Arno arno.rauschenbeutel @uni-mainz.de

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Institution	Group / Web	Country	Contact Person / Email
Università del Salento	CMTG http://cmtg.unile.it/	Italy	Reggiani, Lino lino.reggiani@unisalento.it
CNR - IMM Institute for Microelectronic and Microsystems	Sensors and biosensors group www.imm.cnr.it	Italy	Rella, Roberto roberto.rella@le.imm.cnr.it
University of Regensburg	Mesoscopic Physics www.physik.uni-regensburg.de/forschung/richter/richter/	Germany	Richter, Klaus klaus.richter@physik.uni-r.de
IBM Research GmbH	Nanoscale Electronics www.zurich.ibm.com/	Switzerland	Riel, Heike hei@zurich.ibm.com
University of Cambridge	www-g.eng.cam.ac.uk/edm/	United Kingdom	Robertson, John jr@eng.cam.ac.uk
CEA	Atomistic Simulation Laboratory inac.cea.fr/L_Sim/	France	Roche, Stephan stephan.roche@cea.fr
Instituto de Ciencia de Materiales de Sevilla	Thin Film Engineering and Plasma Technology www.sincaf-icmse.es	Spain	Rodríguez Agustín arge@icmse.csic.es
UPV/EHU	Solid state and materials chemistry http://www.ehu.es/qi/	Spain	Rojo Aparicio, Teófilo teo.rojo@ehu.es
INRS	Nano(meter)-Femto(second) Laboratory www.nanofemtolab.qc.ca	Canada	Rosei, Federico rosei@emt.inrs.ca
Universidad del Pais Vasco	Nano-bio Spectroscopy Group and European Theoretical Spectroscopy Facility (ETSF) nano-bio.ehu.es/	Spain	Rubio, Angel angel.rubio@ehu.es
Universidad Autonoma de Madrid	MOLE-UAM www.uam.es/gruposinv/MoLE/	Spain	Sáenz Gutiérrez, J. José juanjo.saenz@uam.es
Institute for Bioengineering of Catalonia	Nanobioengineering group www.ibecbarcelona.eu/index.php?option=com_recerca&Itemid=1002&task=linia&ansubdepartments_id=20&dept_id=2	Spain	Samitier, Josep jsamitier@ub.edu
Lund University	The Nanometer Structure Consortium nano.lu.se	Sweden	Samuelson, Lars Lars.Samuelson@ftf.lth.se
CEA	SPSMS/Laboratory for Quantum Electronic Transport and Superconductivity inac.cea.fr/en/Phocea/Vie_des_labos/Ast/ast_visu.php?id_ast=208	France	Sanquer, Marc marc.sanquer@cea.fr
Sapienza University of Rome	EMC Lab http://w3.uniroma1.it/CNIS/CNIS/	Italy	Sarto, Maria Sabrina mariasabrina.sarto@uniroma1.it
UJF-CNRS-CEA	SPINTEC www.spintec.fr	France	Schuhl, Alain alain.schuhl@cea.fr
CEA	Laboratory for Innovative NAnophotonic systems (LINA) www.leti.fr	France	Segolene, Olivier segolene.olivier@cea.fr
Technische Universität Wien	www.iue.tuwien.ac.at/	Austria	Selberherr, Siegfried Selberherr@TUWien.ac.at
Università degli Studi di Udine	Nano Electronics www.diegm.uniud.it/selmi	Italy	Selmi, Luca luca.selmi@uniud.it

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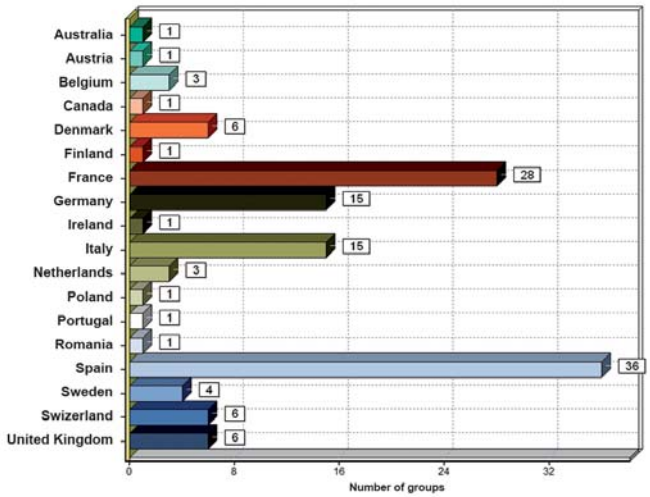
Institution	Group / Web	Country	Contact Person / Email
Instituto de Ciencia de Materiales de Madrid (CSIC)	Condensed Matter Theory www.icmm.csic.es/Teoria/	Spain	Serena, Pedro Amalio pedro.serena@icmm.csic.es
Universita di Roma	Università di Roma www.uniroma1.it/	Italy	Sibilia, Concita concita.sibilia@uniroma1.it
Institut Català de Nanotecnologia	The Phononic and Photonic Nanostructures Group (P2N) www.nanocat.org/	Spain	Sotomayor Torres, Clivia clivia.sotomayor@cin2.es
Jagiellonian University	NANOSAM www.if.uj.edu.pl/NANOSAM/	Poland	Szymonski, Marek ufszymon@cyf-kr.edu.pl
UNIVERSITY OF SALERNO	Lab of electromagnetic characterization of materials	Italy	TUCCI, Vincenzo vtucci@unisa.it
TUDelft	MED	Netherlands	van der Zant, Herre h.s.j.vanderzant@tudelft.nl
IMEC	Functional Nanosystems www.imec.be	Belgium	Van Roy, Wim vanroy@imec.be
Comissariat à Energie Atomique	Laboratoire dElectronique et des Technologies de lInformation www-leti.cea.fr	France	Viala, Bernard bernard.viala@cea.fr
Freie Universitaet Berlin	Theory of quantum transport www.physik.fu-berlin.de/en/einrichtungen/ag/ag-von-oppen/	Germany	von Oppen, Felix vonoppen_AT_physik.fu-berlin.de
Institute for Electronics Microelectronics and Nanotechnology	Molecular Nanostructures & Devices group ncm.iemn.univ-lille1.fr	France	Vuillaume, Dominique dominique.vuillaume@iemn.univ-lille1.fr
Forschungszentrum Juelich GmbH	Electronic Materials www.fz-juelich.de/iff	Germany	Waser, Rainer r.waser@fz-juelich.de
National Physical Laboratory	www.npl.co.uk	United Kingdom	Weaver, Paul paul.weaver@npl.co.uk
Ludwig-Maximilians-University	Nanomechanics Group nano.physik.uni-muenchen.de/nanomech	Germany	Weig, Eva weig@lmu.de
European Laboratory for Non Linear Spectroscopy	Optics of Complex Systems www.complexphotonics.org	Italy	Wiersma, Diederik wiersma@lens.unifi.it
Hitachi Europe Ltd	Hitachi Cambridge Laboratory www.hitachi-eu.com/r&d/rdcentres/Cambridge.pdf	United Kingdom	Williams, David Janice Jermy
Julius-Maximilians-Universität Würzburg	Nanoelectronics www.physik.uni-wuerzburg.de/institute_einrichtungen/physikalisches_institut/technische_physik	Germany	Worschech, Lukas worschech@physik.uni-wuerzburg.de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Belgium 3
Canada 1
Denmark 6
Finland 1
France 28
Germany 15
Ireland 1
Italy 15
Netherlands 3
Poland 1
Portugal 1
Romania 1
Spain 36
Sweden 4
Swizerland 6
United Kingdom 6
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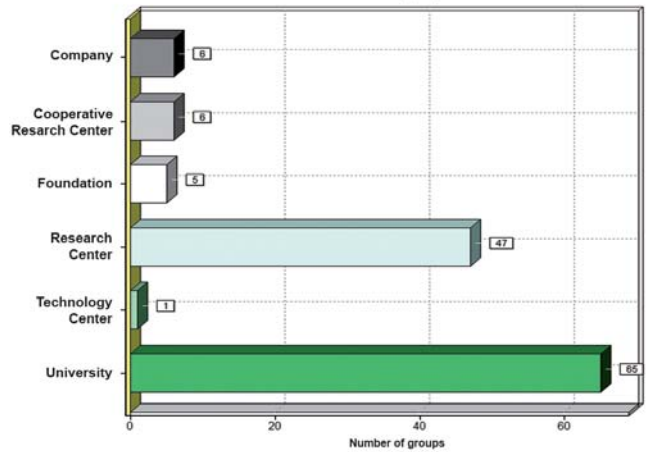
Number of groups


Groups/Institution
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Cooperative Resarch Center 6
Foundation 5
Research Center 47
Technology Center 1
University 65
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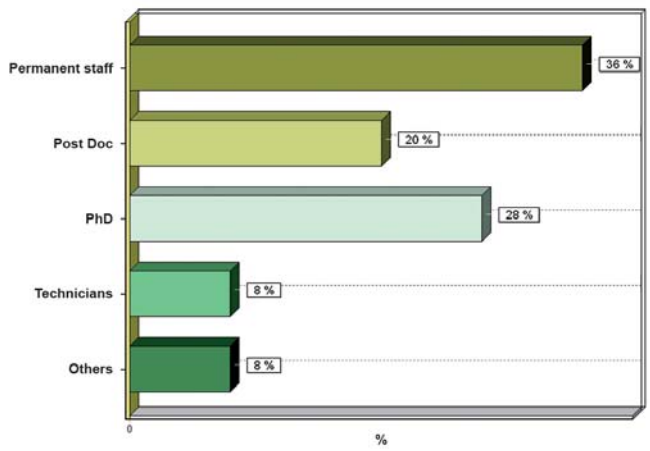
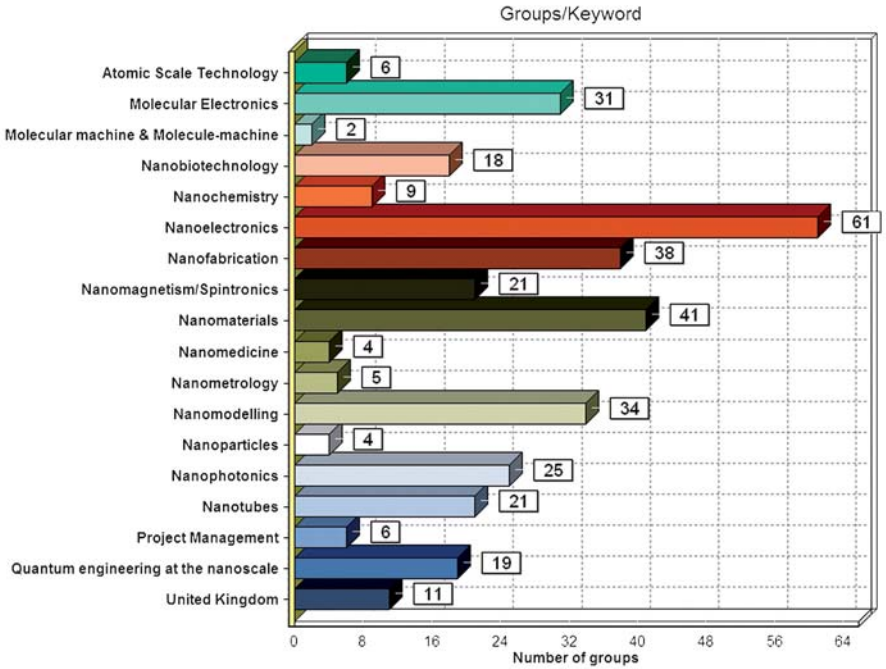
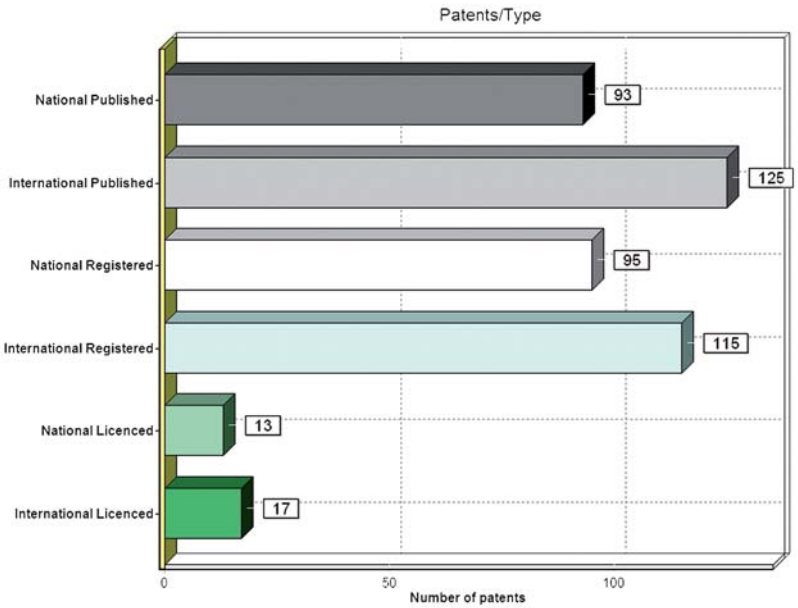
Number of groups


Personnel (Total number 2887)
Permanent staff 36 %
Post Doc 20 %
PhD 28 %
Technicians 8 %
Others 8 %
0
%



Groups/Keyword



Patents/Type

Notes

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www.nanoict.org