

Design of Semi-Metal Nanowire Transistor

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Abstract

Bandgap engineering in semimetal nanowires can be used to form a field effect transistor (FET) operating on a molecular length scale and eliminates one of the key obstacles to the manufacture of devices below 5 nm: the need for doping in a transistor's source and drain. For sufficiently small wire diameters the metallic behaviour of the semimetal is lost and a bandgap is induced. Using a full quantum mechanical description of the semimetal nanowires, we were able to demonstrate the design of a dopant-free, monomaterial confinement modulated gap transistors (CMGT).

Nanowire FETs enable the continuation of the Moore's law for future technology generations, by enabling higher device density and consequently high function per integrated circuit at lower unit cost. Critically, use of nanowire transistors permit efficient electrostatic control over charges in the nanowires to allow for low power nanoelectronics, that are now required at the heart of all mobile applications such as smart phones and tablets. For the very small length scales that we consider, even 2 or 3 dopant atoms within the nanowire corresponds to extremely high doping concentration, and since there are only few dopant atoms available, the very concept of a *pn* junction breaks down. Recently, the introduction of a single carrier type in the source, channel, and drain regions of nanowire-like structures led to the demonstration of junctionless nanowire transistors (JNTs) [1]. This design offers one of the few competitive solutions to engineer out difficulties related to aggressive scaling of the traditional (bulk or nano-engineered) MOSFETs; physical operation of these transistors with a gate length as small as 3 nm has been theoretically and experimentally studied [2,3]. In JNTs, variability issues due to the formation of *pn* junctions are avoided. For channels with sub-5 nm lengths, the number of semiconductor atoms in the channel and source/drain regions for semiconductor nanowires is typically on the order of a few hundred to thousand and introduction of even a few dopant atoms introduces extremely high doping levels. Another limitation at this length scale arises the decoupling of dopant levels from the energy bands (due to confinement) which suppresses dopant activation [2,4].

Difficulties with the doping of nanowire structures and the drawbacks associated with energy bandgaps increasing with decreasing diameter can be avoided. Using a full quantum mechanical description of the semimetal nanowires, it is demonstrated that on the length scale on which a semimetal-semiconductor transition occurs, bandgap engineering allows for the formation of a field-effect transistor while eliminating the need for doping. The resulting proposal for a transistor design, the confinement modulated gap transistor (CMGT), follows by forming the source, channel and drain regions using atoms of a single element, unlike in conventional MOSFETs which require dopant atoms to define different device regions. The electronic and electrical properties of the channel are engineered by varying the nanowire cross-section to achieve modulation of the band gap energy along the wire's axis. This creates metallic source and drain regions and a semiconducting channel. For the length scales we are interested in, we demonstrate this is readily achievable using semimetal nanowires.

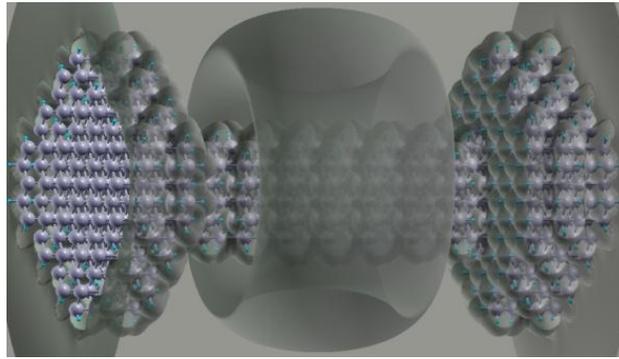
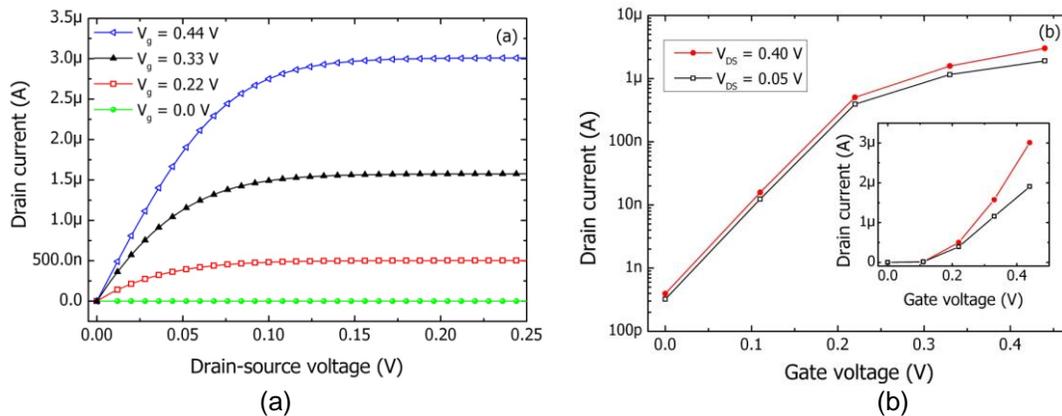


Figure 1- Atomic scale illustration of CMGT implemented using α -tin. The ring around the channel region indicates an isopotential surface due to the applied gate bias.

The model CMGT is comprised of 1 nm diameter SnNW and physical gate length of $L_g = 2.3$ nm. It should be noted that the physical channel length in the off-state is approximately 4.1 nm as estimated from the local density of states. The oxide isolating the channel from the gate electrode is modelled as a continuum characterised by 1 nm hafnium oxide thickness and a dielectric constant of $\epsilon_{\text{HfO}_2} \sim 25$. Note these dimensions were chosen for computational ease, and similar device structures at larger critical dimensions with different wire orientations and materials can be achieved. The predicted current-voltage characteristics from *ab initio* simulation are shown in figure 2, with the prediction of extremely good turn-off characteristics in a gate-all-around configuration [5].



Acknowledgments

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