ENHANCED COMPETITIVENESS OF SLOWER ELECTRON BEAM LITHOGRAPHY PROCESSES AT THE NANOSCALE AS A CONSEQUENCE OF SHOT NOISE CONSIDERATIONS

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A large number of high resolution lithography techniques have been developed over the past three decades based on the use of a focused and controlled electron beam for patterning. Typically, the mechanism for patterning involves the scission of polymer bonds by the incident electrons, or the reticulation of monomers to form large molecular weight polymers. Much work has been carried out to develop high sensitivity processes in order to improve the speed of overall pattern writing and thus increase the pattern area that can be exposed within a reasonable time. In recent years, the focus of research has been on chemically amplified resists (CAR) that provide extremely high sensitivity and which are now commonly used for patterning photomasks in the semiconductor industry.

Fundamental shot noise effects are involved in almost all aspects of the electron beam lithography (EBL) process. These arise at the source of electrons, in the interaction of the electrons with the resist and in the propagation of the acids in the CAR. For nanoscale patterns (10 nm and less), shot noise effects impose severe limitations for writing patterns that meet minimum criteria for edge roughness (typically expected to be less than 10% of the linewidth), and for proper filling of the exposed patterns. Furthermore, the current trend of new EBL systems, namely moving from 50 keV to 100 keV electron beam energies in high throughput systems, actually increases the effects of shot noise.

A shot noise model has been elaborated that is based on an optimal resist development approach and the model will be discussed in detail. Modeling results indicate that high sensitivity resists such as CARs are completely unsuitable for patterning at the 10nm scale since minimum sensitivities on the order of $1mC/cm^2$ are required for proper patterning of features <10nm. This sensitivity is almost three orders of magnitude beyond the requirements stated in the International Technology Roadmap for Semiconductors. However, several companies are currently developing lithography systems which make use of massively parallel electron beams (MPEB), with several proposed systems having ~10 000 beams operating at beam currents near 1nA. This makes it possible to use less sensitive EBL processes that have the potential for producing patterns <10nm in size while still maintaining respectable pattern writing times. Among these, results will be shown for a new technique to produce gold nanoparticles ranging in size from 3 to 15 nm by using EBL on thin-films of gold complexes on silicon surfaces (fig.1). This technique has a demonstrated sensitivity in the range where it might be practical to produce nanoscale features in a manufacturing environment using MPEB systems. Other low sensitivity techniques previously reported and which possess interesting properties, such as conformal coating for patterning nanostructures on non-planar substrates (fig. 2), will be revisited as they may offer high potential for use with MPEB systems at feature sizes <10nm. These approaches will be put into context of results obtained by many other groups over the past decades who have developed electron beam lithography techniques that had sensitivities too low to be deemed practical in manufacturing at the time.

Figures

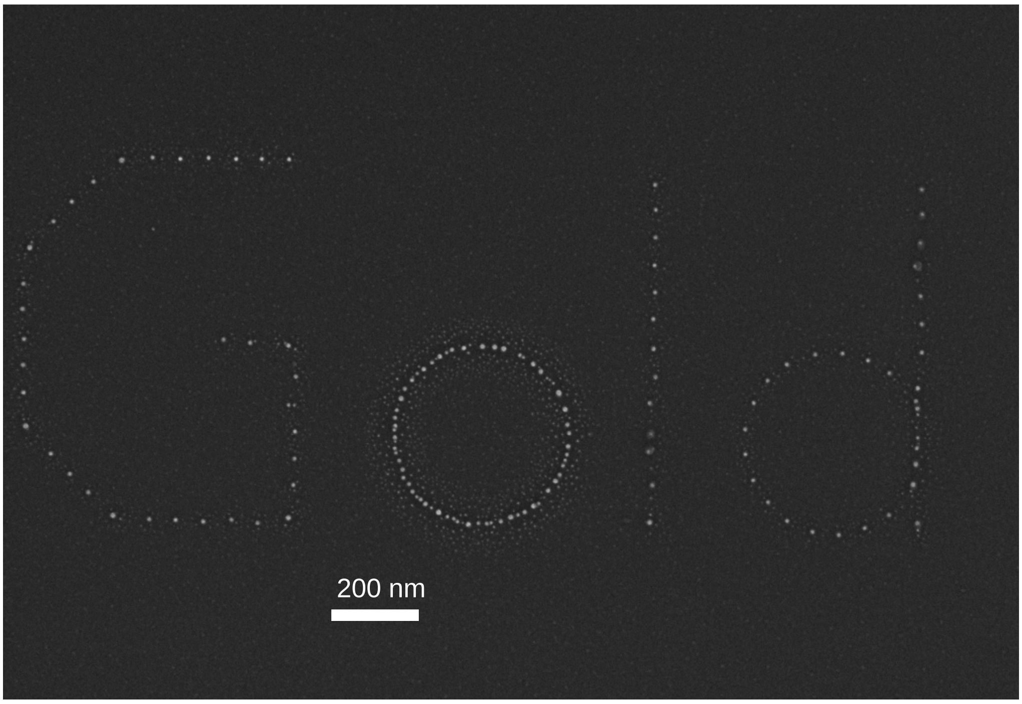

Figure 1: Gold nanoparticles patterned using EBL on thin-films of gold complexes on a silicon surface

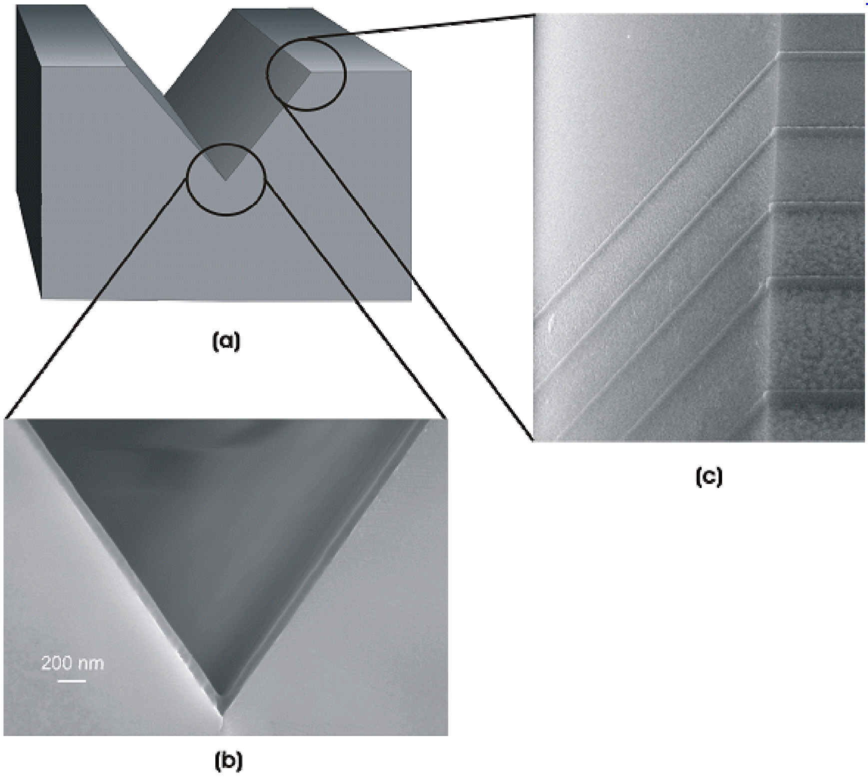

Figure 2: High resolution resist pattern obtained by EBL over non-planar substrate (silicon v-groove)