NONOVERLAP SOURCE/DRAIN-TO-GATE NANO-CMOS STRUCTURE FOR LOW LEAKAGE DRAM DESIGN

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In order to scale CMOS devices to smaller dimensions while maintaining good control over the short-channel effect, the gate oxide thickness needs to be reduced in close proportion to the channel length [1]. With the reduction of oxide thickness, the gate-induced drain leakage (GIDL) increases exponentially by high gate-to-drain electric field due to an imperfect optimization of the gate-to-drain structure [2]. To achieve good retention time property in DRAM, low cell leakage current is essential [3], [4].

We propose the source/drain-to-gate nonoverlap Nano-CMOS structure and optimize DRAM cell transistor structure. We show GIDL can be suppressed in this structure by adjusting nonoverlap region to reduce drain-to-gate electric field.

To reduce the GIDL current, we simulated the nonoverlap source/drain-to-gate structure shown in Fig.1 using SILVACO. In this structure, the wide nonoverlap region formed by spacer suppresses the electric field in the drain edge. Using the oxide spacer, the nonoverlap length (L_{no}) is adjusted. The gate electric field at the gate corner induces an inversion layer in the source/drain-to-gate nonoverlap region and that makes the transistor work [5]. The source and drain is medium doped for junction leakage suppression.

The structure in Fig.1 shows good switching property for DRAM cell transistor in the simulation results. Suppression of the threshold voltage variation is shown in Fig.2. Comparing the threshold voltage difference between T_{ox} = 40Å and T_{ox} = 60Å, more abruptly increasing threshold voltage is found in the structure with thicker oxide, and all structures show less threshold voltage changes in the nonoverlap region. Improvement of subthreshold slope appears in Fig.3 as the nonoverlap region increases. This result shows nonoverlap structure is effective in suppressing short channel effect. The reason is this structure has larger metallurgical gate length than conventional MOS structure in the same physical gate length, the channel in the drain side has less effect to the whole channel.

The simulation result about I_{on}/I_{off} is shown in Fig.4 with various nonoverlap lengths. Enhanced I_{on}/I_{off} ratio is expected from the result in Fig.2, Fig.3 and low GIDL current property of this structure. We have found that the maximum I_{on}/I_{off} ratio is achieved at the nonoverlap region and the I_{on}/I_{off} ratio at the optimum region is increased more than 50 times of the ratio at the overlapped region. The maximum ratio is found at the point of 90nm gate length and 15nm nonoverlap length. The prediction of the optimum point is the key technique in DRAM design using the nonoverlap source/drain-to-gate structure to reduce cell leakage.

In conclusion, this study shows the nonoverlap source/drain-to-gate Nano-CMOS structure is suitable for future DRAM cell transistor because this structure has extremely low leakage current and high I_{on}/I_{off} current ratio. Moreover, the nonoverlap source/drain-to-gate Nano-CMOS structure shows more process tolerance on the threshold voltage in Fig.2.

References:

[1] R. H. Dennard, et al., IEEE J. Solid-State Circuits, **SSC-9** (1974) 256.
[2] O. Semenov, et al.,IEEE Trans. Semiconductor Manufacturing, **15** (2002) 9.
[3] Minchen Chang, et al., IEEE Trans. Electron Devices, **50** (2003) 1036.
[4] Ja-Hao Chen, et al., IEEE Trans. Electron Devices, **48** (2001) 1400.
[5] Hyunjin Lee, et al., IEEE Trans. Nanotechnology, **1** (2002) 219.

Figures:

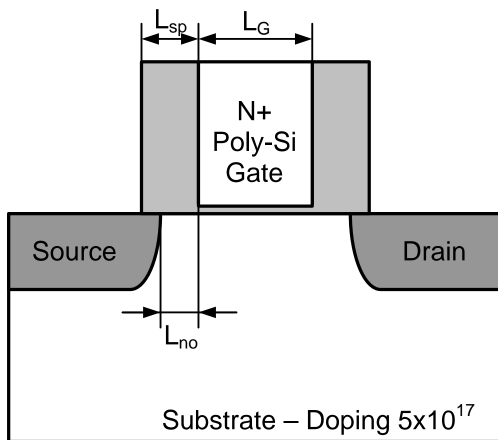

Fig. 1 Schematic of the simulated MOS structure.

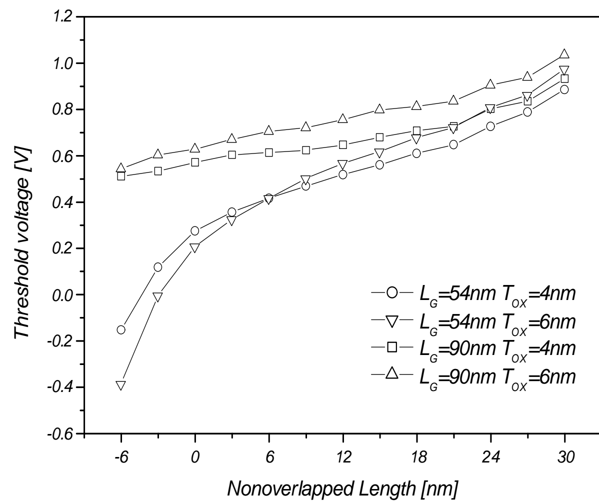

Fig. 2 Threshold voltage, V_{th} versus nonoverlap length, L_{no} with various gate oxide thicknesses, T_{ox} and physical gate lengths, L_G.

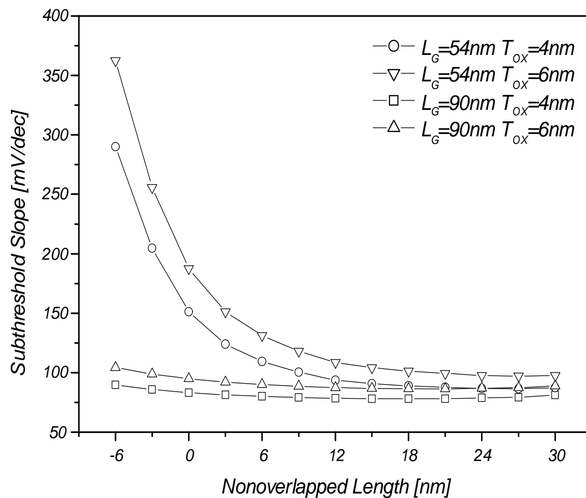

Fig. 3 Subthreshold slope versus nonoverlap length, L_{no} with various gate oxide thicknesses, T_{ox} and physical gate lengths, L_G.

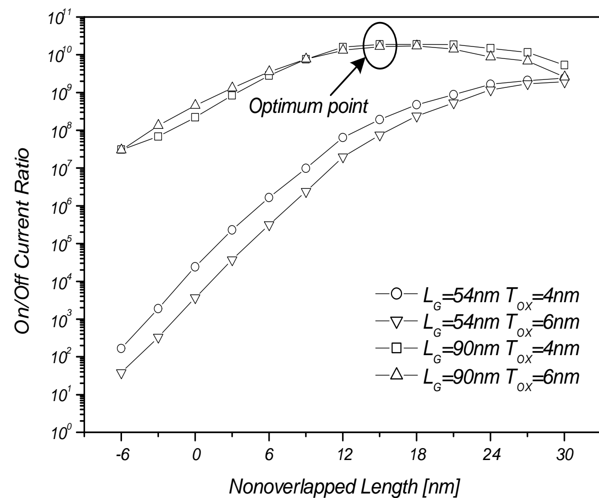

Fig. 4 On/Off Current Ratio versus nonoverlap length, L_{no} with various gate oxide thicknesses, T_{ox} and physical gate lengths, L_G. The optimum point is observed at L_G=90nm, L_{no}=15nm.