CHARACTERIZATION OF SILICON NANOWIRE FABRICATED BY AFM LITHOGRAPHY ON ULTRATHINNED SOI SAMPLE

N. Rochdi, D. Tonneau, H. Dallaporta, J. Gautier, V. Safarov, M. Vinet
CRMCN, Faculté des Sciences de Luminy, Case 913, 13288 Marseille cedex 09, France
Contact : rochdi@crmcn.univ-mrs.fr

AFM lithography is a very friendly-use lithography technique to fabricate rapidly silicon nanowires. The technique is based on a two-step process of oxide mask generation on a passivated silicon sample under an AFM probe, followed by a step of wet etching of silicon selectively regarding SiO_2. The silicon local oxidation occurs via an anodisation process by application of a negative bias to the conducting tip of the AFM. In fact the resulting high tip-sample electric field drives the oxidation species in the water meniscus linking tip to sample, towards the silicon surface. A great number of papers have already been published on the oxide mask generation and the mechanisms involved in the oxide growth are quite well-known [1,2]. It has been demonstrated that 10 nm oxide lines or dots can be fabricated by this technique.

Starting from SOI sample, it is possible to generate silicon nanowires whose width and thickness are limited respectively by the lithography process performance and by the thickness of the silicon top layer of the SOI sample [3]. We have worked on mildly doped SOI samples (2.10^{17} cm^{-3}) thinned down to 8 nm, provided by CEA-LETI. After optimisation of the lithography process, connected silicon nanowires of 60 nm width are currently obtained, when the AFM operates in non-contact mode (figure 1). The back silicon template can be used as a gate (backgate in the following).

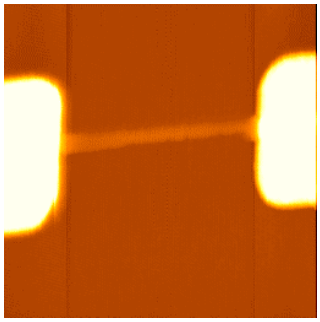

Fig1. AFM image of a connected nanowire W = 100 nm, h = 8 nm (N = 2.10^{17} cm^{-3})

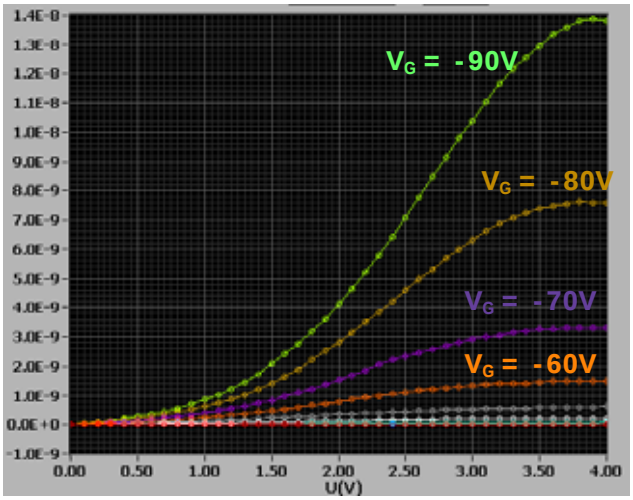

Fig2. Drain courant Vs drain source voltage for different values of backgate voltage.

At such low thicknesses, the behaviour of the silicon nanowires exhibited strange electrical characteristics [4,5]; for instance, figure 2 presents drain courant vs drain source voltage for different values of backgate voltages, these characteristics (done at room temperature) are similar to those of a conventional field effect transistor, nevertheless the device could conduct for either positive and negative backgate voltages.

IV measurements highlighted a progressive decrease of the drain source current while repeating the same measurement many times. This phenomenon is attributed to some charge trapping at the Si/SiO_2 interface, which reduces the depletion of the very thin (8 nm) channel.

Polarizing the backgate alternatively by negative then by positive bias restores the level of drain source current (figure 3), by evacuation of the charges.

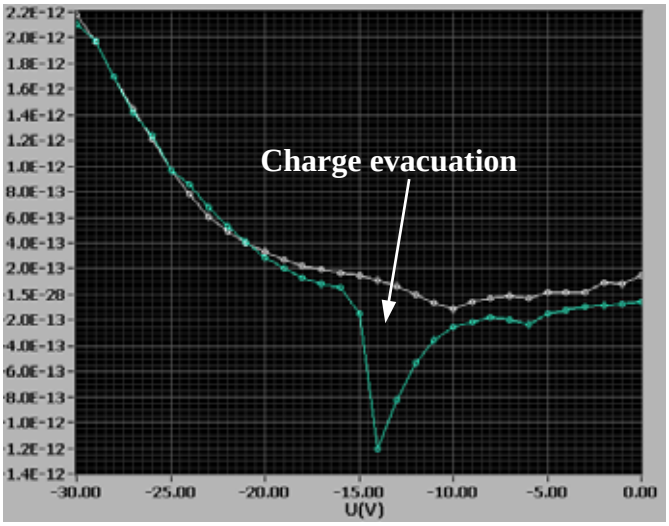

Fig3. Drain courant Vs backgate voltage at Vds = 50 mV.

In addition, we herewith enclose one of the preliminary results of Coulomb blockade at low temperature (figure 4), this figure presenting the drain courant vs the backgate voltage at Vds = 60 mV (T = 4.5 K) shows some characteristic peaks, corresponding to the one-by-one electron transfer.

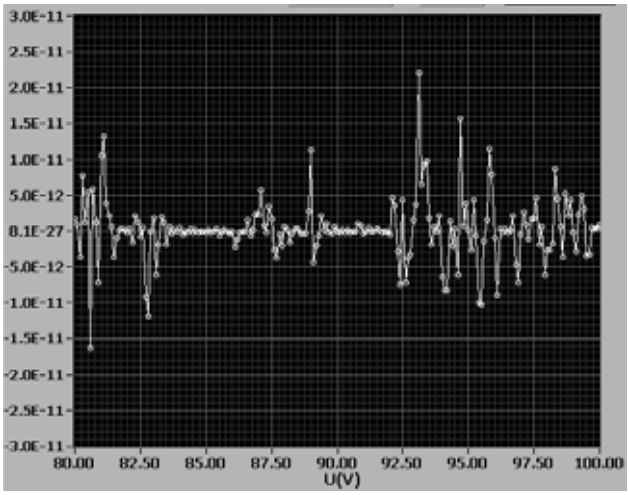

Fig4. Drain courant Vs backgate voltage at Vds = 60 mV at very low temperature, T = 4.5K.

[1].F. Marchi, V. Bouchiat, H. Dallaporta, V. Safarov, D. Tonneau, J. Vac. Sci. Technol. B16(6), 2952-2956 (1998).
[2].N. Clement, D.Tonneau, B.Gely, H. Dallaporta and V. Safarov, J. Gautier, J. Vac. Sci. Technol. B 21(6), 2348-2351 (2003).
[3]. N. Clément, D. Tonneau, H. Dallaporta, V. Bouchiat D. Fraboulet, D. Mariole, J. Gautier and V. Safarov, Physica E, Vol. 13, 999-1002, (2002).
[4]. N. Clément, A. Francinelli, D. Tonneau, H. Dallaporta, F. Jandard, D. Fraboulet, J. Gautier V. Safarov, Appl. Phys. Lett., 82(11), 1727-1729 (2003).
[5]. A. Francinelli, D. Tonneau, N. Clément, H.Abed, F.Jandard, H. Dallaporta, V.Safarov, Appl. Phys. Lett., 85(22), 5272-5274 (2004).