Electrical Characterization of Carbon Nanofiber Arrays for On-chip Interconnect Applications

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On-chip interconnects fabricated using copper damascene technology have provided the performance necessary to keep pace with the International Technology Roadmap for Semiconductors (ITRS) [1] since the adoption of copper as a replacement for aluminum-based wiring schemes. As microelectronics moves towards the 45 nm node and beyond, however, a multitude of factors provide a formidable challenge for the science and engineering community. Issues such as reliability under high current stress, and high resistivity due to enhanced electron scattering processes at small dimensions provide the motivation for new on-chip interconnect material development. Carbon-based nanostructures such as carbon nanotubes (CNTs) and carbon nanofibers (CNFs) have been shown to possess outstanding electrical [2-4], thermal [5-7], and mechanical [8-9] properties suitable for on-chip interconnect integration schemes.

This work presents a critical evaluation of both the reliability and resistivity of carbon nanofiber structures as they apply to interconnect systems. A model system for the work presented here is shown in figure 1. A free-standing, vertically aligned CNF array is grown by plasma enhanced chemical vapor deposition (PECVD) [10] as shown in figure 1 (a), and is subsequently gap-filled with SiO_2 and subjected to chemical mechanical polishing [11] as shown in figure 1 (b). Figure 1 (c) shows the microstructural characteristics of a single as-grown CNF investigated by transmission electron microscopy (TEM). Initial electrical testing performed on single CNFs show the metallic behavior of our plasma-grown nanofibers at room temperature (figure 2). Stress tests performed at room temperature indicate the robustness of the CNF array, as shown in figure 3. The inset of figure 3 shows the I-V characteristics of the array after approximately 180 hours of high current density stress ($1x10^7$ A/cm^2), showing no degradation of the ohmic behavior. Similar measurements conducted at elevated temperatures exhibited the same characteristics. In addition to the outstanding reliability demonstrated by the CNF array, low temperature measurements were performed to elucidate their fundamental electron transport processes. The low-temperature conductance of the CNF array (figure 4) can be explained by examining transport processes at low temperatures of pure basal plane graphite, where the conductance monotonically increases with respect to temperature. At temperatures above 180K, the material behaves as a metallic conductor, exhibiting a low temperature coefficient of resistance (TCR).

Fundamental measurements of temperature-dependent conductance and reliability of carbon nanofiber array structures have been investigated. The results of these studies demonstrate progress towards the possible integration of these carbon-based nanostructures into next-generation ultra-large scale integrated (ULSI) on-chip interconnect schemes. While the preliminary electrical measurements demonstrate the viability of this material for interconnect applications, further work is required to eliminate integration issues before such structures are implemented.