

## Full-wafer stencils fabricated by a DUV/MEMS process for high-throughput patterning of mesoscopic structures

M.A.F. van den Boogaart, G.M. Kim<sup>\*</sup>, R. Pellens<sup>\*\*</sup>, J-P. v/d Heuvel<sup>\*\*</sup>, L.M. Doeswijk, and J. Brugger

Microsystems Laboratory (LMIS1)

Swiss Federal Institute of Technology (EPFL), 1015 Lausanne, Switzerland

E-mail: marc.vandenboogaart@epfl.ch

<sup>\*\*</sup> ASML Special Applications, De Run 6501, 5504 DR Veldhoven, The Netherlands

Photoresist-based lithography has major limitations when applied to micro-electro-mechanical systems (MEMS) with mechanically fragile and/or chemically functionalised surfaces. As a remedy, alternative, complementary nanopatterning methods have been developed, e.g. thermo-mechanical indentation (nanoimprint lithography), local printing of molecular layers (soft lithography), and shadow-mask deposition (nanostencil patterning). The nanostencil method is a resistless patterning method based on direct, local deposition of material on an arbitrary surface through a solid-state silicon nitride (SiN) membrane. In addition, the method offers the possibility of simultaneous deposition of micrometer and nanometer scale structures. Patterning of such mesoscopic structures ( $10^{-9}$  -  $10^{-5}$  m) through stencils fabricated by MEMS processes in combination with focused ion beam (FIB) milling has been demonstrated within a limited area.<sup>1,2</sup>

In order to produce larger membranes enabling increased throughput of the nanostencil method, we developed a 100-mm wafer-scale (deep-UV) DUV/MEMS fabrication process. The mesoscopic patterns were first defined by a 4× reduced projection exposure using an ASML wafer stepper and then transferred into a SiN layer by means of reactive ion etching (RIE). The membranes were released by wafer-through etching using potassium hydroxide (KOH). Figure 1 shows the mid-process details of 200 nm DUV patterns after the RIE transfer into the 500-nm thick SiN layer. Furthermore, Figure 1 shows the resulting full-wafer stencil (100 mm) consisting of various membranes, each containing numerous geometrical apertures. Patterning of nano-scale structures using stencils allows for a large choice of materials and surfaces to be nanopatterned since no etch steps need to be applied. We have studied the nanopatterning of metals (Al, Au, Bi, and Cr) on various surfaces (silicon, oxides, freestanding SiN cantilevers, and self-assembled monolayers (SAM)) for different mesoscopic experiments. Deposition of a 150-nm thick Al layer through a stencil and the resulting structure are shown in Figure 2. We will present details on the DUV/MEMS process and the application of the full-wafer stencil for specific applications such as templates for molecular electronics, nano-mechanical devices with a 90 MHz resonance frequency<sup>3</sup>, as well as nano-scale Hall-sensor devices.<sup>4</sup>

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<sup>\*</sup> Present address: School of Mechanical Engineering, Kyungpook National University, Daegu, South Korea

<sup>1</sup> M. M Deshmukh, D. C. Ralph, M. Thomas, J. Silcox, Applied Physics Letters 75 (1999) 1631-1633

<sup>2</sup> G. M. Kim, M. A. F. van den Boogaart, J. Brugger, Microelectronic Engineering 67-68 (2003), 609-614

<sup>3</sup> G. M. Kim, M. A. F. van den Boogaart, S. Kawai, H. Kawakatsu, J. Brugger, Transducers 2003, conference proceedings vol 1, Boston. (see TNT2004 conference abstract by D. Grogg)

<sup>4</sup> See TNT2004 conference abstract by S. Mouaziz

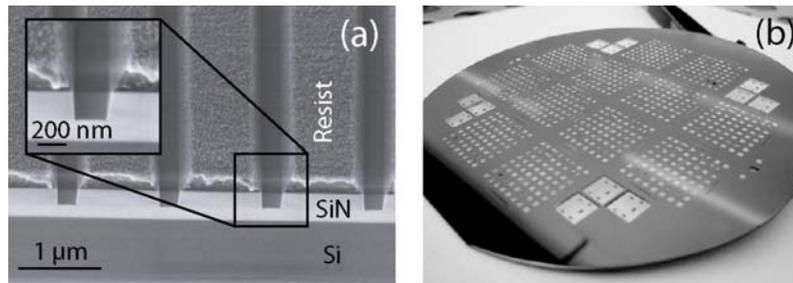


Figure 1: Process detail of the DUV pattern transfer and a full wafer stencil. (a) Mid-process details showing 200-nm pattern profile etched into 500-nm thick SiN. This confirms the high accuracy and selectivity of the RIE transfer process at this length-scale. (b) A full-wafer scale stencil (100 mm) consisting of various membranes, each containing numerous geometrical apertures.

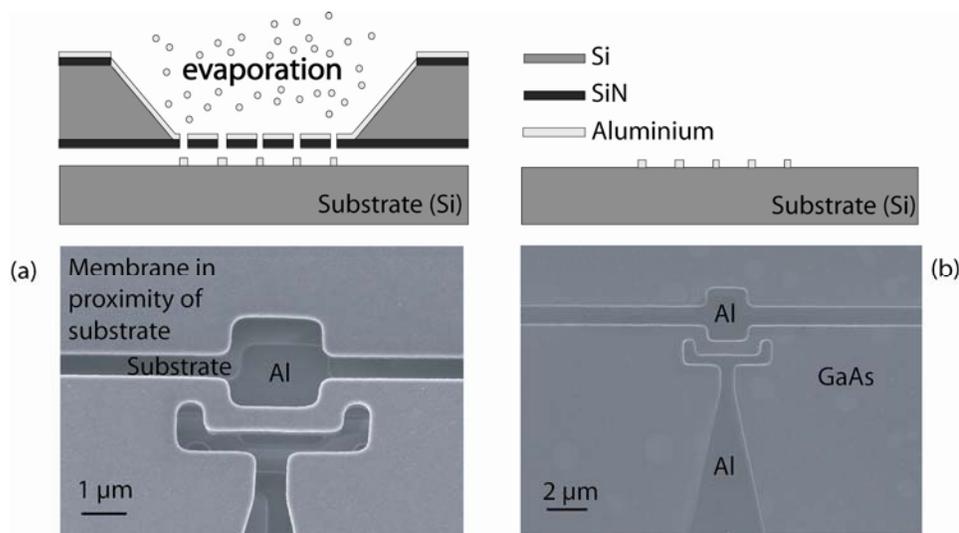


Figure 2: Deposition process using a stencil. (a) The stencil is placed in contact or in close proximity to the substrate and a material is evaporated through the apertures in the membrane. The SEM image shows a stencil mask with a gap of less than  $1\ \mu\text{m}$  to the substrate (GaAs in this case) after evaporation of 150 nm Al. (b) The stencil is removed from the substrate. The SEM image shows the resulting Al structures.