Top and back gate single-wall carbon nanotube transistors by rapid growth chemical vapour deposition method

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The remarkable electronic and mechanical properties of carbon nanotubes have generated an intense interest in their deposition methods over the past few years. For electronic device applications, a fast and 'clean' growth method for SWCNTs without the presence of amorphous carbon (a-C) is essential. In this work, a novel approach based on high temperature (1000°C) and rapid growth (~5s of acetylene, C_2H_2) is used to achieve high quality SWCNTs without a-C. Using a triple-layer thin film of Al/Fe/Mo (with Fe as a catalyst) on an oxidized Si substrate, the sample is exposed to a single short burst (5s) of acetylene at 1000^{o}C. This produced a high yield of very well graphitised SWCNTs, as confirmed by transmission electron microscopy and Raman spectroscopy. The rapid growth process allows us to achieve a clean, amorphous carbon (a-C) free deposition which is important for SWCNT device fabrication. The absence of a-C is confirmed by Auger Electron Spectroscopy, Raman spectroscopy and electrical measurements. By patterning the thin film catalyst, selective growth of SWNT at pre-defined locations on the Si substrate is achieved enabling the fabrication of top and back gate SWCNT transistors. The top gate transistors were formed by contacting the ends of the SWNT (source-drain), covering the SWNT with gate oxide, then putting gate metal on top (Fig. 1). The yield and electrical measurements of these transistors at room temperature will be discussed.

References:

[1] R. G. Lacerda et al., Appl. Phys. Lett. 84, 269 (2004).

Figures:

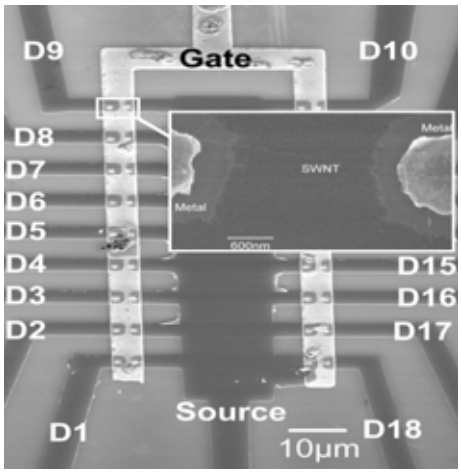

Figure 1 - Top gate transistor array