Physics-based model of ballistic silicon nanowire transistors

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To scale MOSFETs below 10 nm, efficient gate control is required. For this reason, silicon nanowires, which allow multi-gate or surrounding-gate transistors are being explored. Recent numerical studies demonstrated that silicon nanowire transistors (SNWTs) shows promise (e.g., better electrostatic scaling for a given Si body thickness) and may provide a manufacturable opportunity to scale silicon transistors down below the scaling limit of planar MOSFETs. Compared with planar double-gate MOSFETs, SNWTs may offer better gate control, simpler fabrication, and more flexibility in device design [1]. In this work we propose a simple physics-based model for the cylindrical SNWT. The silicon channel in this structure is covered by a cylindrical surrounding-gate electrode, providing an excellent control of Short-Channel Effects (SCEs), [Fig. 1]. The small vertical electric field and the use of undoped silicon channels in these structures reduce the surface and Coulomb's scattering [2], being the electronic transport close to the ballistic regime. To account for the electrostatics the Poisson's equation is exaclty solved along the radial direction. The current is obtained by means of the Landauer transmission theory [3-6]. The proposed model captures the static current-voltage characteristics in all the operation regimes, below and above the threshold voltage, for low and high temperatures, incorporating effects of multi-subband conduction, and taking into account the band structure of silicon. As an illustrative example of the capability of this physics-based model we show in Fig. 2 the simulated transconductance and conductance of a cylindrical SNWT with a gate oxide of 1.5 nm, a silicon film thickness of 3 nm working at low temperature (to highlight one-dimensional subbands effects).

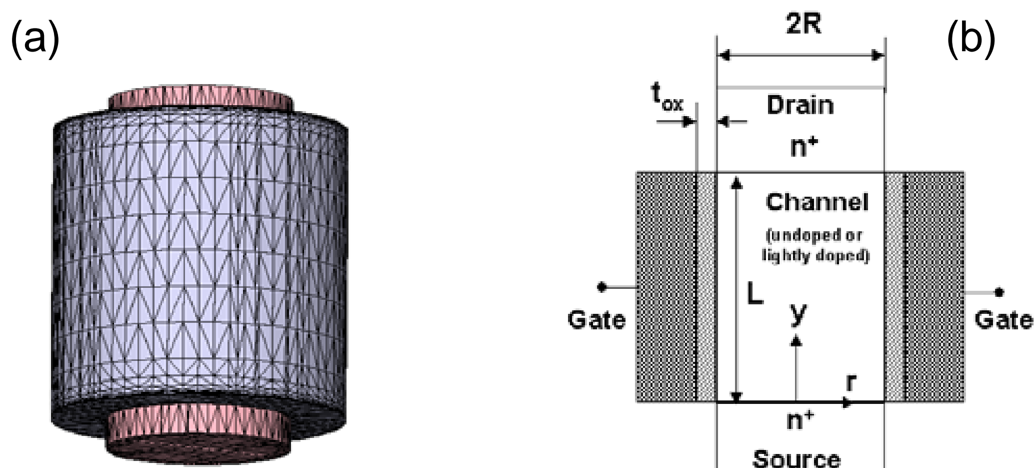

Figure 1. (a) Geometry of the cylindrical silicon nanowire transistor, (b) cross-section.

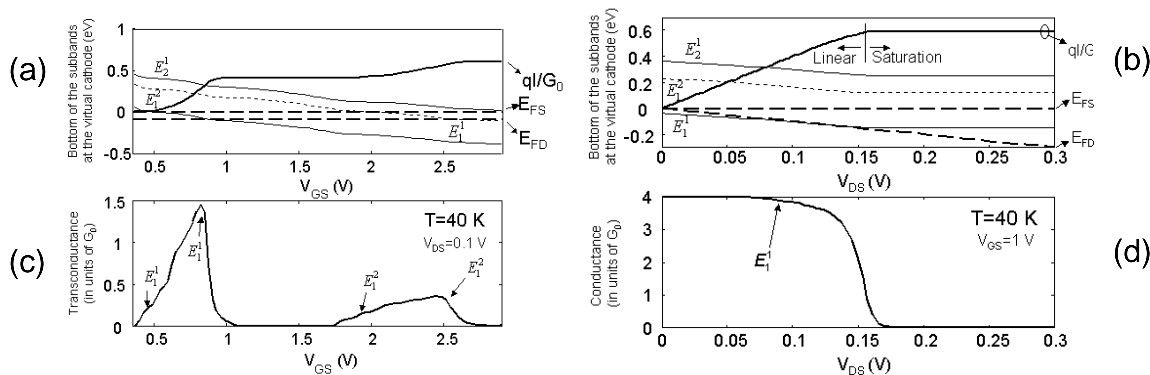

Figure 2. (a)-(b) Bottom of the subbands at the top of the barrier (virtual cathode) versus the gate (drain) voltage. The thin solid and dashed lines represent the bottom of the subbands from the first and second set of valleys, respectively. The Fermi level at the source (E_{FS}) is taken as a reference. In (c)-(d) we plot the simulated transconductance (conductance), showing a clear structure of peaks and valleys at the positions where subbands cross the source and drain Fermi levels.

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