Poster

SIZE AND LOCALISATION EXTRACTIONS OF SILICON NANO-CRYSTALS USING ELECTRICAL APPROACHES

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In the objective to turn the limit of the downscaling away, novel structures have to be imagined, fabricated and optimized. In the field of the Non Volatile Memory devices, a solution consists in replacing the continuous Si-poly floating gate by a planar distribution of Silicon nanocrystals (Si-nc), the Si-nc acting as a storage node[1] (fig.1). In this kind of devices an improvement of reliability, plus a read/write process at moderate voltage are expected.

The aims of this work is to determine both the position and the size dispersion of the Si-nc embedded in the gate oxide of a MOS structure using two original electrical approaches [2][3]. The size dispersion is investigated by measuring the quasi-static current flowing across the tunnel barrier (2-3nm) which separates the Si-nc layer from the conduction channel of a MOS capacitor. The charging effects of the Si-nc with electrons is clearly evidenced by the presence of an excess current in the strong inversion regime. In this paper, we show that the excess current can be explained by a model involving the granular shape of the floating gate. A good agreement between experimental data and theory is obtained by specifying a size distribution of the Si-nc (fig.2). On the other side, the dispersion in position of the Si-nc from the channel is revealed by Low Frequency Noise (LFN) measurements performed on MOSFET devices. In the presence of Si-nc in the oxide, a deviation of the 1/f behavior is observed on the drain current power spectral density, S_{id}. The frequency dependence can be explained by a model which incorporates a distribution of traps in the gate oxide (fig.3). A Gaussian function is used to represent the distribution of the Si-nc in the oxide. The position of the maximum of the Gaussian well agrees with the technological parameters i.e. the tunnel oxide thickness, t_{nc}, which separates the Si-nc layer from the conduction channel. The Full Width Half Maximum (FWHM) of the Gaussian has been adjusted to fit the spectra. We discuss the FWHM by the dispersion in position of the Si-nc around an average value designed by t_{nc}. In conclusion, we propose two efficient and specific electrical methods to extract both the dispersion in position and size of Si-nc embedded in the gate oxide of a MOS Structure.

References:

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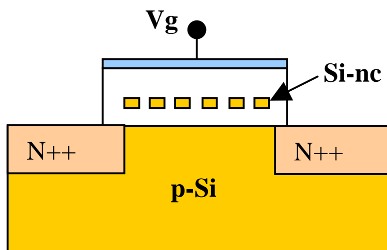

Fig. 1: Cross sectional view of a Non Volatile Memory device with Si-nc acting as a floating gate.

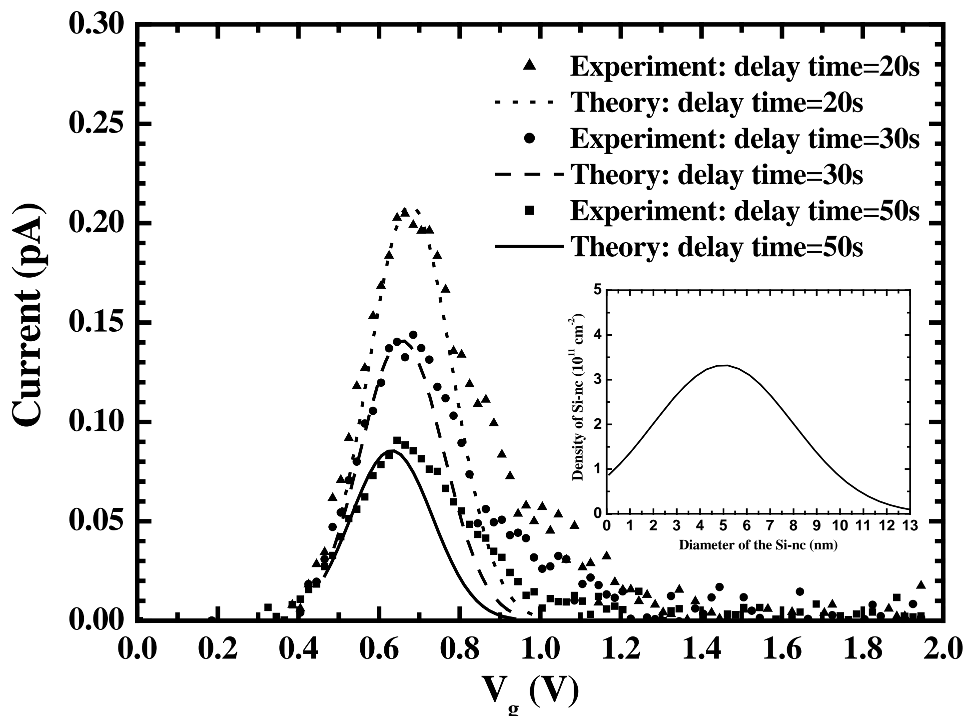

Fig. 2: Theory-experiment comparisons of the quasi-static current flowing across the tunnel barrier separating the Si-nc layer from the channel of conduction. The inset represents the distribution of the density of Si-nc versus their diameter which was used to fit the experimental data.

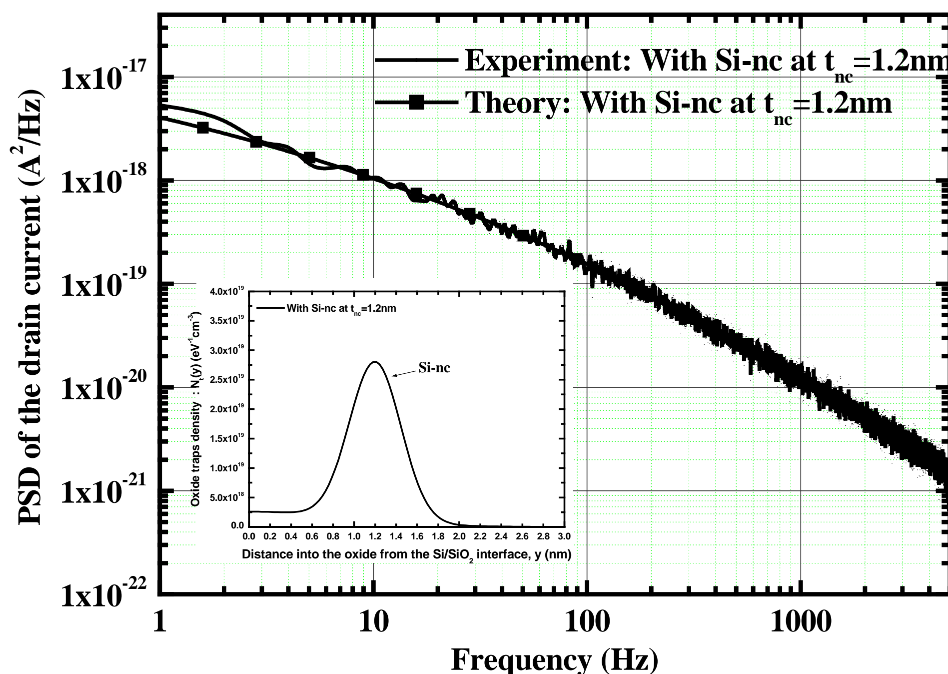

Fig. 3: Theory-experiment comparison of the PSD of drain current fluctuations. The model uses the distribution of the traps density in the gate oxide (incorporating the Si-nc) as shown in the inset. The data were taken at Id=90µA.