CONDUCTIVE ATOMIC FORCE MICROSCOPY FOR CHARACTERIZATION OF HIGH-K DIELECTRICS

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The thickness decrease of the SiO_2 used as the gate oxide of MOS devices has become one of the main showstoppers of the microelectronic scaling down process, due to a dramatic increase of leakage currents and a decrease in lifetime[1]. The use of an alternative material with a higher dielectric constant (high-K) has been proposed to replace SiO_2 as the gate dielectric, because High-K materials will allow to reach the required equivalent oxide thickness (EOT), but with a larger physical oxide thickness, which reduces the leakage current drastically. Most of the knowledge about the electrical behavior of high-k materials has been gained from measurements performed on macroscopic MOS capacitors or transistors[2,3,4] using standard electrical characterization methods at wafer level. This kind of tests, however, provides a spatially averaged information on the electrical properties of the material. On the contrary, Conductive Atomic Force Microscopy (CAFM), as demonstrated for SiO_2[5], is able to characterize the gate dielectric at a nanometer scale.

In this work the CAFM has been used to: a) Study the dependence on the post deposition annealing temperature (T_A) of the electrical properties of a $HfAlO_x$ /SiO_2 gate stack with EOT<2nm. The wafers were annealed in N_2 for 1 min at different temperatures, ranging from 700C to 1000C. Some of the wafers were not exposed to annealing, to keep them as reference. b) Study the electrical degradation and dielectric breakdown (BD) of a HfO_2 /SiO_2 gate stack with EOT<1.5nm, when different electrical tests are applied. In both cases p-type Silicon is used as substrate.

Fig.1. shows the current maps obtained for $HfAlO_x$ reference samples (not annealed) (a) and samples annealed at 900C (b), with an applied sample voltage of 6V (substrate injection) in a $2\times2\mu m^2$ region. For $T_A\geq900C$ the average current and electrical roughness are about 10 times larger. The increase in inhomogeneity is believed to be caused by the material transition from an amorphous to a poly-(nano)crystalline structure, as evidenced also in TEM measurements (not shown) for samples annealed above 800C.

To study the electrical degradation and BD of the HfO_2/SiO_2 stack, ramped voltage stresses (RVS) were applied at different locations of the stack. For RVS from 0 up to 15V (substrate injection) topography (fig.2.a and b) and current (fig.2.c) maps exhibit modifications: at the RVS locations topography hillocks have appeared and their conductivity has dramatically increased, indicating that BD has happened. This kind of behavior is analogous to that observed on SiO_2 layers after their BD[5]. The hillock height ranges from ~1nm up to ~6nm being the average 2.1nm, and has been found to be related to BD voltage. Statistically speaking, the larger the BD voltage, the higher the hillock height. As for SiO_2, the hillock height can be an indicator of structural BD damage caused to the stack. The observed hillocks can probably be the result of a combination of real structural modifications of the stack plus an extra deflection of the CAFM tip due to charge generated during BD.

To sum up, CAFM has been successfully used for characterization of several high-k/SiO_2 stacks at the nanoscale. In particular: (a) It has revealed the different electrical behaviors of samples annealed at different temperatures. Larger currents and conduction inhomogeneity

are observed above the high-k material crystallization temperature. (b) BD spots in HfO_2/SiO_2 stacks have been observed for the first time. As for SiO_2, the BD of the stack leads to modifications in the topography images and high conductive spots in the current images. The height of the hillocks has been considered an indicator of structural damage.

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Figures:

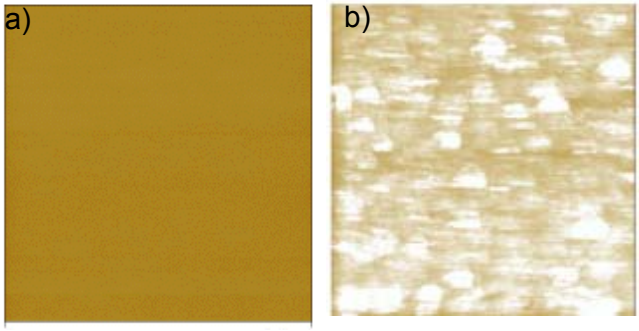

Fig. 1. Current maps of the gate stacks measured when applying a sample bias of 6V (substrate injection), a) not annealed sample, b) T_A=900C. The area of the scanned region is $2\times2\mu m^2$. The current ranges from 0pA (black) to 20pA (white).

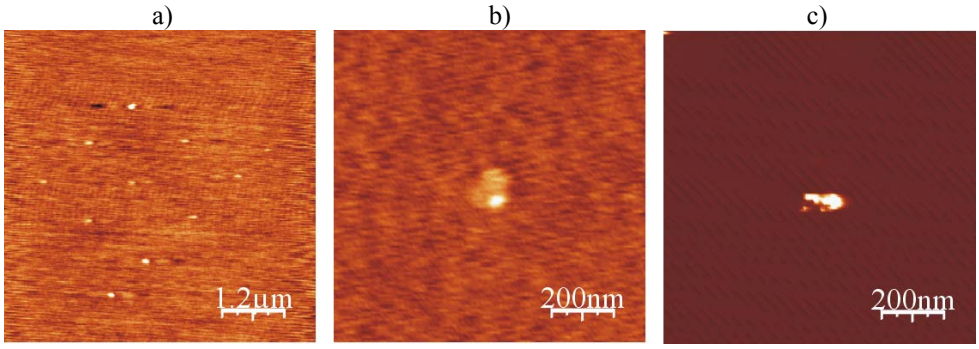

Figure 2. a) Topography map showing 10 hillocks measured at the location where RVS (0V up to 15V) were previously applied. Hillock height ranges from 1 to 6 nm. b)Topography and c) current maps (V_{gate}=3V) corresponding to a zoom of one of the hillocks observed in a). Height range is from 0 (black) up to 6nm (white). Current range is from 100fA (noise level) (black) up to 300pA (white).