Self-Aligned Single-Electron Memories

SASEM Project (IST-2001-32674)

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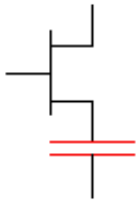
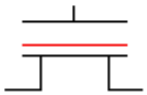
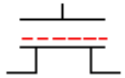
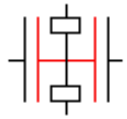
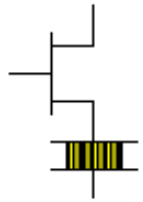
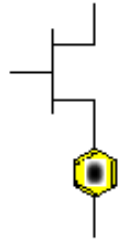
Introduction

Emerging Research Memory Devices

	Present Day Baseline Technologies		*Phase Change Memory**	*Floating Body DRAM*	*Nano-floating Gate Memory***	*Single/Few Electron Memories***	*Insulator Resistance Change Memory***	*Molecular Memories***
Storage Mechanism								
Device Types	DRAM	NOR Flash	OUM	1TDRAM	Engineered tunnel barrier or nanocrystal	SET	MIM	Bi-stable switch
Availability	2004	2004	~2006	~2006	>2006	>2007	~2010	>2010

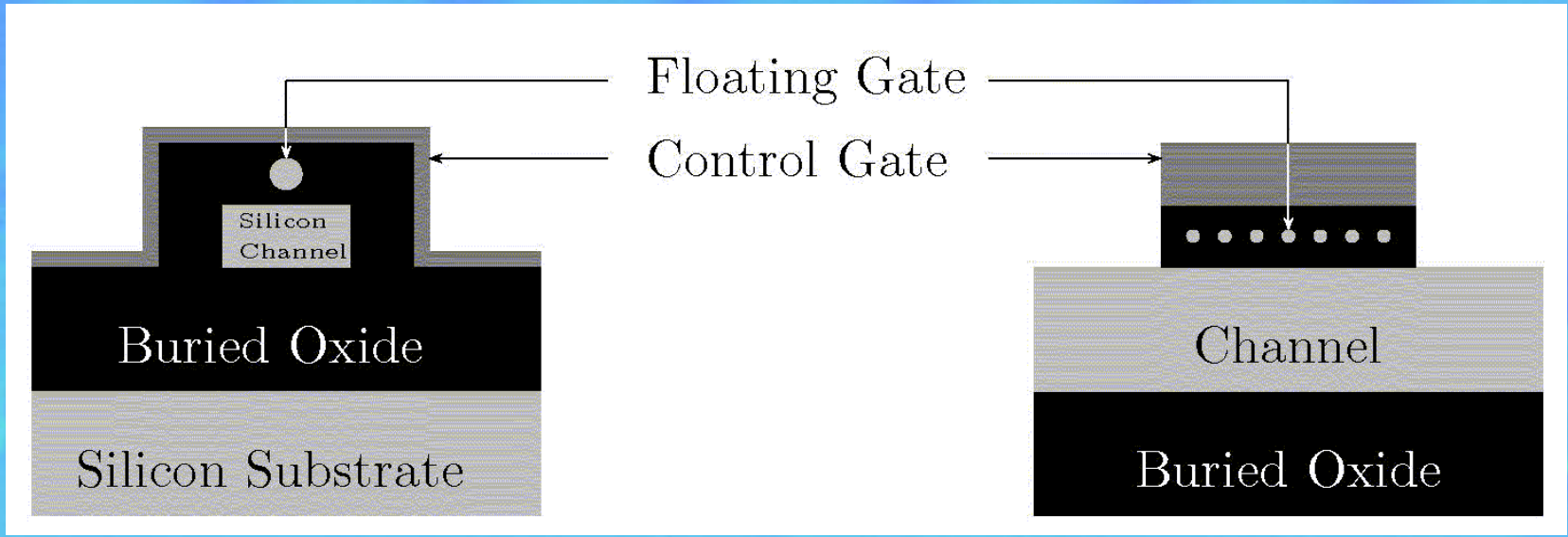
SASEM device: **S**elf **A**ligned **S**ingle **E**lectron **M**emory

According to international technology roadmap for semiconductors, single-electron memory devices are considered as an emerging research memory devices. *A strong theme is to merge each of these memory options into a CMOS technology platform in a seamless manner.*SASEM Device is compatible with CMOS technology.

ITRS-ROADMAP 2003 edition: emerging research device

Introduction

Two main approaches have been proposed to fabricate single-electron memories: multiple-dot and single-dot devices.



Single-dot devices are composed of a narrow MOSFET channel with a single nano-floating gate embedded in the gate oxide.

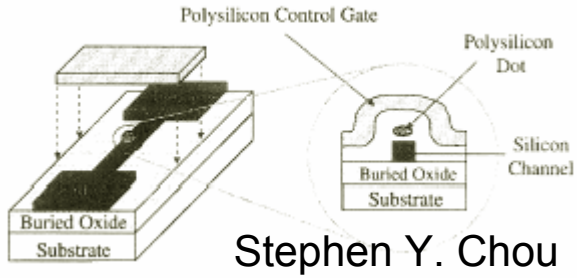
Key technological issue: to fabricate the nano-floating gate by lithography and to align it to the channel in a controlled manner.

The large number of dots implies that these devices are intrinsically not single-electron devices, but each dot stores only one or a few electrons depending on its size.

-Nano dots: Si, Ge or metal.

-- Tunnel oxide: SiO_2, Si_3N_4, Al_2O_3, organic insulator, …

Introduction



Stephen Y. Chou

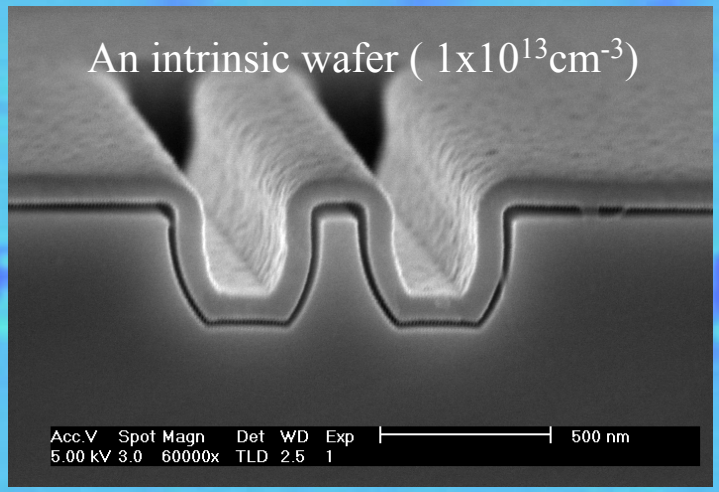
- **To our knowledge, there are only four papers related to Si single-dot floating gate memory devices, probably because of the difficulty of their realization.**
- **All of them were realized by very high-resolution lithography tool to define the floating gate and the channel.**
- **In the SASEM project, we presented a new single-dot memory device which can be realized by current state-of-the-art optical lithography tools (minimum size: 100 nm).**
- **Moreover, the floating gate is self-aligned to the channel, and the whole structure is formed in a single oxidation step.**

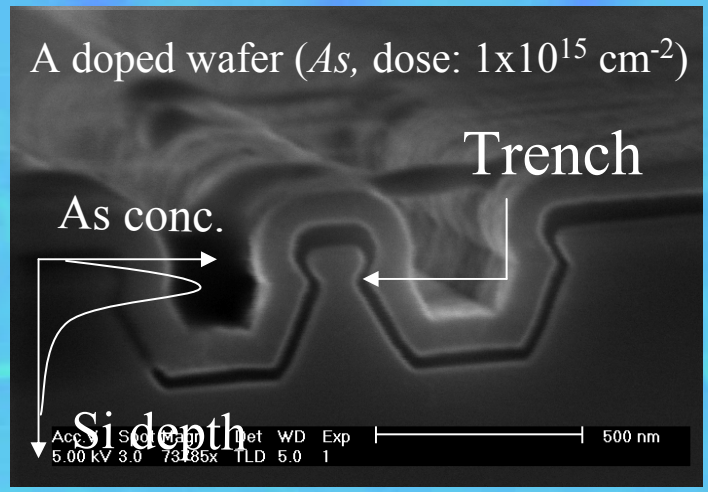
Fabrication

Arsenic-assisted etching effect:

A trench is formed at the sidewalls of As-doped silicon pillar.

The trenches are located in the region of As peak concentration.



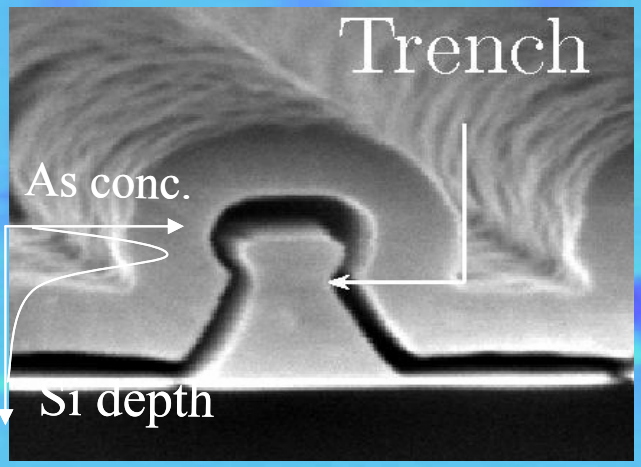


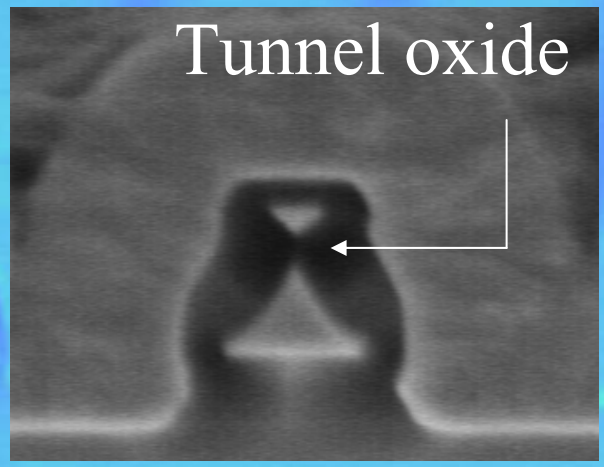
Silicon etch rate depends on the doping type of the silicon substrate. Heavily As-doped silicon (n-type) is etched faster than intrinsic silicon, which is etched faster than heavily B-doped silicon (p-type). When arsenic is implanted in the silicon substrate, with peak concentration several orders of magnitude larger than the background concentration, the silicon lateral etch rate is the fastest in the region of arsenic peak concentration.

Fabrication

Arsenic-assisted oxidation effect:

The tunnel oxide is formed in the trench region.



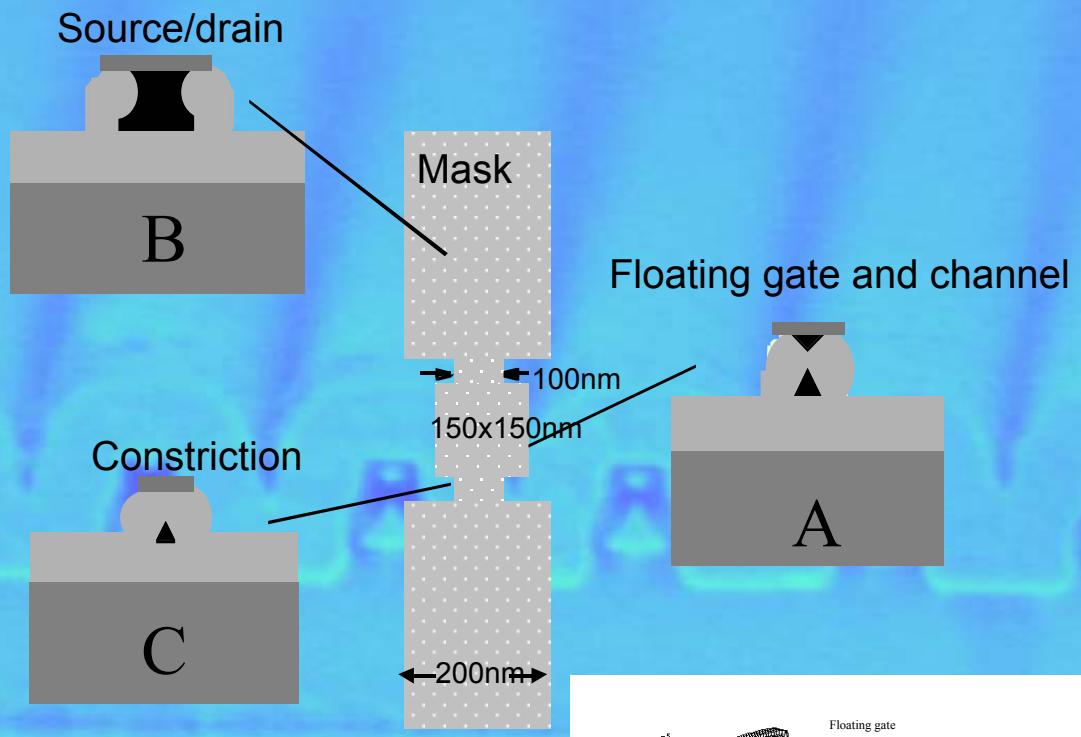


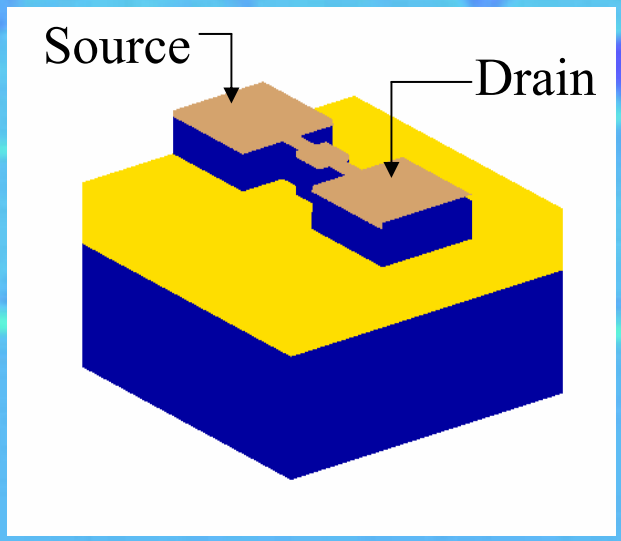
The silicon oxidation rate reaches the maximal in the region of As peak concentration. As a result, silicon pillar is separated into a large bottom wire and a small top wire. The top wire and bottom wire can be used as the flating gate and the channel of the flash memory device by means of an appropriate layout.

Fabrication

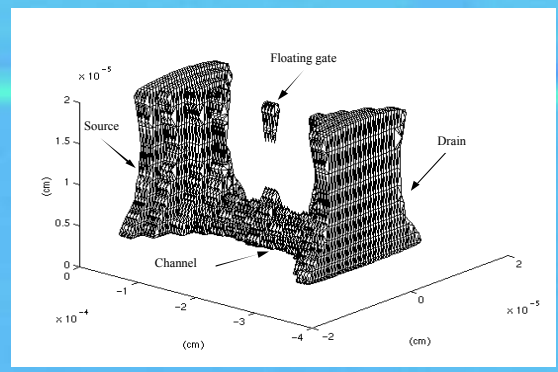
Layout:

Central region: 150X150nm^2
Constriction width: 100nm
Silicon thickness: 200nm



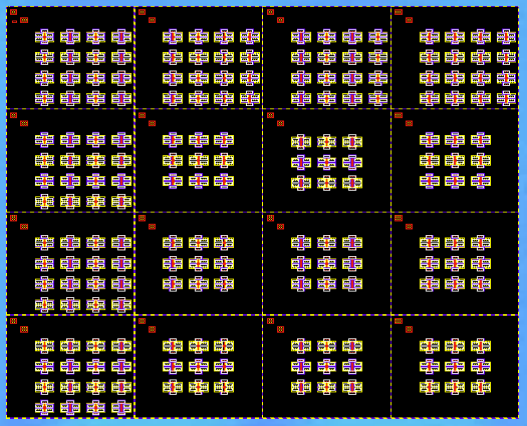


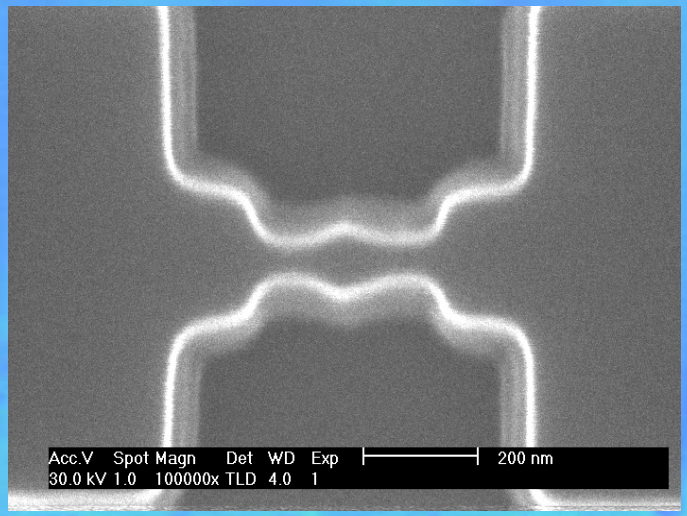
The floating gate is restricted to the central region due to the presence of constrictions.



Experimental results

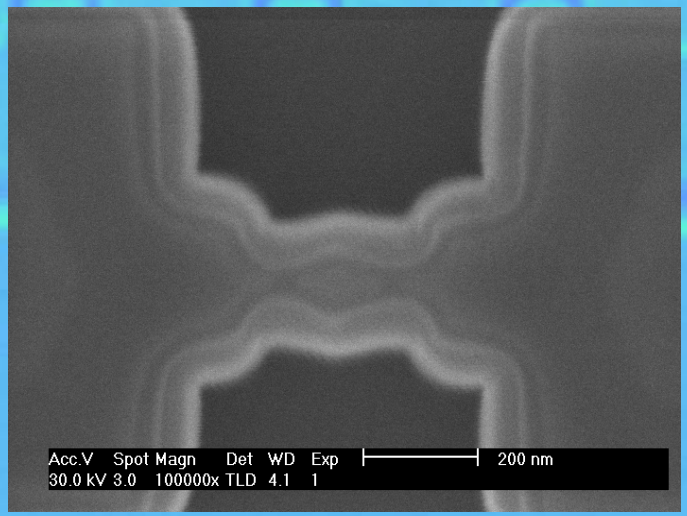
Fabrication



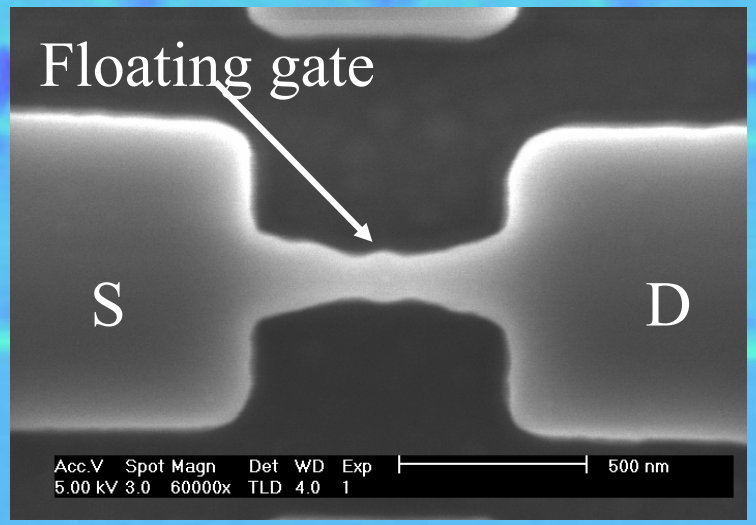


Memory device before oxidation

Mix and match lithography is used to decrease the exposure time and to increase device throughput.



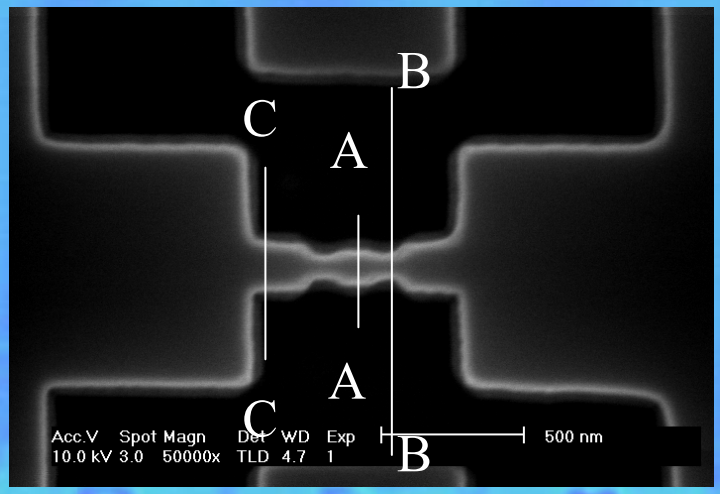
Memory device ofter oxidation

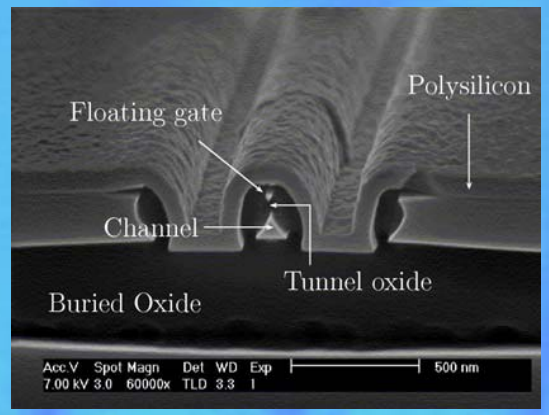


The same device after oxidation, a large dot can be seen in picture through the gate insulator.

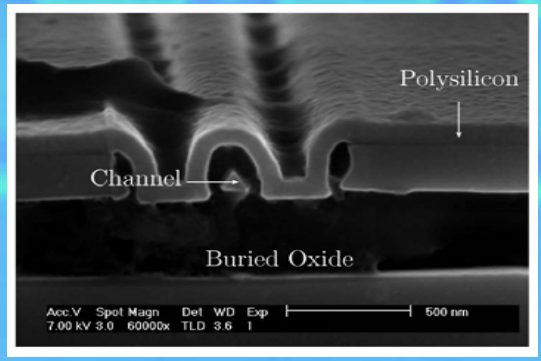
Fabrication

Experimental results

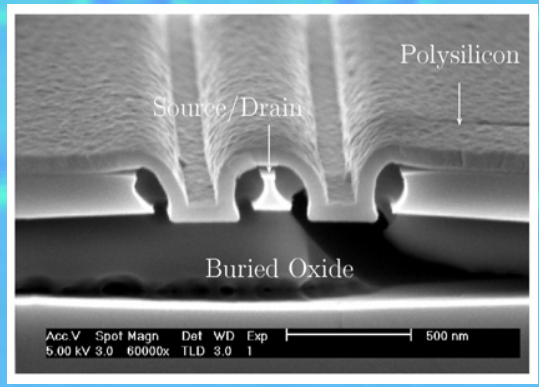




Cross-section along AA: the tunnel oxide separating top wire from the bottom wire.



Cross-section along BB: top wire is completely oxidized .

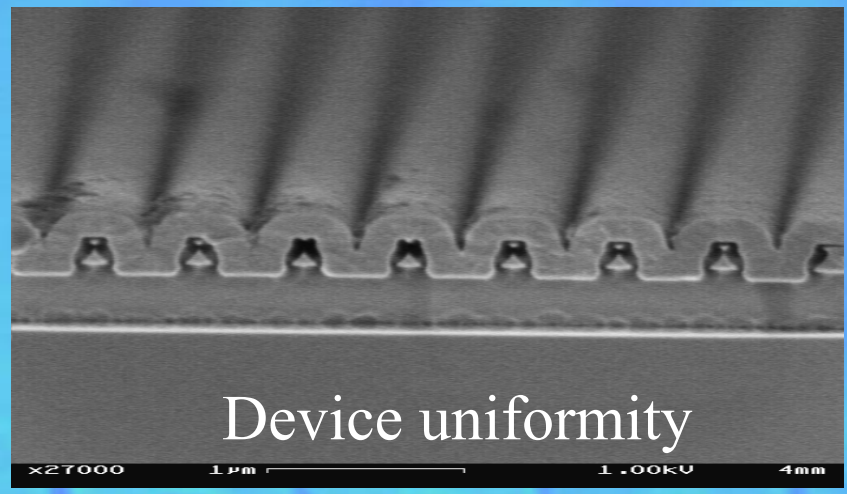


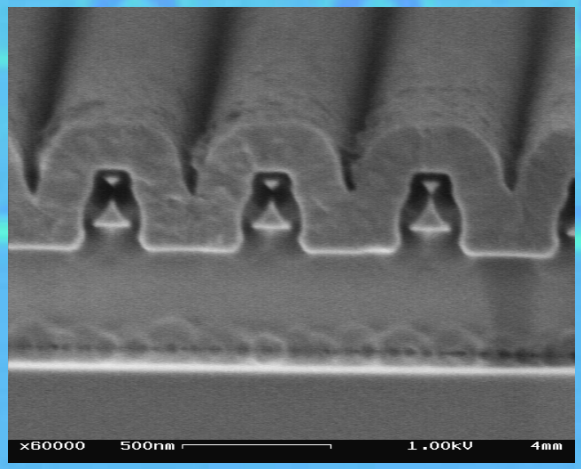
Cross-section along CC: the larger width avoiding the formation of the tunnel oxide.

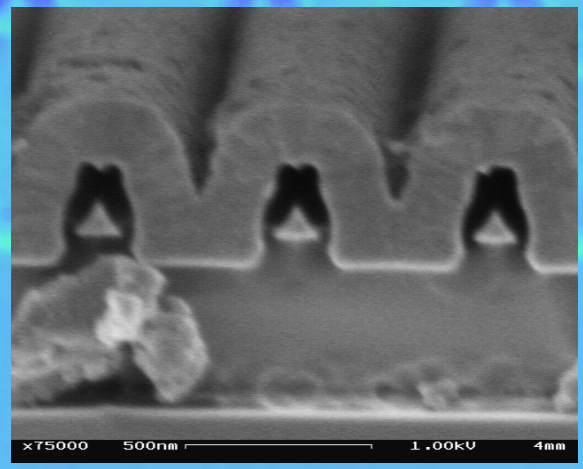
Fabrication

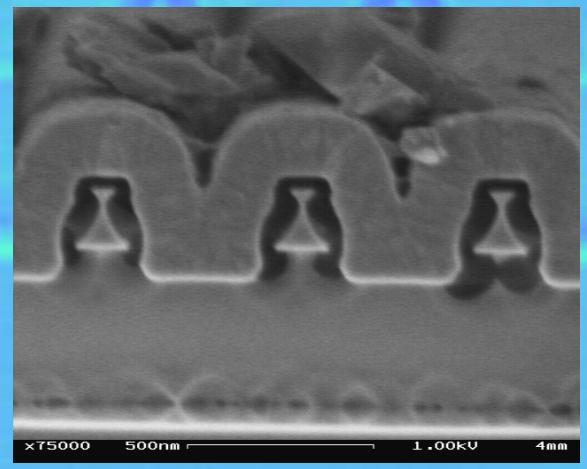
Process uniformity:

- For memory circuit, uniformity across the array is a more relevant parameter compared to the memory device size itself.
- Excellent uniformity is observed in each array.









SEM images of cross-sections for 3 cells in central, constriction and electrode regions.

Fabrication

Process advantages

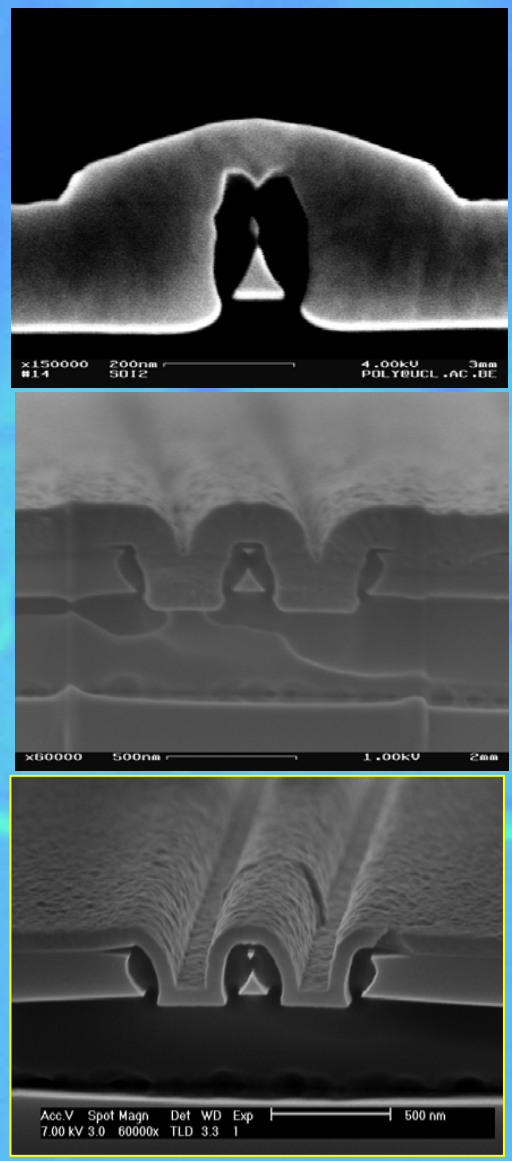
(1) It does not require very fine pattern formation technology to obtain a nano floating gate;

(2) The nano floating gate and the tunnel oxide are performed simultaneously and the floating gate and the channel are self-aligned;

(3) This process is compatible with CMOS technologies;

(4) Excellent uniformity is observed in each array;

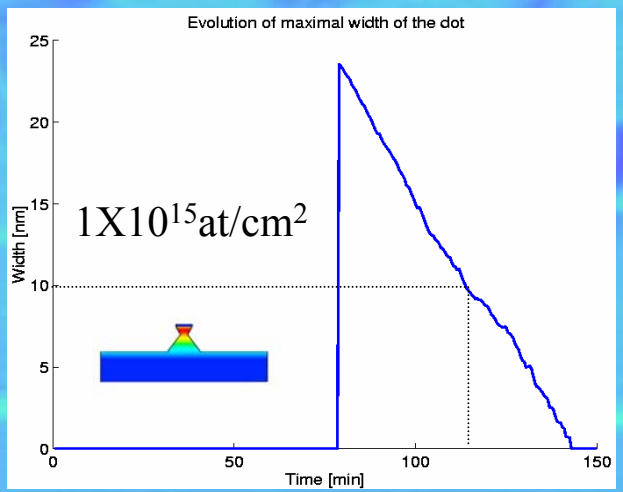
(5) This process is highly reproducible and could be used to realized memory circuits.

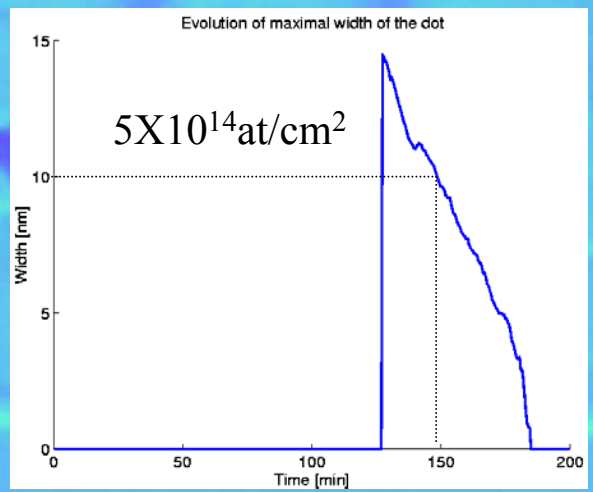


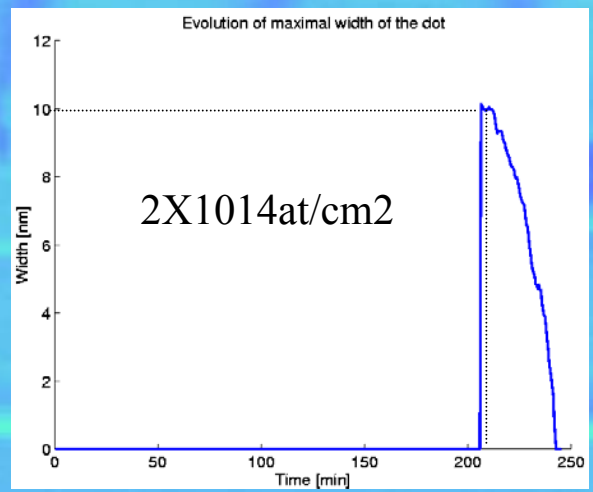
Simulation

Possibility to reduce the As dose

Reducing As dose: $1X10^{15}$==>$5X10^{14}$==>$2X10^{14}$ at/cm^2



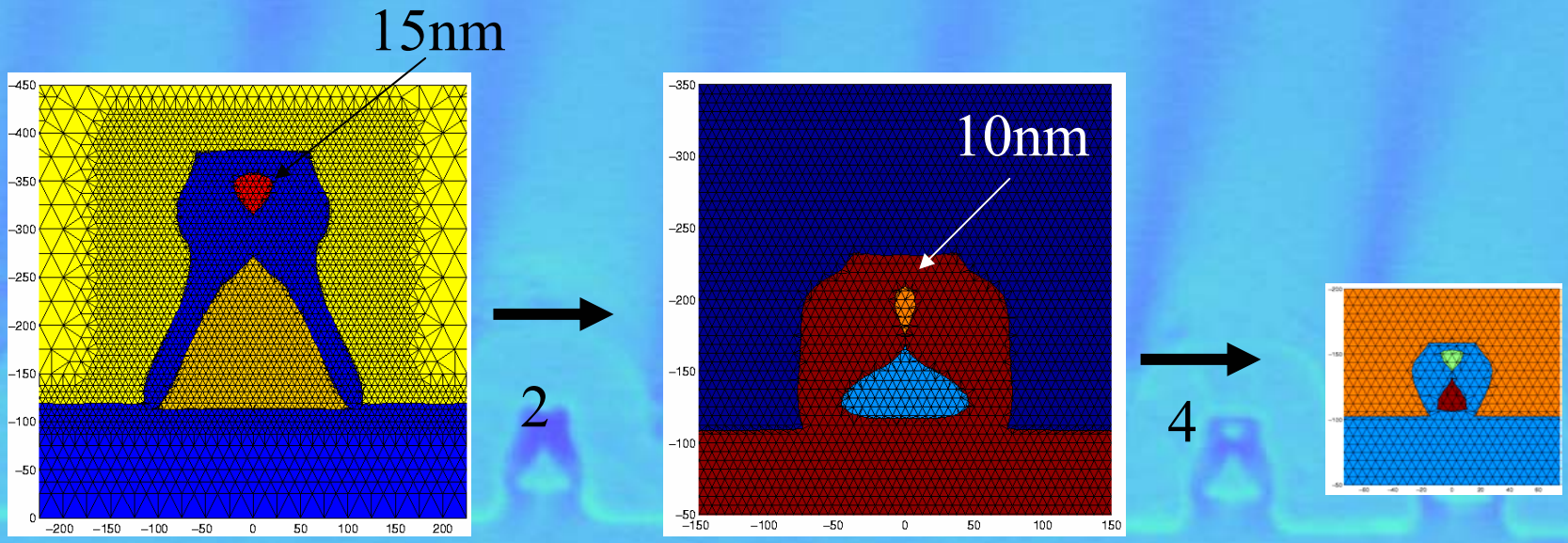




Simulation results:115, 150 and 210 min is needed to obtain a dot of 10nm.

Simulation

- Possibility to have downsizing of a factor *2 and *4



Initial SASEM device

Mini SASEM device

Simulation device

Silicon thickness:200nm;
Central width:150nm;
As doping energy:110KeV;
As doping dose:$1X10^{15}at/cm^2$.

Silicon thickness:100nm;
Central width:75nm;
As doping energy:55KeV;
As doping dose:$5X10^{14}at/cm^2$.

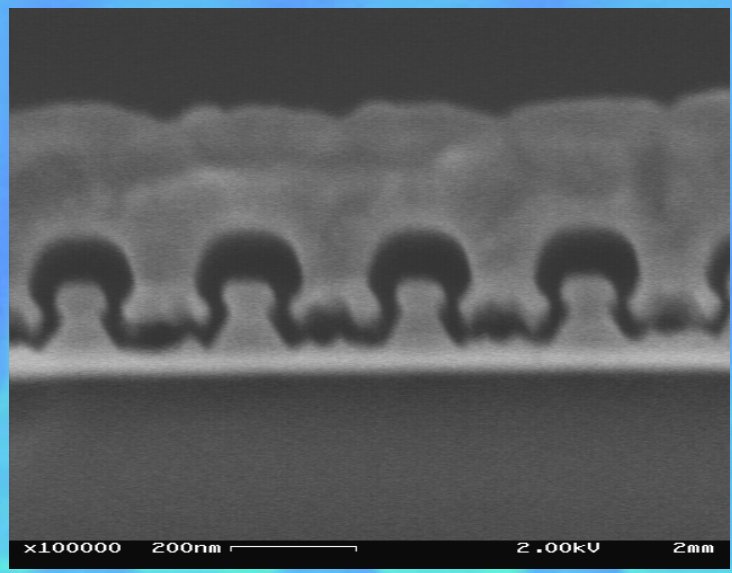
Silicon thickness:50nm;
Central width:35nm;
As doping energy:25KeV;
As doping dose:$2X10^{14}at/cm^2$.

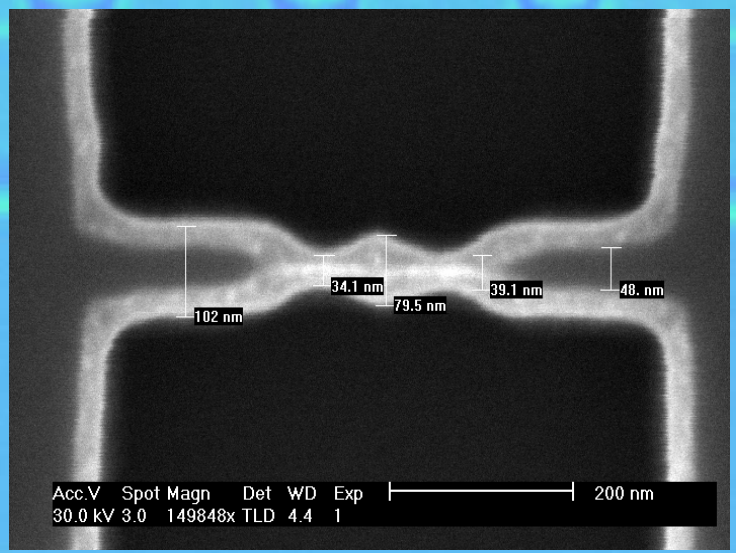
Fabrication

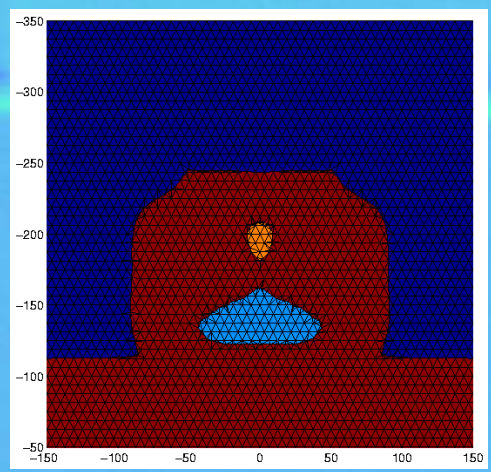
Mini SASEM device

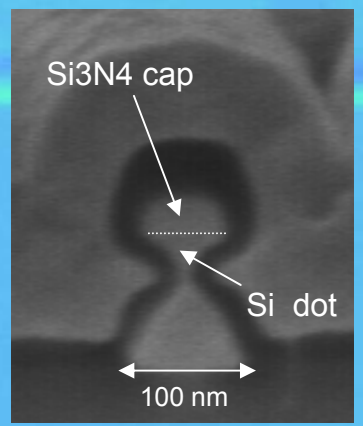
To scale down the initial device by a factor of 2:

Central region:150X150 ==> 75X75nm^2
Constriction width: 100 ==> 50nm
Silicon thickness: 200 ==> 100nm
As doping energy:110 ==> 55KeV;
As doping dose:1X10^{15} ==> 5X10^{14}at/cm^2





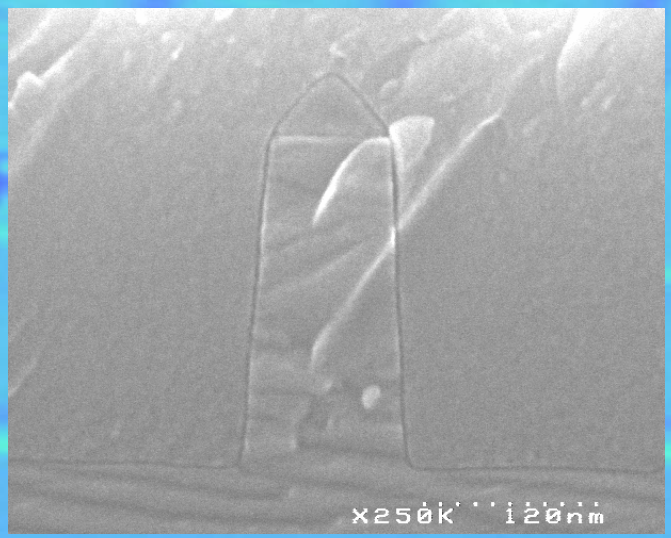




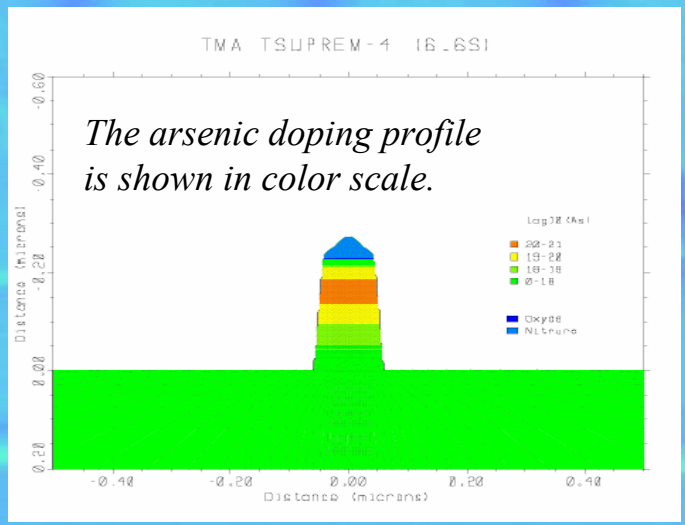
Process at industrial level

Several key steps have been processed in a fabrication line of ST.

Implantation, optical lithography,dry etching, wet and dry oxidation.



Cross-section of a silicon wire after dry etching provided by ST.



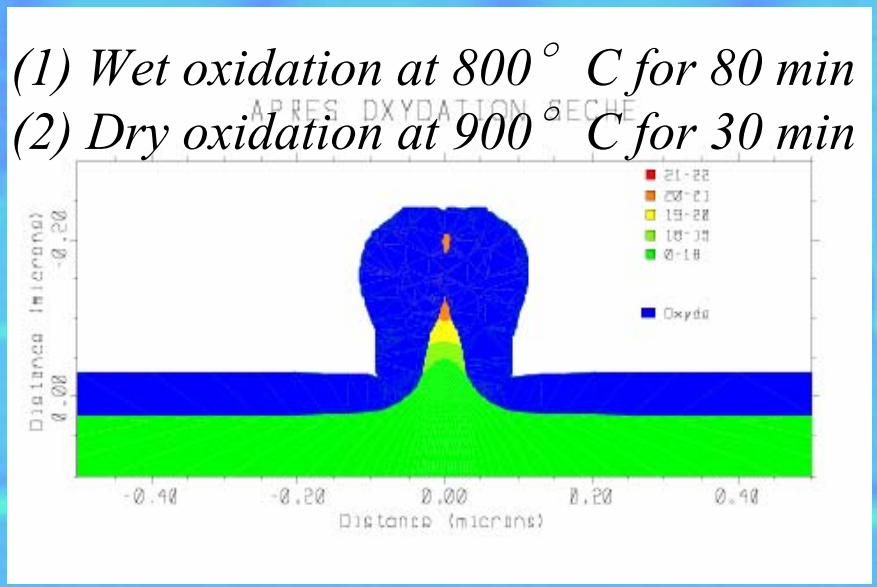
Cross-section of a silicon wire used in simulation.

Process at industrial level

A good agreement between simulation and process is obtained

Oxidation conditions:

(1) Wet oxidation at 800 ° C for 80 min
(2) Dry oxidation at 900 ° C for 30 min

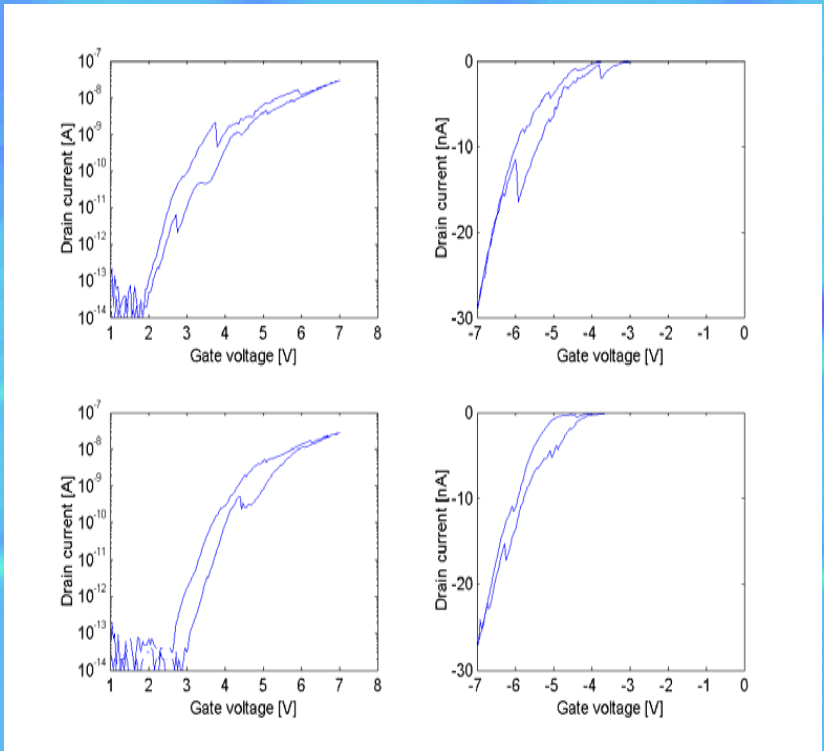


Simulation result of oxidation process performed by UCL.

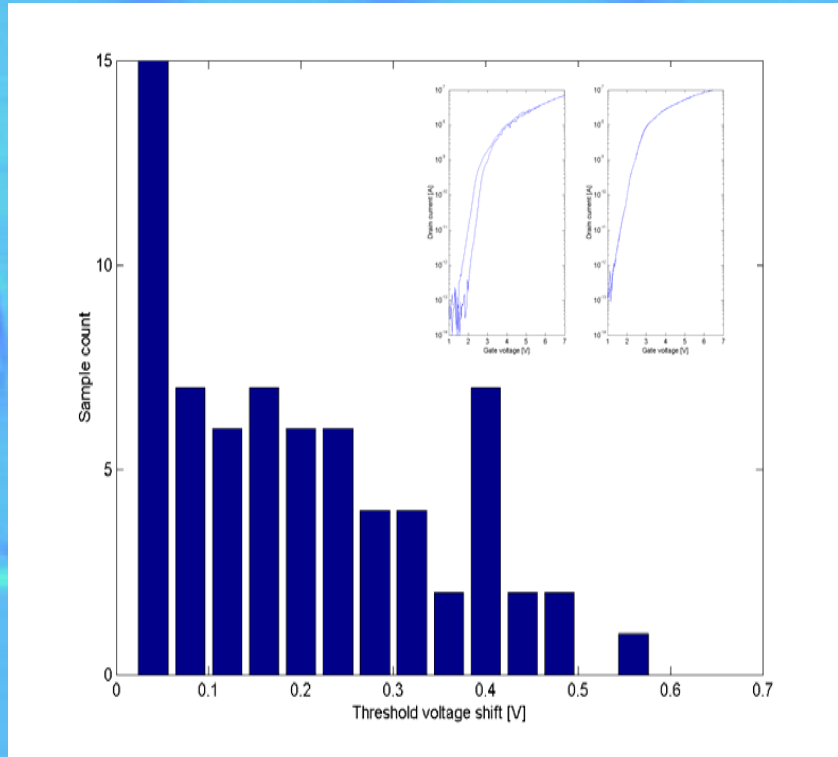
Experimental result of oxidation process provided by ST.

Characterization

This indicates that holes are injected into the floating gate rather than into the traps of the gate oxide.



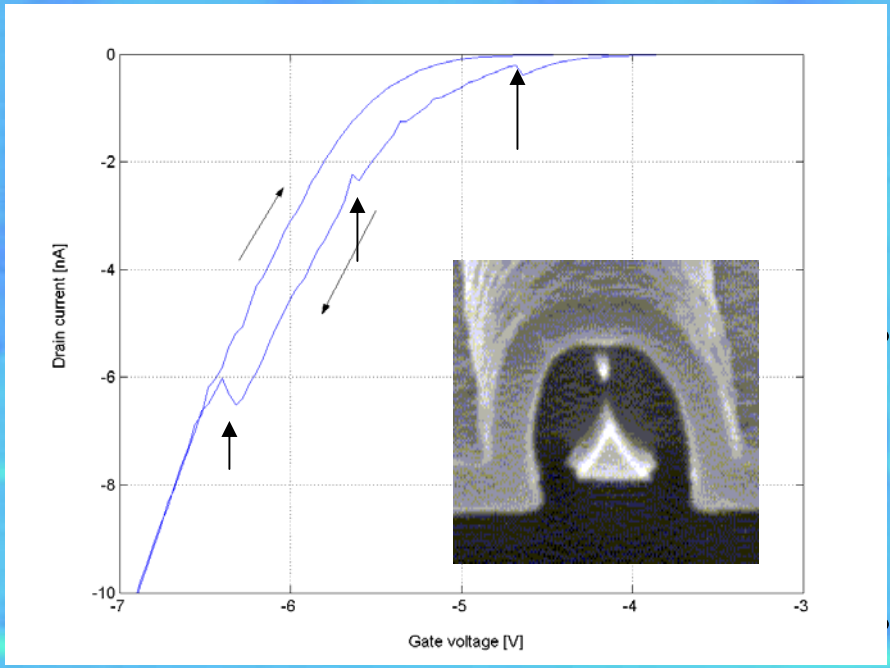
Hysteresis characteristics of memory devices with a gate length of 200nm.



The threshold voltage shift distribution for 70 memory devices.

Characterization

Single-electron memory operation



Hysteresis characteristics of the memory device at room temperature

- Three I_D shifts, corresponding to single hole injection into the floating gate: the first one at -4.6 V, the second one at -5.6 V and the last one at -6.4 V.

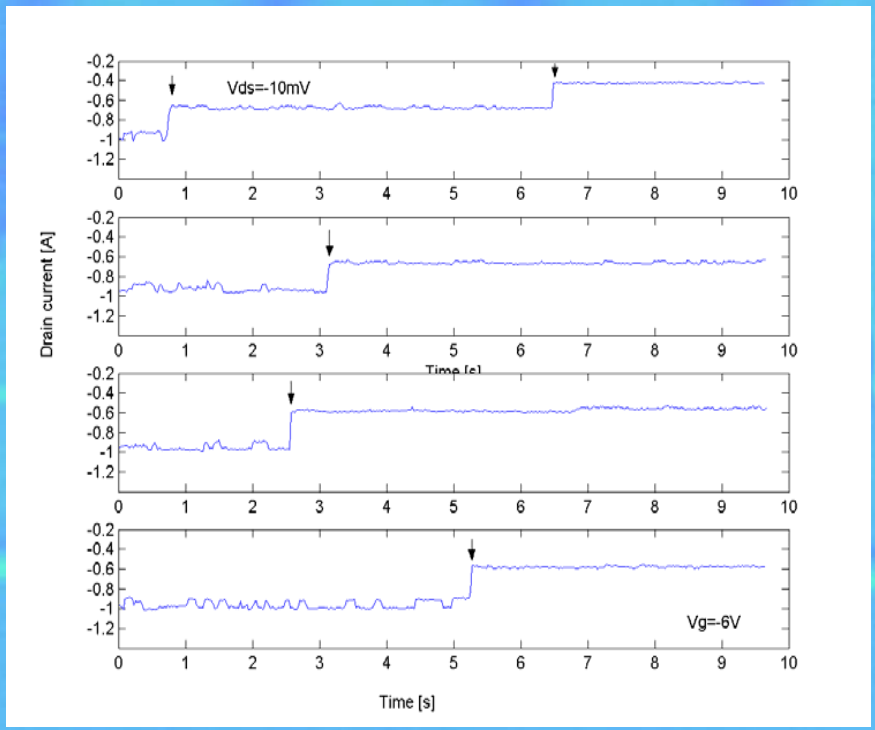
- A quantized threshold voltage shift is obtained. The ΔVth can be expressed approximately by $nX\Delta Vth$, where n is integer and $\Delta Vth=0.1V$.

- $T=q^2/2k_BC_\Sigma$, $C_\Sigma=3aF$ (T=300K)

$C_\Sigma=4\pi\varepsilon_{ox}r$, 2r=14nm.

Characterization

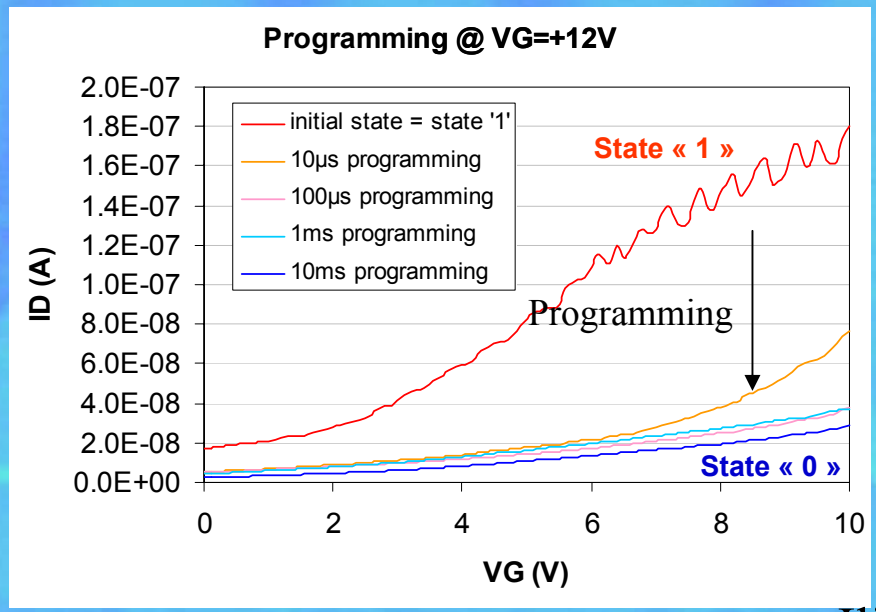
Real-time hole counting measurement

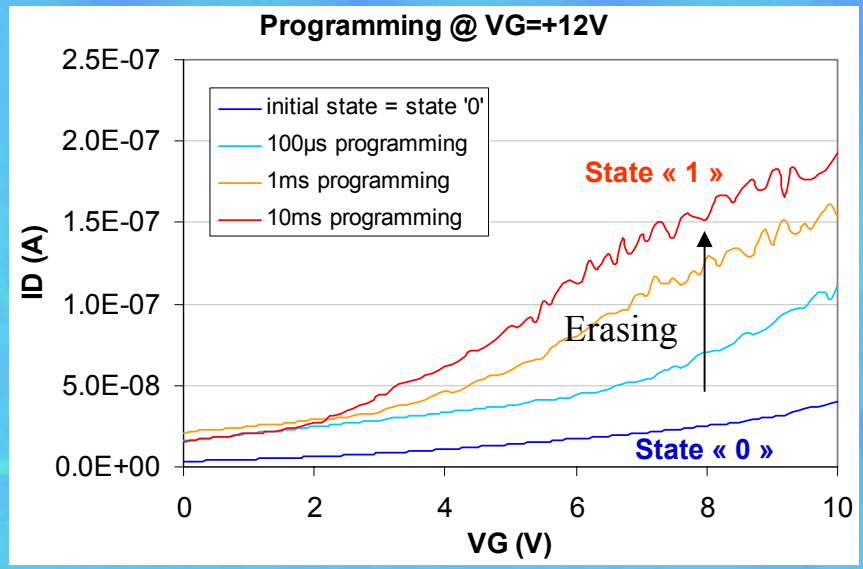


- When one hole is injected into the floating gate, an abrupt drain current reduction was observed at room temperature.
- Sometimes the second hole injection was observed.
- The average injection time of the first hole is calculated to be 7.7s

Characterization

Programming/erasing characterization as a function of pulse duration.





Ilitial state: a negative charge is stored in FG.

Ilitial state:there is no charge stored in FG.

Programming duration:10us
Fowler-Nordheim mechanism

Erasing duration:10ms
Direct tunneling mechanism

Conclusion

- Self-aligned single-electron memory devices with a floating gate of sub-10nm have been fabricated.
- 70 devices have been characterized, memory effects are observed at room temperature. Single-electron memory effects are obtained in some devices.
- Key steps have been processed in a fabrication line of ST microelectronics. Although further improvements are needed to go to industrial fabrication, the present process is compatible with CMOS technology.
- Excellent process uniformity and reproducibility indicates that this process can be used to realize the final memory circuits.