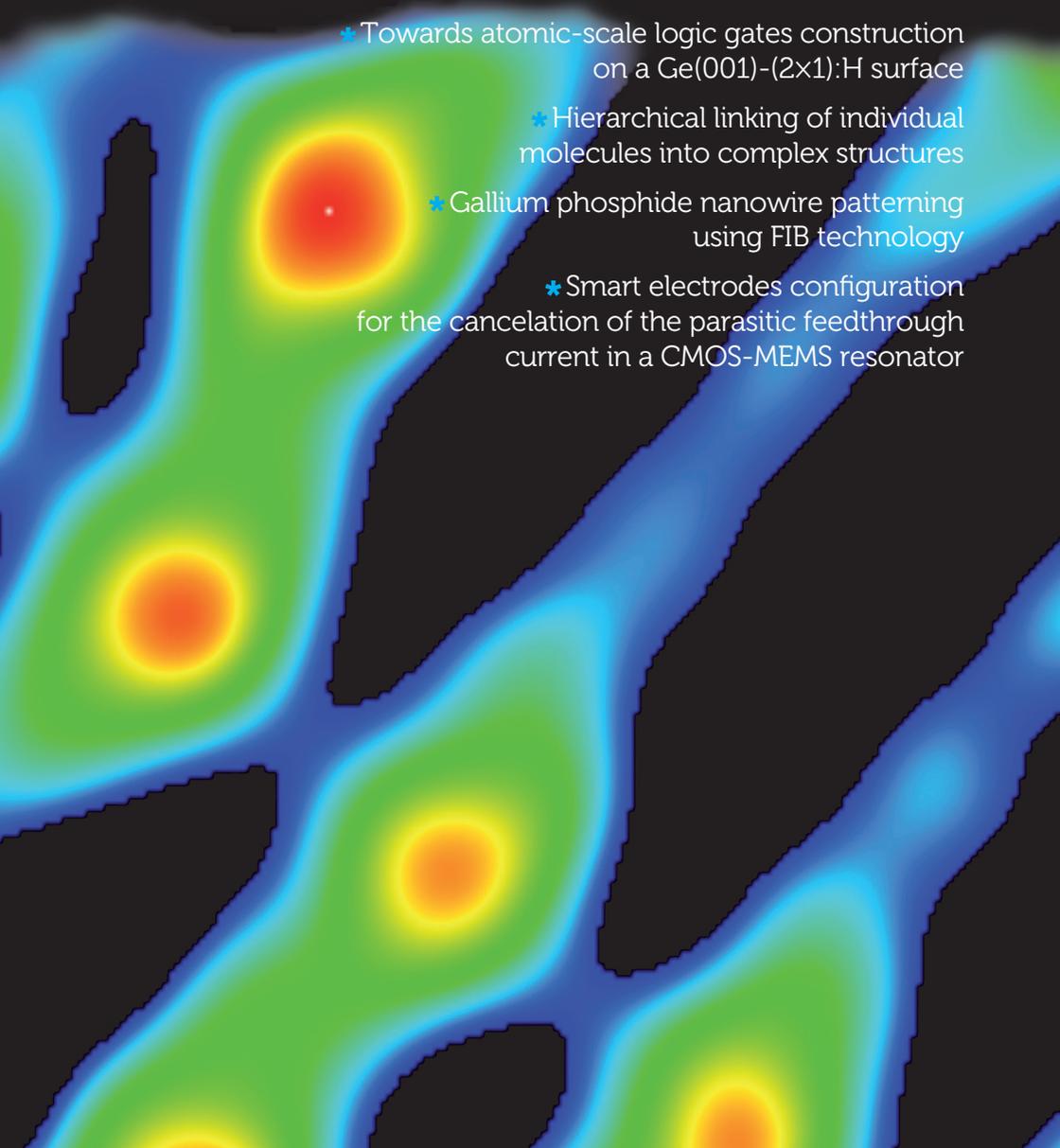


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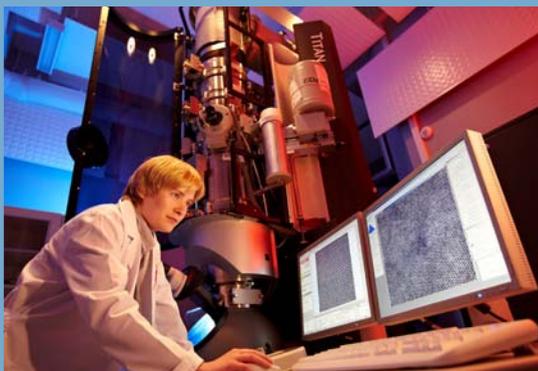
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- * Towards atomic-scale logic gates construction on a Ge(001)-(2x1):H surface
- * Hierarchical linking of individual molecules into complex structures
- * Gallium phosphide nanowire patterning using FIB technology
- * Smart electrodes configuration for the cancelation of the parasitic feedthrough current in a CMOS-MEMS resonator





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dear readers,

The AtMol Integrated Project (EU/ICT/FET) will establish comprehensive process flow for fabricating a molecular chip, i.e. a molecular processing unit comprising a single molecule connected to external mesoscopic electrodes with atomic scale precision and preserving the integrity of the gates down to the atomic level after the encapsulation. This E-nano Newsletter issue contains an article providing new insights towards atomic-scale logic gates construction on a Ge(001)-(2x1):H surface as well as a research highlight on hierarchical linking of individual molecules into complex structures.

In 2011, the nanoICT project (EU/ICT/FET Coordination Action) launched its second call for exchange visits for PhD students and research personnel with the following main objectives: 1. To perform joint work or to be trained in the leading European industrial and academic research institutions; 2. To enhance long-term collaborations within the ERA; 3. To generate high-skilled personnel and to facilitate technology transfer.

The first outcome reports were published in issues 22 & 23 and this edition contains two new articles providing insights in relevant fields for nanoICT.

We would like to thank all the authors who contributed to this issue as well as the European Commission for the financial support (ICT/FET FP7 AtMol No. 270028).

> **Dr. Antonio Correia** Editor - Phantoms Foundation

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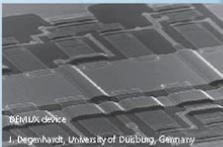
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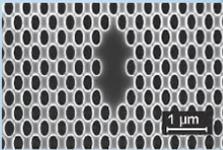
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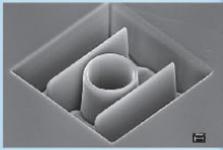
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Towards atomic-scale logic gates construction on a Ge(001)-(2×1):H surface

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Abstract

Atomically precise dangling bond (DB) are fabricated dimer-by-dimer on a hydrogen-passivated Ge(001)-(2×1):H surface by STM tip-induced desorption. The DB lines are characterized spectroscopically by STS which reveals that the DB-derived states gradually shift with the number of coupled DBs forming short lines running perpendicular to the surface reconstruction rows. The perspectives for fabrication of DB logic gates are discussed on the basis of the constructed circuit prototypes.

Introduction

Continuous miniaturization of microelectronic devices is nowadays approaching size limitations arising from quantum effects strongly influencing performance of the devices in the nanoscale. Beyond those limits the most straightforward approach in which the

density of solid state logic units per surface unit area is constantly increased will no longer be possible. Therefore alternative solutions have been proposed. Among them the idea of monomolecular electronics and atomic scale logic gates seems to be one of the most interesting approaches and has been subjected to numerous experiments and simulations (see [1] and references therein).

For successful development of novel logic gate circuits at the nanoscale specific surfaces are required that allow for creation of electronic interconnects and atomic nanostructures and provide retention of intrinsic properties of active organic molecules adsorbed on this surface. Among different templates the hydrogen passivated semiconductors, i.e. Ge(100):H and Si(100):H are very promising. On one hand hydrogen layer isolates significantly polyaromatic boards from the influence of the electronic structure of underlying substrate. On the other hand, as it was already demonstrated, the application of atomically precise STM tip induced desorption of hydrogen atoms makes perspectives for at will fabrication of sophisticated and complex dangling bond (DB) nanostructures [2-9]. DB nanostructures may be directly used for molecular electronics as interconnects at the nanoscale. Recently also new concepts have been presented in which DB structures would intercept the role of active organic parts, and equipped with additional molecular latches, may play a

role of counting/logic circuits based on quantum interferences [3].

Future utilization of dangling bond (DB) nanostructures requires detailed knowledge of their electronic structure which is, regardless of the numerous experiments, still badly understood. Therefore a thorough examination of electronic structure and couplings between adjacent DBs is needed. In this context, the low temperature STM is a very powerful tool enabling both very precise characterization of the geometry and morphology of the system as well as the evaluation of the spatial distribution of the density of states in the subnanometer range.

Formation of single and double DB structures and their electronic properties on the hydrogen passivated Si(001):H surface have been widely studied by STM/STS techniques at room temperature as well as at low temperature regime [10,11]. Similarly formation of lines of silicon DBs have been proven to be feasible [4,5,11].

Wolkov et al have analyzed the influence of substrate doping on charge states of single silicon DBs and demonstrated that due to coupling between them charging of single DBs depends on the presence of neighboring DBs and the separation between them [7,9]. Similarly larger surface structures, i.e. titanium islands also influences the charge states of DBs present in the vicinity [8].

Coupling between nearest neighbors has been described by Hitusogi et al who prepared silicon DB lines running along surface reconstruction rows. Experiments showed strong coupling leading to Jahn

Teller distortion and charge redistribution [5]. For applications in atomic scale computing devices and quantum state engineering, a moderate coupling in effect smaller than within those lines, would be beneficial. Therefore DB lines running across surface rows are promising candidates, but still have not been explored.

In this paper we present that dimer-by-dimer hydrogen extraction can lead to at will formation of complex DB nanostructures on Ge(001):H. Furthermore, we demonstrate that, unlike on Si(001):H surface, the electronic properties of STM fabricated DB structures could be directly explored by STS technique.

Experimental details

The experiment was carried out in an ultra-high vacuum (UHV) system containing preparation, surface analysis, and radial distribution chambers. The STM measurements were performed with the Omicron low temperature scanning probe microscope (LT STM/AFM). The base pressure was in the low 10^{-10} mbar range. The preparation chamber was supplied with a noble gas ion gun, home built hydrogen cracker and an infrared pyrometer. The surface quality was monitored with a low energy electron diffraction (LEED) setup. The Ge(001) undoped wafers (TBL Kelpin Crystals) were mounted on sample holders and were heated by direct current flowing through the sample. The samples were first annealed for 6 h at 800 K, and subsequently the cycles of 1 keV Ar⁺ sputtering for 15 min and annealing at 1040 K for 15 min were repeated until a

clean, well-defined surface was obtained, as checked by LEED and STM. The annealing temperature was controlled by the infrared pyrometer. Hydrogen passivation was performed with use of a home built hydrogen cracker providing atomic hydrogen. During the passivation procedure, the sample was kept at 485 K and the hydrogen pressure was maintained at 1×10^{-7} mbar. The STM imaging was carried out at reduced temperature of around 4 K (liquid helium) with etched tungsten tips used as probes. For image processing and STM data analysis SPIP software was used.

Results and discussion

Ge(001):H surface

Figure 1 shows low temperature (liquid helium, 4 K) filled state STM images of Ge(001) (left panel) and hydrogen passivated Ge(001):H (right panel) surfaces. Ge(001) image exhibits clearly a $c(4 \times 2)$ reconstruction which arises from out-of-phase buckling of neighboring Ge dimers. The hydrogenated surface is recorded as a ladder structure consisting of rows of Ge dimers passivated by hydrogen atoms. In the right panel image, one can distinguish three main types of intrinsic defects usually present on this surface. The brightest are attributed to surface double DBs (two dangling bonds on a Ge dimer), slightly smaller and less bright are single DBs (one dangling bond per Ge dimer). The third type recorded as dark depletion is ascribed to surface Ge atom vacancies. Note that the apparent height of surface double DBs is in principle identical to the height of surface Ge atoms on unpassivated surface.

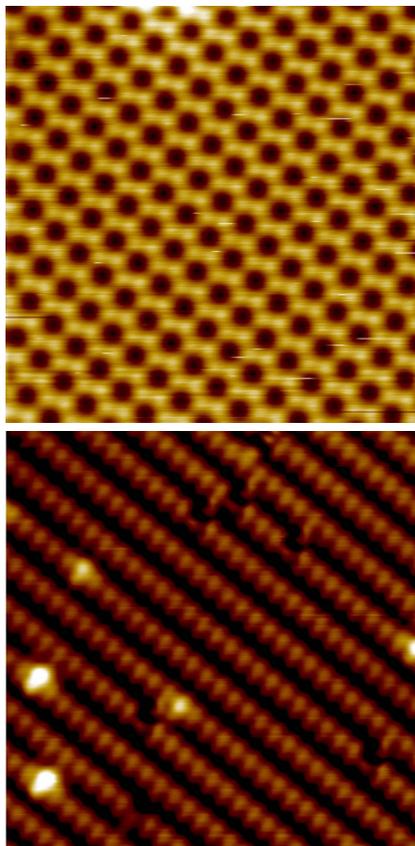


Fig. 1 > Filled state low temperature STM images of Ge(001)- $c(4 \times 2)$ (top panel) and Ge(001)- (2×1) :H (bottom panel) surfaces, scan size $10 \times 10 \text{ nm}^2$, STM parameters - 2 V and 25 pA (top panel), -0.5 V and 1 nA (bottom panel)./

LT-UHV-STM Dangling Bond line construction on the Ge(001):H surface

Only very few examples of DB nanostructures constructed on the Ge(001):H surface have been demonstrated. We have constructed atomically clean and ordered dangling bond lines and also obtained the first

spectroscopic characterization of Ge(001):H-DB lines running across the Ge(001):H surface reconstruction rows. The construction of a given DB atomic scale line is performed with a newly developed vertical atom manipulation procedure. First, the STM tip apex is located over a selected passivated dimer. Then, the STM feedback loop signal is turned off and the tunnel junction bias voltage is increased for a certain period of time. The described procedure allows for at will creation of DB atomic scale lines and small circuits. In the upper row of Fig. 2, the step by step LT-STM construction of a DB atomic line running across reconstruction rows of the substrate is presented. To interpret the images obtained from the STM measurements, the surface images were theoretically calculated using the ESQC scattering matrix approach as incorporated in a surface Green-function matching (SGFM) method. A tungsten tip was used to calculate those images in order to reproduce the experimental conditions. The calculated images of the Ge(001):H surfaces shown in the middle row of Fig. 2 match very well with the experimental images, confirming the relaxed conformation of the surface DB dimers on a Ge(001):H surface. In this constructed DB line, simple atomic structure with 1, 2, and 3 DB dimers in length are buckled to one side with a buckling angle of about 19 degrees. This

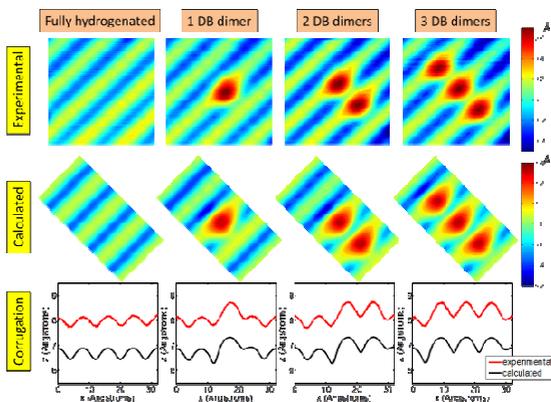


Fig. 2 > LT-UHV-STM experimentals and ESQC calculated images of a progressively STM constructed dangling bond atomic line on the Ge(001):H surface (top row) and a comparison with the theoretical calculations..

buckling was confirmed by comparing line by line the experimental and the calculated scans using the optimized Ge(001):H-dangling bond dimer surface structure. A small difference in corrugation between the two still exists due to the tip apex structure difference between the one used in the calculation and the one in the experiments as shown in the bottom row of Fig. 2.

In order to investigate the electronic structure of those DB lines, we have also performed a series of STS measurements. The differential tunneling conductance dI/dV for V in the range from -0.5 V to 1.0 V was recorded in a STS mode where the feedback loop is turned on between every two $I(V)$ characteristics recording. For dI/dV mapping, a grid over a 2.5 nm \times 2.5 nm surface area was used. The results obtained for 1, 2, and 3 DB dimers aligned perpendicular to the reconstruction rows, for a fully hydrogenated Ge(001) surface, and for a Ge(001)-c(4 \times 2) surface at 4 K are

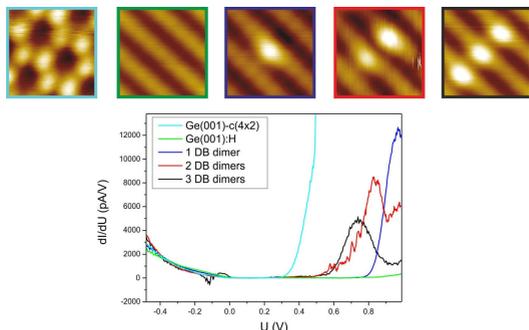


Fig. 3 > Experimentally measured standard constant current (1 nA, -0.5 V) STM images (upper row) and the STS data taken for the corresponding 1, 2, and 3 DB dimers, a fully hydrogenated Ge(001):H surface, and bare Ge(001)-c(4x2) surface./

presented in Fig. 3. The dI/dV spectra for Ge(001)-c(4x2) (green curve) and Ge(001):H (light blue curve), averaged over several unit cells, clearly show the broadening of the surface band gap after the hydrogenation procedure, which significantly increases from 250 mV for bare Ge surface to about 800 mV for Ge(001):H. In the dI/dV spectra for 1, 2, and 3 DB dimers, the data are integrated over the whole nanostructure area in order to average out effects arising from inevitable fluctuations. Most notably, in an energy range from +0.5 eV to +1.0 eV, there is a pronounced DOS maximum which is gradually shifting towards lower energies (within the band gap range of the Ge(001):H surface) when the length of the DB line increases. Those STS experiments confirms that conductance channels are created by the construction of a dangling bond line on a Ge(001):H surface as already predicted theoretically for Si(001):H surfaces [12].

The construction of the DB logic gate circuitry

In order to develop efficient protocols allowing for construction of surface atomic logic gates, we have focused the experiments on the construction of stable DB atomic scale lines extended over sizable areas to follow the planar circuit design. Contrary to the usual very fast high voltage pulse scanning used to extract randomly a lot of H atoms, we have extracted

dimer-by-dimer H atoms reaching the best possible atomic scale ordered DB lines. The experiments demonstrated that the logic gates design proposed in [3] is realistic, can be constructed and is stable in LT under the UHV conditions. We have succeeded to construct very long DB lines up to 10 nm in length and one atom in width to demonstrate that the developed planar interconnection strategy is now fully compatible in dimensions with the atomic scale construction technique. The length of the line presented in Fig. 4 is

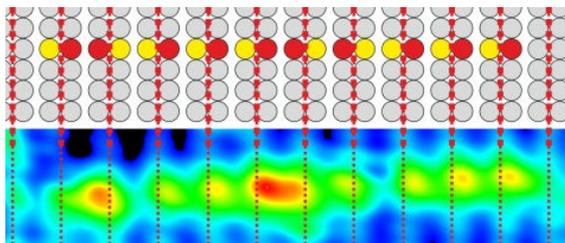


Fig. 4 > A 10 nm long DB line constructed dimer-by-dimer on the Ge(001):H surface and extending in a direction perpendicular to the hydrogenated surface rows, filled states STM image (lower panel, $2 \times 10 \text{ nm}^2$) and a schematic geometrical model (upper panel). Color coding: light grey – surface hydrogen atoms, red and yellow – buckled (up and down respectively) surface Ge atoms exposing dangling bonds at the vacuum interface. Tunneling current 1 nA, bias voltage 0.5 V. 20 H atoms have been step-by-step extracted./

compatible with the metallic nano-pads separation, which can now be reached under an atomic scale interconnection machines.

Those experiments have also demonstrated that the construction of long DB lines is only limited by the quality of the hydrogenated semiconductor surface, i.e. by the density of native surface defects which are inevitably present on the Ge(001):H surface. However, small surface DB circuit must contain not only DBs distributed across Ge(001):H dimer rows, but also nearest neighbors located over the very same hydrogenated surface row [3]. Therefore due to the significantly stronger electronic coupling between DBs running parallel to the dimer rows than those running perpendicular, it was of prime importance to construct the simple DB logic gates containing neighboring DB dimers situated over the same surface reconstruction row and check their stability. As demonstrated in Fig.5, structural fluctuations take place even at LT. This comes from the fact that the structural buckling order along the DB line constructed in Fig. 5 is competing with the relaxation of the DB dimers over the same surface reconstruction row. This competition occurs already for 2 neighboring DBs. This points out that the next design of surface DB logic gates will have to take into account the surface relaxation phenomenon.

To overcome the fluctuations, we have constructed a small 2-input like DB circuit by extracting the gate input atoms one lattice constant away from the DB line. This is presented in Fig. 6 with the corresponding atomic scale surface structure. Here and also for larger

separation between the input DB and the DB line, the surface structural fluctuations are no more observed. The simple circuit shown in Fig. 6 is a very nice experimental demonstration that the atomic scale construction technology is beneficial for the design of not only semi-classical DB circuits but also for quantum Hamiltonian computing (QHC) DB logic gates. Those DB logic gates are good candidates for using the moderate electronic decoupling between the input dimers and the core of the DB line as shown in Fig. 6.

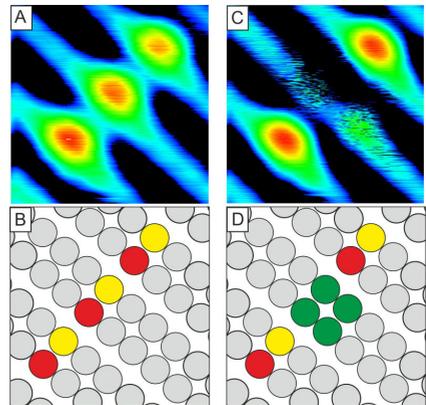


Fig. 5 > DB lines constructed on the Ge(001):H surface. (A) filled state STM image of DB atomic scale line containing 3 DB dimers (6 DBs); (B) structural model of the line; (C) STM image revealing fluctuations after desorption of following hydrogen atoms; (D) structural model of the fluctuating system, color coding: light grey – surface hydrogen atoms, red and yellow – buckled (up and down respectively) surface Ge atoms exposing dangling bonds at the vacuum interface, green – fluctuating atoms, image area: $2,5 \times 2,5 \text{ nm}^2$, tunneling current 1 nA, bias voltage 0,5 V./

Conclusions

In conclusion, we have developed a new protocol to efficiently construct atomically

precise DB nanostructures on a Ge(001):H surface, by at will dimer-by-dimer hydrogen desorption. We demonstrate that fabricated DB nanostructures are stable and STS experiments indicate that the coupling between neighboring DBs results in DOS peak shifts that gives perspectives for applications of DB nanocircuits in logic gates and as quantum dots.

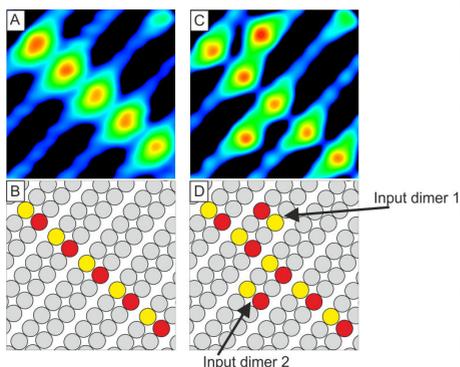


Fig. 6 > DB line fabricated on the Ge(001):H surface; (A) filled state STM image of DB line containing 5 DB dimers (10 DBs), (B) structural model of the line, (C) STM image showing the same DB line structure but containing now two additional DB dimers (4 DBs) revealing stability of the entire structure, (D) structural model of the final structure, color coding: as in Fig. 5, image area: $3,5 \times 3,5 \text{ nm}^2$, tunneling current 1 nA, bias voltage 0,5 V.

Acknowledgments

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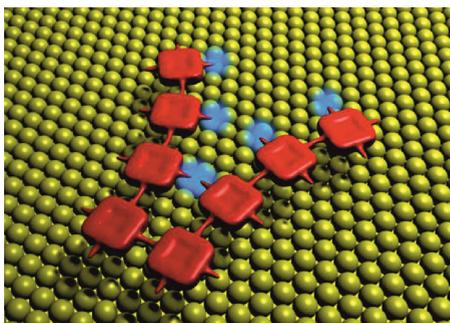
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Hierarchical linking of individual molecules into complex structures

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Controlled assembly of nanoscopic building blocks on a surface - towards novel materials and molecular electronics.



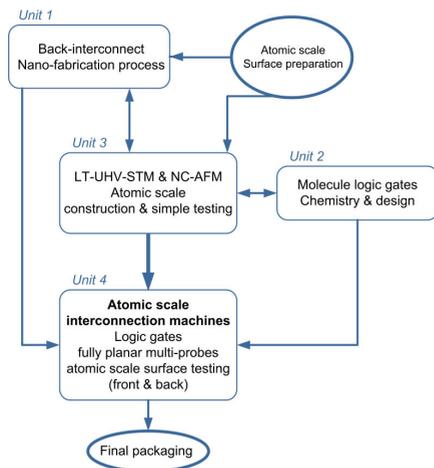
A central challenge of nanotechnology which is crucial to visions such as molecular machines, novel materials and molecular electronics lies in the “bottom-up” connection of molecular building blocks in a well-defined assembly. One can think of it as similar to LEGO, however at the nanometer scale (1 nm = 1 billionth of a meter). Due to their exceptionally low size such structures hold the promise of various advantages, such as low energy consumption, high operating speeds and low production costs. However, so far molecules could only be connected in a

one-step process, resulting in low complexity.

Researchers at the Fritz-Haber-Institute Berlin (in collaboration with physicists of the Laboratorio TASC in Trieste and chemists of the Humboldt-University Berlin) could now within the European Project AtMol demonstrate for the first time hierarchical growth in several steps by “activating” particular sites of the molecules in a controlled manner. This was performed by sequentially supplying reactive sites on molecular building blocks via specifically designed side groups, allowing the step-by-step formation of more sophisticated structures. With this method the researchers could obtain high selectivity in the formation of networks made of two different molecular building blocks, which would not have been possible with a non-hierarchical process. The selectively induced linking allows not only the growth of more sophisticated but also of more regular networks. It could also be shown that a pre-ordering of the adsorbed structures is achieved by the use of a suitable corrugated surface.

Publication

L. Lafferentz, V. Eberhardt, C. Dri, C. Africh, G. Comelli, F. Esch, S. Hecht, L. Grill, *Controlling on-surface polymerization by hierarchical and substrate-directed growth*; Nature Chemistry Vol. 4, 215 (2012).



Unit 01: Back interconnects nanofabrication process

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Unit 2: Molecule logic gate chemistry & design

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- Multi-probe characterization of 1D and 2D nanostructures assembled on Ge(001) surface by gold atom deposition and annealing; In Advances in Atom and Single Molecule Machines, Vol.1 (2012).

Unit 05: Management, dissemination and training activities

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- AtMol International Workshop 2011 Singapore Abstracts Book: "Atomic Scale Interconnection Machine"
- E-Nano Newsletter 22, 5 (2011): "Atomic Scale and Single Molecule Logic Gate Technologies"
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Gallium phosphide nanowire patterning using FIB technology

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Abstract

The fabrication of ultrathin (20nm in diameter or less) gallium phosphide (GaP) nanowires (NWs) patterns is still a challenge. This article presents a new promising method: we will achieve the growth and patterning of gallium phosphide nanowires after local implantation of gold catalyzers by ultrahigh resolution focused ion beam (FIB), using a pure gold ion source. We also propose to use a thin SiC dielectric layer on the GaP substrate to limit the creation of defects in the GaP and to tune the resolution of implanted gold nanoparticles. This is possible as the pure gold ion source FIB allows for both etching the SiC layer and implantation of gold ions at the GaP surface. GaP NWs are subsequently grown from the implanted gold nanoparticles using metal organic vapor phase epitaxy (MOVPE).

Introduction

Several applications in biology would benefit from the ability to make nanowires (NWs) with a diameter smaller than 20 nm, with a controlled positioning

and spacing. Recently, nanoscale surfaces were used for the long-term maintenance of mesenchymal stem cell phenotype and multipotency [1]. Similarly, the stem cell differentiation has also been shown to depend on the geometry, and the order/disorder of nanostructures or nanopores on a substrate [2]. Recently, a method for measuring cellular forces using hexagonal nanowire arrays was developed in our lab [3]. By labeling nanowires fluorescently and by monitoring the nanowire tip displacement using confocal microscopy, it was possible to calculate the forces exerted on the deflected nanowires according to linear elasticity theory. The nanowires, grown on (111) B gallium phosphide (GaP) substrate from gold nano-seeds in a hexagonal pattern produced by electron beam lithography (EBL), metal evaporation and lift-off had a diameter of 40 nm, setting the force detection limit to approximately 10 pN. Many forces in living cells are between 1 and 10 pN and typical forces in lipid bilayers are on the order of 1 pN. This nanowire based sensing method and the necessity to study cell responses to different kinds of nanostructured surfaces both require a technique enabling the development of arrays of GaP NWs with a diameter below 40 nm.

In order to detect forces in the piconewton range and to develop biomimetic models of cell membranes, we aim at seeding sub-20 nm diameter gold nanoparticles by using ultrahigh

resolution focused ion beam (FIB) equipped with a pure gold ion source. The use of a pure gold ion source offers to deposit catalyst gold particles without contamination by gallium ions which may hinder the epitaxial growth of nanowires. We show that it is possible to grow nanowires from these implanted particles. The use of the FIB-nanowriter in that purpose would enable the implantation of very small doses of gold on the substrate, and therefore the possibility to obtain very thin GaP NWs.

Pure gold ion source FIB

We have used a new type of FIB instrument for patterning the gold particles on the substrate. The prototype is using a focused beam of charged particles similarly to the technology that has been validated in the NanoFIB project [4]. Major modifications were needed in order to investigate the deposition of nanometer scale gold islands on the substrate. These technological developments can be listed as the following key elements:

1. The Liquid Metal Ion Source (LMIS) emitter

We have developed a pure gold ion emitter with a geometry that is extremely stable. We have demonstrated that Au-LMIS sources can reach lifetimes exceeding 500 hours without any noticeable degradation of both the I/V and optical characteristics for operation at a gun base pressure around 1×10^{-8} mbar [5]. Our source geometry allows pure gold to be used rather than eutectic alloys with reduced melting points. In our case, the main advantage is to avoid the insertion

of a velocity filter (Wien filter) to select Au-ions having a precise charge to mass ratio. Indeed such a filter drastically reduces the probe current of the Au beam (to below a few pA) and adds detrimental aberrations to the focusing ion optics making it difficult to produce spot sizes below 100 nm.

2. The electrostatic optics design

The electrostatic optics architecture of the FIB column was designed to achieve the highest possible patterning resolution with a beam energy range below 20 keV. This ion optics uses two electrostatic lenses working in the deceleration mode and is physically separated, by using a narrow collimation aperture (5 to 20 μm in size), from the beam generating unit hosting the gold LMIS. The optimum value of the spot diameter was found to be below 50 nm (FWHM) for a 20 keV gold ion beam. Such a low value has never previously been demonstrated for a focused gold ion beam.

3. The Nanofabrication Platform

The platform on which the Gold FIB column and ion source are implemented is a custom made Raith150 EBL writer. It enables short working distances and strong demagnification mode for the ion optics. The stage is controlled by a 2-axis Michelson-laser interferometer with a numerical resolution of 2 nm, allowing the system stitching capability to be better than 60 nm. A 10 MHz pattern generator governs the ion beam electrostatic deflection in a writing field (typically 100 x 100 μm for a beam energy of 20 keV) allowing gold ions to be implanted onto a substrate at selected locations with a pre-determined organization.

Promising results of thin semiconductor GaAs nanowires grown from implanted gold dots in GaAs substrates with this focused gold ion beam source have been obtained recently [5]. Here, gold nanoparticles were seeded with a (Au^+) ion beam energy of 20 keV on GaP substrates.

GaP NWs growth after gold implantation on a GaP substrate

The GaP NWs were grown by metal organic vapor-phase epitaxy (MOVPE) from the gold nanoparticles. After being transferred to a growth chamber (Aix 200/4, Aixtron AG, Herzogenrath, Germany). The temperature for nanowire growth was 470 °C, and the NW growth was initiated by supplying $\text{Ga}(\text{CH}_3)_3$ in addition to PH_3 , with respective precursor molar fractions of 4.3×10^{-6} and 8.5×10^{-2} in hydrogen carrier gas flow of $13 \text{ L} \cdot \text{min}^{-1}$, and under a pressure of 10 kPa, as previously described [6]. After growth, the NWs were about 1 μm in length. The resulting wires should grow in the (111) B direction, vertical to the surface, but the quality of the GaP crystal near the gold nano-island could also affect the growth direction.

Figure 1 shows a scanning electron microscope (SEM) image of the GaP NWs grown from the implanted patterns. Some sputtering effects during FIB implantation implied a parasitic deposition of the precursor material around the nucleation site, inducing a parasitic nanowires growth. Indeed, due to the insulating nature of GaP, electronic charges accumulate in the GaP area around the nucleation site during gold deposition. Gold ions will be attracted toward this area and constitute precursor sites for parasitic GaP nanowire growth.

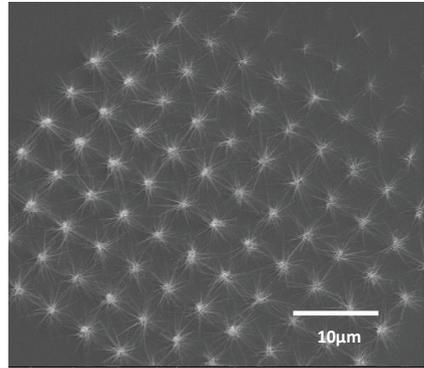


Fig. 1 > SEM image of GaPNWs grown from gold nanoparticles seeded with a (Au^+) ion beam energy of 20keV./

Nano - patterning method: towards thin GaP NW arrays

In order to prevent the parasitic nanowire growth, we propose to coat the GaP substrate with a sacrificial carbonated silicon (SiC) mask (Figure 2.a). A thin SiC layer can be deposited on the GaP (111) B substrate by radio frequency physical vapor deposition plasma enhanced chemical vapor (RF PVD). The pure gold ion source FIB enables both to realize a local nano-patterning of the SiC layer and to deposit the gold nanoparticle inside the pattern (Figure 2.b) [7].

Figure 3 shows a schematic representation of the sample surface profile evolution for different numbers of implanted ions [7]. First, voids and interstitial atoms are created leading to amorphization and resulting in a local volume enhancement (green profile, Figure 3). The SiC layer etching takes place thanks to the two distinct phenomena occurring sequentially during ion implantation: crystal-to-amorphous transition and amorphous-to-etched material transition (blue and red

profile, Figure 3). The SiC layer combined with the typical "V" etching profile created by FIB irradiation (Figure 2.b) will enable a better spatial resolution for the implanted gold particles.

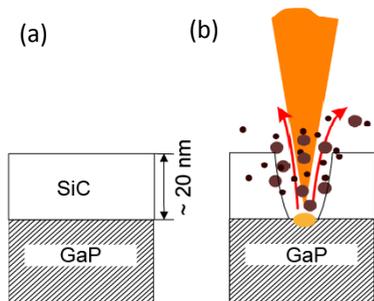


Fig. 2 > Schematic representation of the main processing steps used for the selective gold nanoparticle deposition. (a) SiC mask deposition on the GaP substrate, (b) nano-patterning of the SiC layer and deposition of the gold nanoparticle inside the pattern./

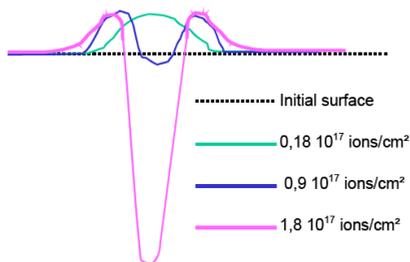


Fig. 3 > Schematic representation of the sample surface evolution with respect to the used implanted ions numbers./

Preliminary tests have been realized and in the future we will test different implanted ions number and different SiC layer thicknesses. This method is promising for the growth of a unique GaP NW for each gold implantation site, and deposition of smaller gold catalytic particles.

Conclusions

We developed a way to seed pure gold nano-catalysts on GaP substrates for subsequent nanowire growth, by using a pure gold ion source FIB. Patterns of GaP NWs were obtained but some parasitic nanowires, grown next to each implantation site, were also observed. We have started to develop a new strategy to seed sub-20nm pure gold particles using a nano-patterning method. The method is based on the use of a SiC coating on the GaP surface prior to the gold implantation and could possibly limit the parasitic nanowire growth.

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Smart electrodes configuration for the cancelation of the parasitic feedthrough current in a CMOS-MEMS resonator

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Abstract

CMOS-MEMS resonators electrostatically actuated and capacitively sensed suffers from parasitic feedthrough current, being more important as the dimensions of the MEMS resonators enters in the NEMS realm. A four electrodes balanced topology has been proven to enhance the electrical transduction of the resonator due to the reduction of the parasitic feedthrough current. The test results obtained show a pure RLC behavior of the resonator with a proper bias polarization using the 4 electrode drivers making suitable for the integration along with a IC oscillator.

Index Terms: MEMS, NEMS, CMOS-MEMS, RF-MEMS, capacitive transduction, feedthrough cancellation.

1. Introduction

Nanoelectromechanical systems (NEMS) are electromechanical devices which are actively investigated because of their physical properties resulting from ultraminiature size elements (dimensions below the microscale) [1]. NEMS advantages include ultralow power

consumption, potential high resonant frequency, and high sensitivity to applied force, external damping, or additional mass. Furthermore, they offer the opportunity to integrate mechanical structures and complementary metal-oxide-semiconductor CMOS- devices on the same die. Due to the small dimensions the most important difficulty is transducing the movement of the NEMS to sense its very small displacements, overcoming parasitic effects and all classes of noise (mainly electrical and intrinsic thermal noise). The use of conductive layers provided by commercial IC-CMOS submicrometric technologies allows to obtain MEMS and NEMS resonators which are electrostatically actuated and capacitively sensed. Several groups have been working in the development of this kind of CMOS-MEMS systems with promising results in the field of sensors [2-4] and also for RF signal processing [5]. In this article we present a new electrode configuration which is capable to decrease the undesired parasitic currents which mask the detection of the resonator movement.

In electrostatic/capacitive MEMS systems, the movement of the resonator is forced by the application of an AC voltage (V_{AC}) between the capacitor formed with the excitation electrode (see Fig. 1a) and the movable structure. The applied voltage generates an attractive electrostatic force that bends the resonator. The capacitive sensing is based on the measurement of the capacitance change originated

between the read-out electrode and the resonator due to the MEMS movement. To quantify this change, a DC voltage (V_{DC}) is applied between the capacitance and the induced output current is measured. Equation 1 corresponds to the measured output current (assuming $V_{dc} \gg V_{ac}$).

$$I \cong V_{DC} \frac{\partial C}{\partial t} + C_p \frac{\partial V_{AC}}{\partial t} \quad (1)$$

where C is the variable capacitance between the suspended structure and the read-out electrode, and C_p is the parasitic capacitance between the excitation and read-out electrodes. The first term corresponds to the current created by the movement while the second term is called parasitic or feedthrough current.

Fig. 1b shows the simplified electrical schematic of a MEMS resonator. An RLC branch models the motional behavior, I_M , while C_p corresponds to the parasitic capacitance that generates the parasitic current. The presence of this capacitance disturbs the MEMS measurement. Depending on the parasitic capacitance value, the majority of the excitation signal goes through the parasitic capacitance and makes the measurement of the resonator characteristics difficult. Moreover, it generates a parallel resonance that makes the phase to have a 90 degrees value at high frequencies, and forces the phase to present two frequencies where their value is zero. [6-7]. Fig.1c shows the simulated effect of the increment of C_p on the resonant peak. It can be seen how a large value of the parasitic capacitance generates a parasitic current that masks the motional current. On the contrary, a reduction of the feedthrough current allows to have a

purely RLC behavior. In the case of the filters, the reduction of the feedthrough capacitance allows to increase the performance of the filter, achieving a higher stop-band rejection.

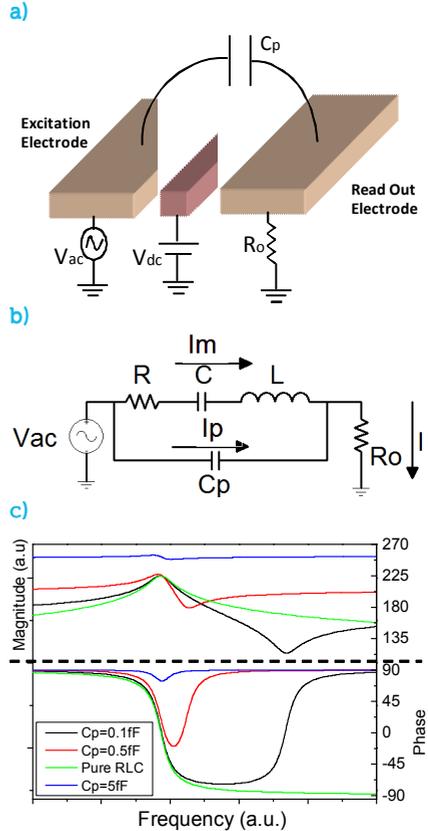


Fig. 1 > a) Schematic of a classical clamped-clamped beam resonator. b) Simplified electrical schematic of a resonator. c) Plot of the magnitude and phase frequency responses of the resonator under the effect of different parasitic capacitance values./

Many studies can be found in the literature focused on reducing the feedthrough effect in MEMS resonators

and filters. Two are the basic ones: a) differential sensing using two identical MEMS resonators [8-11]; b) mixing due to the non-linear dependence of the MEMS movement with the applied voltage allowing to use different frequencies for the actuation and the read-out, cancelling in this way the parasitic effects [12]. In differential methods the cancellation is only effective with identical transduction gaps and coupling areas. While for mixing the electrical set-up is complex and sometimes is not applicable. In [6], Arcamone et al. have proposed a new balanced set-up scheme that allows to eliminate the parasitic capacitance despite the presence of technological mismatching.

Following this work, we present a four electrode configuration for cancelling the parasitic current in a clamped-clamped beam. A correct electrode biasing of the 4 electrodes allows eliminating any gap mismatching that would avoid a correct feedthrough current cancellation. A pure RLC behavior with the elimination of the parallel resonance and a 180° phase shift is then achieved, as we will see in section III. In section IV the electrical characterization of the resonator and the conclusions obtained from this measurements are summarized in the section V.

II. Design and fabrication the resonators

A clamped-clamped beam resonators have been designed and fabricated using the two polysilicon layers of the capacitance module of the Austria Microsystems 0.35µm CMOS technology. The resonator is designed to operate in its first lateral flexural mode in the 10 MHz

range. The nominal resonance frequency of the resonator is given by:

$$f_n = \frac{(\kappa_n l)^2 W}{2\pi L^2} \sqrt{\frac{E}{12\rho}} \quad (2)$$

where the Young modulus E and the density ρ of silicon are respectively 160 GPa and 2330 kg/m³. The first mode constant, $\kappa_n l$, is 4.73. The width, W ; and the length, L as well as the gap, s , and the length of the electrodes, L_e , are detailed in Table I. Fig. 2 shows the SEM image of the 11 MHz fabricated resonator. The first polysilicon layer with a 280 nm thickness is used to implement the beam while the second polysilicon layer is used for the electrodes. Using two different polysilicon layers allows achieving very small gaps down to 40 nm [13].

Resonance frequency	Parameter	Value
11MHz	L	22 µm
	w	500
	L_e	8 µm
	s	100nm

Table 1 > CMOS-MEMS C-C beam dimensions./

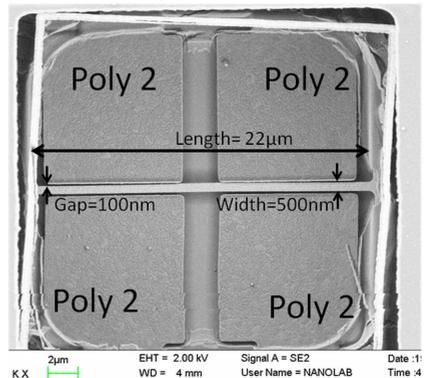


Fig. 2 > SEM image of the four electrode (11MHz) Clamped-Clamped beam resonator./

To reduce the amount of silicon oxide that covers the resonator and reduce the etching time, $15\ \mu\text{m} \times 15\ \mu\text{m}$ vias holes are opened in all metal layers above the resonator. Finally a PAD window is opened to remove the passivation layers on top of the micromechanical resonator. Twenty-eight minutes are enough to eliminate the sacrificial oxide layer and release the structure without using additional masks.

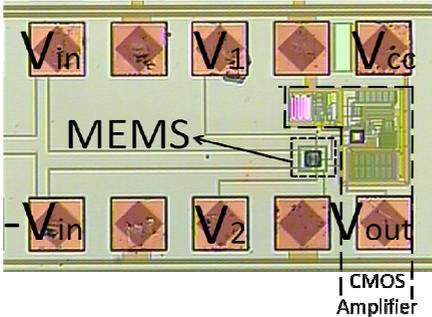


Fig. 3 > Optical image of the four electrode (11MHz) Clamped-Clamped Beam with the CMOS amplifier./

The main advantage of using a CMOS technology to fabricate mechanical devices is the fabrication side by side with the CMOS electronics what provides extreme compactness and enhanced electrical signal-to-noise ratio. The optical image of Fig 3 shows the MEMS and the amplifier as well as the different connection pads used in the characterization stage which will be detailed in next section.

III. Fundamentals of the transduction

Fig.4 shows a diagram of the CC Beam with four electrodes along with the signal set-up. Electrodes 1 and 2 are used as driver electrodes while electrodes 3 and 4

are used to control the gap spacing through the application of specific DC voltages. An ac voltage V_{in} is applied in counter-phase on electrodes 1 and 2 to force the first mechanical flexural mode. Finally, the read-out is performed through the movable structure. A DC voltage V_3 is added to the AC (V_{in}) voltage to allow the signal transduction (see equation 1).

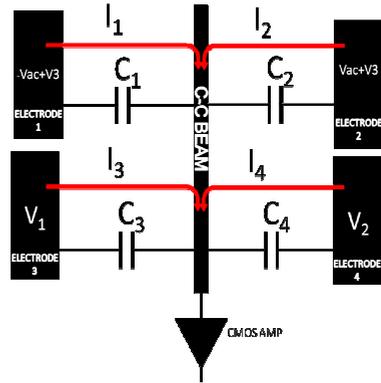


Fig. 4 > Diagram of the four electrode resonator including the excitation and biasing voltages as well as the current induced over the resonator./

Taking into account the beam movement, the variation of the capacitances at both sides of the beam (C_1 versus C_2 and C_3 versus C_4) follow the expression (3) assuming small amplitude variations compared with the transduction gap.

$$\frac{\partial C_1}{dt} = -\frac{\partial C_2}{dt} \quad (3)$$

$$I_{TOT} = \underbrace{(C_2 - C_1) \frac{\partial V_{ac}}{dt}}_{I_{F2}} - \underbrace{(C_3 + C_4) \frac{\partial (V_{out})}{dt}}_{I_{F1}} + \underbrace{\left[(V_1 - V_2) \frac{C_3}{s} + (V_1 + V_2) \frac{C_4}{s} 2 \frac{x}{s} - 2V_3 \frac{C_2}{s} \right] \frac{\partial x}{dt}}_{I_M} \quad (4)$$

Equation (4) shows the parasitic contribution due to the electrodes 1 and 2, I_{F2} , which is a direct consequence of the different capacitance value. The feedthrough current, I_{F1} , is proportional to the addition of the two control capacitances, C_3 and C_4 . Furthermore, the motional current is identified as an addition of different components where the biasing voltages, V_1 , V_2 and V_3 play an important role.

From equation (4), it is possible to note that the cancellation of the feedthrough is possible if $I_{F1} \approx I_{F2}$. Under this circumstance, the output current only originates from a pure motional behavior (I_M in equation 4).

IV. Electrical characterization

A network analyzer (Agilent E5100A) with a balun in the output port has been used to provide the input differential AC signal, in electrodes 1 and 2. The input port of the network analyzer is used to sense the MEMS output that has been previously amplified. Measurements have been carried out in air conditions. Two DC sources has been connected to the Electrode 2 and 3.

Fig. 5 shows both the magnitude and phase response of the MEMS when the control voltages, V_1 and V_2 , are set to 0 V. The parasitic capacitance current forces the 11.38 MHz resonant frequency to be followed with a parallel resonance. Finally, only a 150° phase-shift is obtained and the phase, recovers the 90° at high frequency and Q of 122.

In Fig. 6, both magnitude and phase are shown when a smart biasing of the electrodes is proposed in order to suppress the effect of the feedthrough current (V_3 is set at -36V whereas $V_1=14V$ and $V_2=1.4V$).

It is clearly seen how the proposed biasing eliminates the effect of the parasitic capacitance since the parallel resonance is not present and only a resonant frequency of 10.94 MHz is shown. Moreover, a shift phase of 180° is achieved and there is only one frequency where the phase value is zero, which is valuable when building a NEMS-based self-oscillator. The Q of the integrated resonator is 136.

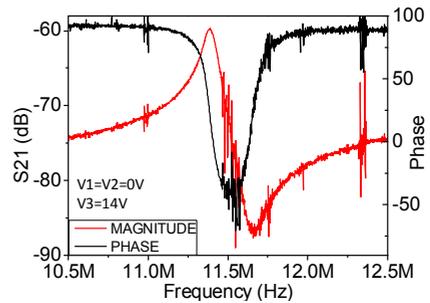


Fig. 5 > Phase (black line) and magnitude (red line) responses with non-optimized polarization./

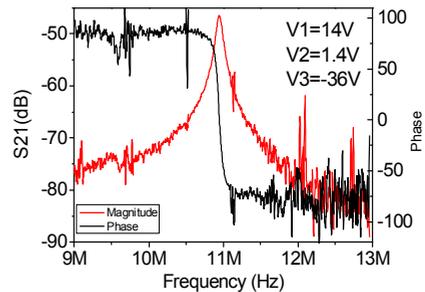


Fig. 6 > Phase (black line) and magnitude (red line) responses with the optimized polarization./

In Table II the main electrical features of the four electrodes resonator are detailed. The Input DC voltage, V_3 , is applied on the 1 and 2 electrodes. Note that the resonator is biased at the input voltage of the CMOS amplifier, which is 1.4 V thus an effective biasing voltage of $V_3=1.4V$ is in fact applied.

Parameter	11 MHz	
f_c (MHz)	11.383	10.94
Q Factor	122	136
Peak (dB)	-60	-43.5
Coupling (dB)	-75	-75
Phase Shift (degrees)	150	180
Input DC (V)	14	-36
Electrodes 3-4 DC (V)	0/0	14/1.4

Table 2 > Electrical parameters for 11 MHz C-C beam./

V. Conclusions

In this paper, a topology of smart electrodes and biasing has been presented with the clear objective to optimize the capacitive transduction method in order to suppress the feedthrough current in NEMS resonators. The results obtained in this work show a pure RLC behavior of the CC beam resonator at 10.98 MHz due to the cancellation of the parasitic current. The large phase shift of 180° of this fully-integrated approach represents an important advance to relax the constraints on the electronics in order to implement MEMS/NEMS self-sustained oscillators.

Acknowledgment

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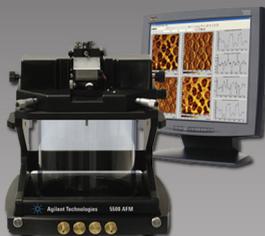
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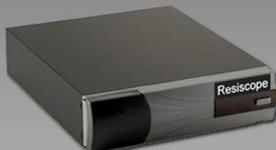
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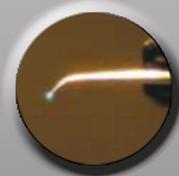
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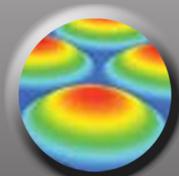
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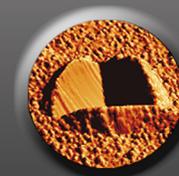
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