4. Planar multiple interconnect Atom Technology

4a. Introduction

Introduction

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Single molecule mechanics [1], mono-molecular electronics [2] and in general multi-probes experiments on atomic scale constructed devices [3] or machineries [4] are requiring a specific planar interconnection technology with a surface atomic precision and ultra cleanness [5]. This surface technology must be able to provide information and energy access channels to the atomic (or molecular) scale machinery constructed or fabricated on the surface (see Figure 1). At the end of the 80's, e-beam lithography was expected to provide such a technology [6]. But with its resist based approach (grown, deposited or contamination), e-beam lithography will not be able to make it [7]. It cannot respect at the same time the atomic scale precision, the cleanness and the expected large number N of access channels to the atomic scale or molecule machinery [8]. Alternative new surface lithography techniques such as nano-imprint [9] or nano-stencil [10] are neither adapted to encompass all the interconnection stages from the macroscopic to the atomic scale nor clean enough down to the atomic scale. At the turn of the century, this problem associated with new targets in atomic scale machineries like molecule logic gate [11], molecule-motor [1] and surface atomic scale electronic circuits [12] triggers a new approach starting at the bottom.

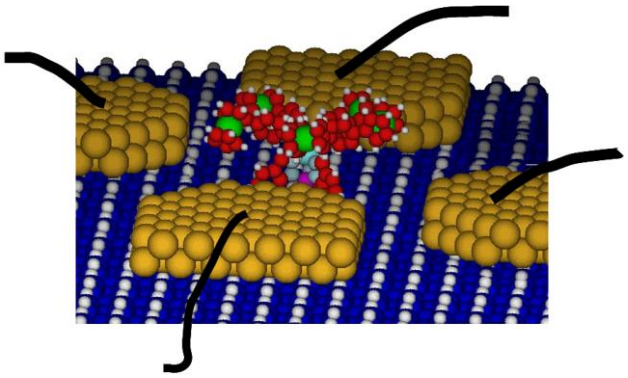

Figure 1: *A single molecule-motor [1] positioned between 4 Au nano pads constructed on the Si(100)-H surface. The motor is driven by the tunnelling electrons sequentially transferred through the motor wings. The 4 black wires getting out of the surface are indicative of the interconnections strategy to be developped.*

An atomic scale precision multiple access interconnection machine must provide N conducting wires converging toward a very small surface area where an active machinery has been constructed or assembled with an atomic scale precision. Those N interconnects are positioned somewhere on a large handle able wafer surface. As a consequence, a very efficient navigation system must be designed to locate this very small active area from a macroscopic starting point while keeping the local atomic precision of the interconnection construction. In this case, one needs to combine two type of microscope: a far field one (optical, scanning electron microscope (SEM)) for large scale navigation and a near field one (Scanning Tunneling Microscope (STM), Atomic Force Microscope (AFM)) for the atomic scale part with a compulsory overlay between those 2 types of microscopy.

In air, the combination of an optical microscope with a standard AFM to interconnect a single wall carbon nanotube on e-beam lithography metallic nano-electrodes has already shown the power of this two-microscopes combination associated with a dedicated way to electrically contact the nano-pads [14]. Those contacts were taken by introducing under the AFM head a comb of metallic micro cantilever electrodes to minimize the overall length of the electrical circuit fabricated on the wafer surface [14]. While not atomic scale, this proof of concept demonstrates all the ingredients that are at the basis of the next generation UHV and atomic scale interconnection machine as schematically presented in Figure 2.

An UHV atomic scale interconnection machine is designed to follow a dedicated interconnection sequence. On an atomically clean well-prepared surface, an atomic scale circuitry is fabricated (A). To reach a large number N of interconnects and to be able to interconnect each atomic wire to the external world, there is a necessary lateral extension of this circuit to reach N contacting metallic nanopads (B) that are positioned around the atomic scale circuit. In the example of Figure 2, a molecule is connected to these nanopads by atomic metallic wires. Depending on the electronic surface gap of the supporting material, the nanopads (B) have to be contacted from the top by a series of N atomically sharp metallic tips (C1) or by a series of N nano-scale wires (C2) up to the point where mesoscopic metallic wiring or microelectrodes (D) can be surface fabricated and contacted by a series of N micro-scale metallic cantilever (E) also from the top of the wafer. During the process, the sequence of those different steps depends on the machine and on the supporting material. What is triggering the choice of the interconnection technology between C1 and C2 (and after the need for the D and E interconnection steps in Figure 2a) is the electronic gap of the surface that in turn will determine the kind of far field microscopy to be used for navigation over the wafer surface.

For a large valence-conduction band electronic surface gap (more than a few eV up to 12 eV for standard insulators), SEM is difficult to use because the electron beam will charge the surface. In this case, an optical microscope must be used. This microscope determines the minimum length of metallic surface wiring which must be fabricated starting from the nano-pads (B) in Figure 2a toward the next contact stage based on metallic micro-cantilever (Figure 2a). Fortunately enough, with a large surface gap, the surface area of those interconnects can be expanded laterally without too much lateral leakage current between the different electrodes. This is the basic of the UHV interconnection machine described in section 3 where a low temperature approach is not compulsory but preferable.

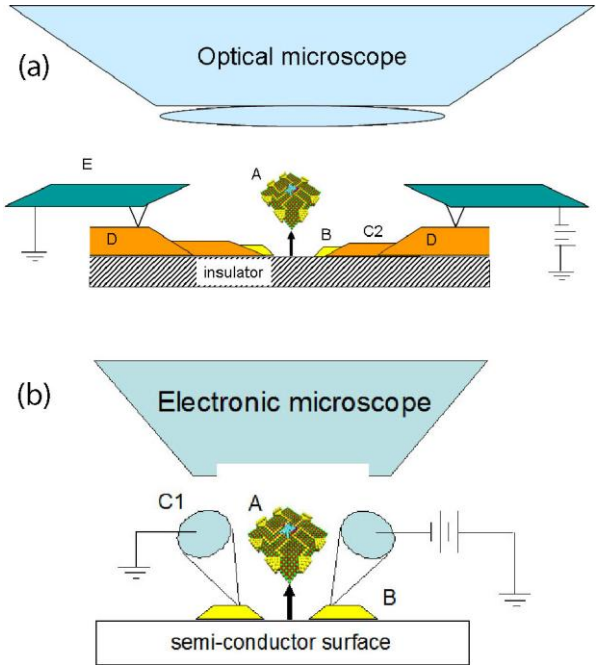

Figure 2: *Scheme of the atomic scale interconnection machines for (a) wide and (b) moderate surface band gap substrates. A: Atomic scale circuitry, B: Contacting metallic nanopads, C1: Ultrasharp metallic tips, C2: Nanowires, D: Microelectrodes, E: Metallic microcantilevers*

For a moderated valence band-conduction band electronic surface gap (around a few eV), it is not possible to use very long surface metallic circuitry due to the possible lateral surface leakage current between the surface electrodes. In this case, one solution is to use ultra sharp STM like tips positioned from the top on the surface (Figure 2b). In this case, the core of the tips will not be in contact with the supporting surface and one can go continuously from a tip apex radius of curvature of a few nanometer up to a 100 microns or more section for the tip body. In this case, navigation on the surface can be performed using an UHV-SEM (Figure 2b) by grounding the sample during the SEM imaging to avoid the surface charging effect. This is the basic of the UHV interconnection machine described in section 4. Here, a low temperature approach is compulsory because of the low electronic gap at the surface of the supporting material.

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4b. Number of interconnection steps & interconnection strategies

How to exchange information with a single molecule

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At the laboratory scale, there is an urgent technological problem to be solved: how to interconnect a molecule with the prospect to exchange information in a multi-channel configuration with this molecule? Starting from a surface science point of view, one of the Research Unit aims of the Pico-Inside project was to explore the solutions of this problem. Whatever the type of information to be exchanged, connecting a molecule to electrodes or dielectric waveguides means creating an interaction between a few parts of this molecule and the surface-end of each interconnect. From the surface science point of view adopted in Pico-Inside, any change of the detail atomic ordering at the "molecule-surface-end" junction or any change in the adsorption site of the molecule in interaction with the interconnects will modify the orbital mixing between the surface and the molecule. Then, the quality of the information exchange will be degraded.

In the following, research work of Pico-Inside partners is presented in a way to indicate the starting point of the Pico-Inside exploration of this interconnection problem. Pico-Inside concentrated its efforts on electronic interconnects meaning that only metallic electrodes issues are discussed. They also concentrated on the physical and technological aspect of the interconnects and not of the type of information to be exchanged (classical, quantum) nor on the chemical aspect of the interconnection problem.

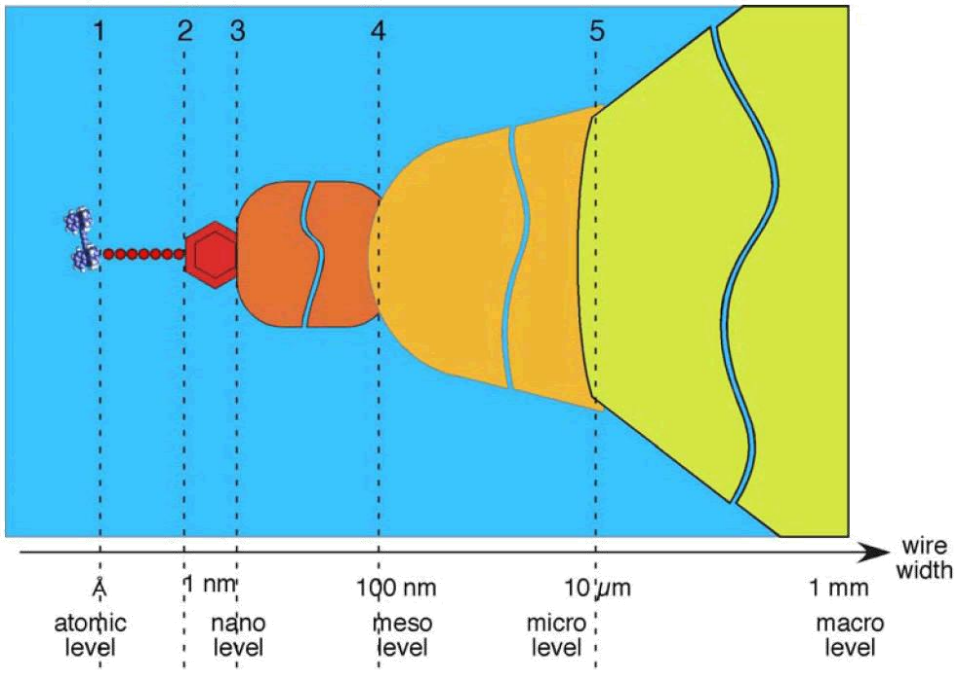

Figure 1: *The aim of Pico-Inside was to multiple connect a single molecules to the macro world under ultrahigh vacuum conditions. Different interconnections were be studied: 1) molecule to atomic wire (atomic level) 2) atomic wire to a metallic island of a few monolayers high which links the atomic level and the nano level 3) metallic island to a thin metallic ribbon which links the nano level and the meso level 4) thin metallic ribbon to micro-electrode which links the meso level and the micro level 5) microelectrode to macroscopic wiring which links the micro level and the macro level.*

In a fully planar technology, a maximum of 5 levels of interconnection is required to pass from the molecule to a macroscopic amperemeter (see Figure 1):

1. From the molecule to the atomic wires. This is the atomic scale level of the interconnects.
2. From the atomic wires to nano metallic islands, only a few mono layers in height. This is the nano scale level of the interconnects.
3. From those nano metallic islands to mesoscopic metallic wires with a width below 100 nm. This is the mesoscale level of the interconnects.
4. From those mesoscopic wires to micron scale metallic pads. This is the microscale level of the interconnects. The lateral size of those pads depending of the next level.
5. From the micropads to macroscopic wiring which links the micro level and the macro level and then to the amperemeter.

At all the levels, a major point is to preserve the cleanness of the others level of the interconnection sequence. This means that the difficult task is to determine a succession of technologies which will preserve the initial atomic scale precision of the atomic scale level of the interconnect. This requires the exploration of fabricating metallic atomic scale mesa islands on semi-conductor and insulating surface, of molecular molding and stabilisation of atomic wires, of self-assembling molecule on an insulator in a systematic way, of developing a nanostencil technique down to 10 nm and of using metallic cantilevers for the interconnect to the macroscopic level. In Pico-Inside, we will also take care of the possibility to suppress one or more of those interconnection levels to increase the reproducibility of the final interconnection chain.

The need for a first atomic scale level of interconnect is explained by a very hard geometric constrain in this multi-interconnection problem. To illustrate this point, let us remind the past tentative in another FET-IST project BUN which ended in year 2003. The problem was to use the ebeam lithography technique for the fabrication of a maximum of nanoscale metallic wires on a circle. A maximum of 20 nanoscale metallic electrodes terminated each by a 20 nm apex diameter were fabricated on a SiO_2 surface.
On this surface, those 20 electrodes open the access to an area of a diameter not smaller than 200 nm. This diameter is clearly too large as compared to the size of conjugate molecules available in our days. This geometrical constrain forces to fabricate local access on the molecule using atomic wires. But this can be considered as positive because it will force the molecular designer to integrate as much as possible the electronic functions to be performed in a small molecule. This part was worked out in the research Unit 1 of Pico-Inside.

The 5 interconnection levels can be separated in two groups. One group for the first and the second interconnect levels is relevant to surface science. The second group for the three last, can be considered as technological interconnects. Notice that these electrical contacts will be used under or near an UHV-STM or NC-UHV AFM head. Therefore, the way to fabricate the second group will depend strongly on the geometrical environment around the local STM or AFM probe. The realization of the first group will depend on the nature of the substrate (semiconductor or insulator) to be used.

4c. From the molecule to the nano-pads on a semi-conductor surface

Constructing interconnection nanostructure on the MoS_2 surface

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Introduction

As presented in section 4a, a small electronic gap (below a few eV) of the surface material supporting the interconnection structure leads to only 3 levels of interconnects. Levels (A) and (B) are depending on the mastering of atomic scale surface science phenomena while level (C2) is relying on the ability to fabricate multiple ultra sharp metallic tips to contact each metallic nano-island of level (B). With a multi-access interconnection technology on a small electronic gap surface material, the constraint is to avoid surface leakage current between the electrodes contacting the surface metallic nano-islands. Therefore, it is compulsory to contact them from the top. This constrain has a lot of consequences in the structure of the interconnection machine depicted in section 4a. In particular, a scanning electron microscope is required instead of an optical microscope because the lateral size of the nano-islands is necessary very small to avoid inter nano-island leakage current. In this section, we are presenting the progresses towards the construction of a nano-pads arrangement at the surface of a low gap semi-conductor. This was explored mainly in Singapore under the VIP A*STAR Atom Tech. project where an interconnection machine is under construction at IMRE.

Semi-conductor surface preparation

After an atomic scale UHV surface preparation, not a lot of semiconductor materials are presenting a surface semi-conductor electronic gap in the range of a few eV. Generally, the surface of these materials needs to be saturated by an ultra thin layer in charge of completing the valence of the surface atoms existing after the cleavage operation of the crystal. This is for example the case of the standard Ge and Si surfaces. While for example the native Si(100) surface gap is 1.2 eV, it reaches 2.1 eV with an hydrogen saturation in its 2x1 reconstruction phase [1]. In UHV, the preparation of such a semi-conductor surface is usually following the same procedure. After degassing and destroying the oxide layer, the surface is reconstructed by passing a high intensity current through the sample, between 8 to 12 A depending of the doping level of the bulk material behind [2]. One problem is to prepare large atomically flat terraces in the 50 nm width range with a homogeneous reconstruction all along a terrace. Another problem is that such an open surface is very sensitive to the quality of the vacuum in the preparation chamber. It is often found that without any chemical protection, a very well prepared semi-conductor surface becomes totally polluted by contaminants if the waiting time for working on this surface is too long.
Saturating these surfaces by adsorbing hydrogen, chlorine, sulfur or small molecules is a nice solution to preserve the surface integrity [3]. In many case, it is also a good solution to increase the electronic surface band gap. For example, molecular hydrogen can be cracked in front of Si(100) or Si(111) surfaces to form the hydrogen saturated Si(100)-H or Si(111)-H surfaces. But the rule is not systematic. The saturation of a semi-conductor surface not always leads to a large increase of its surface electronic gap [3]. Furthermore the phase diagram of such surfaces generally presents a surface

reconstruction temperature with the destruction of the saturation layer beginning between 300°C to 400 °C [4]. Notice that the stabilization of nanowires at the surface of an insulator is a very delicate task. With the saturation layer grown on a semi-conductor surface, an atomic surface wire is natively self-stabilized by the surface structure.

There are a few semi-conductor surfaces where this saturation is part of the material structure. This is the case of lamellar semi-conductor like MoS_2. In this case, the sulphur over layer is hardly bond to the underneath Mo atoms. The MoS_2 surface is rather easy to prepare by a very fast UHV cleaning followed by a standard surface preparation temperature in the 300°C range [5]. The extension of the atomically flat surface of lamellar compounds is usually rather large up to a few microns in lateral extension in some cases. MoS_2 is one of the most interesting materials of the lamellar compound series with a bulk gap around 1.3 eV and a surface gap in the 1.0 eV range [6]. The MoS_2 surface remains atomically perfect and flat up to 1100 K. Above 1200 K, a reconstruction of the top layers of MoS_2 to Mo_2S_3 is observed, leading to one-dimensional atomic double rows on the reconstructed surface [7]. Such temperature stability is very important for the fabrication of surface atomic wires by STM extracting rows of S atoms. The drawback is that it is extremely difficult to extract these surface atoms as compared to the surface atoms of the Si(100) 2x1-H surface [8]. There is a crucial need for a material stable enough in temperature and whose surface atom chemical stability is between Si(100)-H and MoS_2.

LT-STM surface atomic scale imaging

There is generally no STM surface imaging problem of low surface gap semi-conductor materials. STM images of the 2 principal surfaces used at IMRE in Singapore to explore atomic scale interconnection are presented in Figure 1 showing each a nice atomic resolution. For lamellar materials and at low temperature, one imaging problem comes from the softness of lamellar semi-conductor materials in the transverse direction. It is usually very difficult to record a nice current distance characteristic on these materials when changing the tip to surface distance. Therefore, this distance is not known with precision. In this condition, adsorbates or metallic nano-islands can be easily brushed away during an STM tip scan because the tip apex to surface distance can be very small during STM imaging [5].

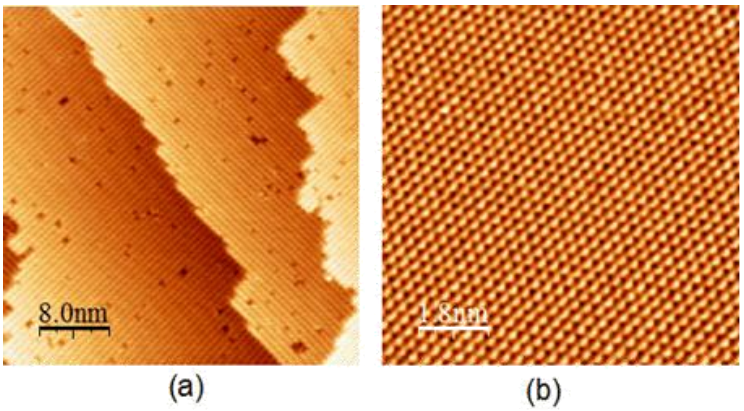

Figure 1: *Standard UHV-STM images of an Si(100) 2x1 and an MoS_2 surfaces showing the atomic resolution before the start of any construction or fabrication steps. As described in this section (and in section 3 for large gap surface materials), those construction and fabrication process must be carefully tested in such a way that this atomic resolution is kept up to the multi probes I-V measurements. (a) The Si(100) surface was prepared with the objective to increase the terrace size before the hydrogenation step V= 2 V and I = 10 pA. (b) The MoS_2 surface was prepared to study the conditions to extract the sulphur surface atoms one at a time.*

Metallic nanopads fabrication and re-configuration

On a semi-conducting surface, metallic nanopads are necessary to pass from the surface atomic wires made of dangling bond lines to the metallic tip apex. This very local metallization must be practiced directly on the passivated semi-conductor surface. It turns out that there is not a lot of passivated surface whose passivation overlayer can sustain the temperature required for metallization [11]. These temperatures are usually higher that a few hundred degrees which locally destroys the passivation. One solution to this problem is to start with a robust semi-conductor surface like MoS_2 and then to transfer the self assembled metallic nano-islands on another surface by contact printing in UHV [6].

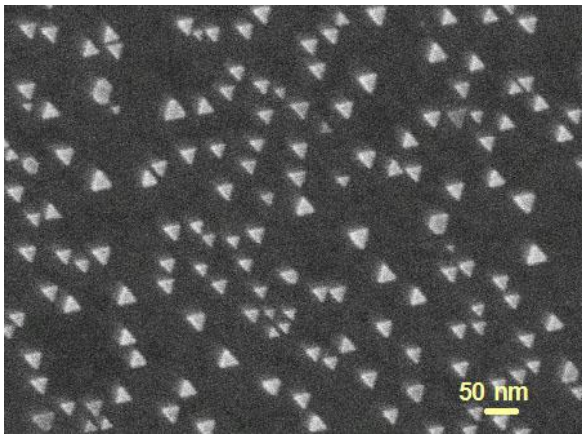

Figure 2: *SEM image of the distribution of Au nano-islands on MoS_2 after the fabrication process detailed in section 4.4. Many nano-islands are 30 nm in lateral size. Notice also the very sharp end at each summit of these triangles.*

On the MoS_2 surface, gold atoms self-assemble in triangular nano-islands whose lateral dimension can go down to 5 nm for a thickness of a few nm [5]. An optimum of 30 nm lateral and 10 nm in height can be easily obtained by tuning the surface temperature during the metal evaporation [5]. In a standard preparation, MoS_2 wafers are fabricated from bulk molybdenite stones directly mined in Australia. The slides are cut into 10 x 10 mm^2 pieces. The top surface of a MoS_2 slide is cleaved and immediately loaded in a thermal evaporator. After the sample is outgassed at 400 ºC for 3 hours, Au is thermally evaporated onto the MoS_2 surface at 400 ºC with a deposition rate of 0.02 nm/sec. The total thickness of evaporated Au, monitored by a quartz microbalance, can be kept as low as 1 nm. After Au deposition, the sample is maintained at 400 °C for another 1 hour to facilitate the self-assembly of crystalline Au nano-islands on the MoS_2 surface. During processing, the vacuum in the chamber must be better than 2 x 10^{-5} Pa. The nano-island growth conditions can be optimized to achieve a majority of nano-islands to be equilateral triangular shape with a 20 to 30 nm lateral size (see Figure 2).

Such a fabrication and self assembly process usually leads to a rather homogeneous distribution of Au nano-islands. In some cases, the apices of 2 nano-islands can be face-to-face at distances as low as a few nanometers, constituting fantastic ultra-clean and atomically well-ordered nano junction to interconnect a single molecule since the background surface has generally kept its atomic scale corrugation. Unfortunately, the MoS_2 electronic surface band gap is too small for the "nano-island - surface - nano-island" conductance to be much smaller than the one of a conjugated molecule to be interconnected. Therefore, we have learnt the conditions to manipulate those nano-islands one by one on the MoS_2 surface [5]. There are 2 modes of manipulation. In the soft one, the tip apex is not mechanically touching the nano-island but is charging it. A large numbers of scans are necessary to charge a nano-island enough for the electrostatic force between the STM tip apex and the nano-island to be large enough for the nano-island to move away but with a precision better than 0.1 nm [5]. In the mechanical mode, the tip apex is simply pushing on a facet of the nano-island. This mode of manipulation is less precise (1 nm or more) but very fast [5]. Figure 3 is

presenting a few examples of Au nano-pads nanostructure arrangements constructed by manipulating the nano-islands one after the other.

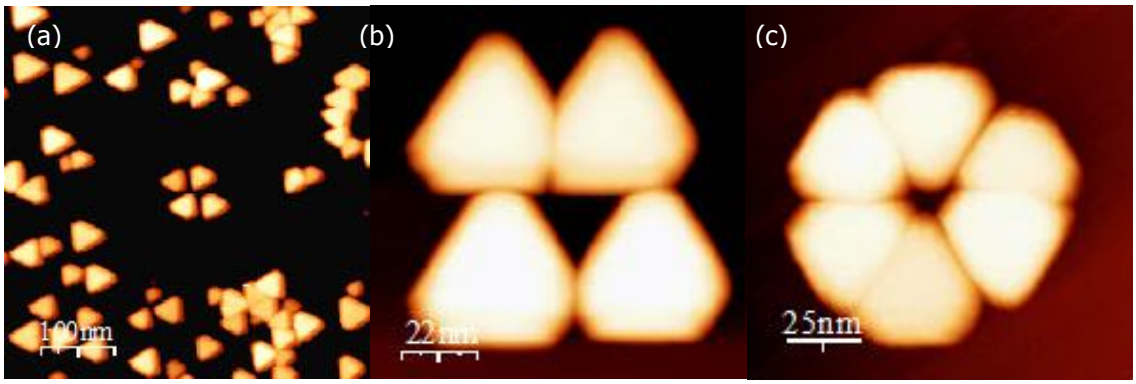

Figure 3: *Example of contacting nanostructures constructed by manipulating the nano-islands one after the other in a lateral STM manipulation mode on the MoS_2 surface. (a) More than 50 nano-islands have been manipulated around to assemble the central 4 contacting nanostructure. (b) Zoom on a peculiar construction of 4 nano-islands manipulated in a square. (c) Zoom on a peculiar construction of a 6 nano-islands interconnection structure converging toward a 12 nm central active area where the atomic circuit is supposed to have been atomically fabricated before this construction. (a), (b) and (c) are UHV-STM images recorded on MoS_2 with V = 0.2 V and I = 10 pA.*

These constructed nanostructures cannot be transferred as such by a direct contact printing on a larger gap semi-conductor surface. First, the construction will be deformed during the printing. Secondly, for interconnecting a surface dangling bond interconnecting circuit, it is better to manipulate the nano-islands after the fabrication of the surface atomic wires. In this way, a given metallic nano-island can be manipulated step by step over the corresponding atomic wire up to the point where the contact conductance is lower than the surface leakage conductance. We have recently demonstrated that Au nano-islands can be transfered from the MoS_2 surface to a Si(100)-H surface [12]. For this to occur, the MoS_2 surface must be structured in micron scale pillars creating a matrix of stamps [12]. We have shown that Au nano-islands can be fabricated on the surface of each pillar after changing the characteristic fabrication temperature [12]. A 10 % overall transfer rate to Si Si(100)-H was obtained for 10 to 20 microns lateral size pillars [12]. The experimental conditions remain to be determine to STM manipulate these nano-islands at the Si(100) 2x1 H surface as it was done on the MoS_2 surface. Notice also that the hydrostatic pressure during transfer printing must be optimized to preserve the Si(100)-2x1-H hydrogen passivation layer under the nano-islands.

Conclusion

After preparing an ultra clean MoS_2 semiconducting surface, we have self assembled on this surface a random distribution of metallic nano-islands with an average lateral size in the 30 nm range for a thickness around 10 nm. After the growth and surface diffusion processes of the metal atoms on the MoS_2 surface, the atomic resolution is preserved on the MoS_2 surface. Then, we demonstrated how single gold nano-islands 30 nm in size and 12 nm in height can be manipulated at room temperature with a UHV-STM, on this MoS_2 surface and with an appropriate choice of STM feedback parameters reaching a precision better than 0.5 nm. The precise manipulation of single ultra-flat metallic nano-islands on a semiconductor surface is a new way of constructing planar metallic contact pads to interconnect an atomic wire or a molecule to macroscopic probes, preserving the atomic cleanliness of the surface. Commercially

available UHV compatible multi-STM systems, where each tip apex is positioned independently on a surface using top SEM imaging, provide direct electrical access to the constructed 4-pads nanostructures without the usual nanolithography techniques.

Acknowledgments: We would like to thank A*STAR and IMRE for financial support of this work under the VIP A*STAR Atom Technology for molecule logic gate program in Singapore.

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Gold-alloy nanowires: a high resolution STM imaging

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Keywords: InSb, nanowires, thermally-assisted assembling, high resolution STM imaging

Successful communication between nano- and micro- environment of the molecular electronic device is a crucial ingredient of the future nanoelectronics. One has to interconnect a single molecule, designed to perform particular tasks within a circuit, with other parts of the circuit, especially with a circuit's output interface. Fabrication of gold nanowires on InSb by means of the thermally-assisted assembling process seems to be a promising solution for such a task. Indeed, for specific range of the sample temperatures during gold deposition, micrometer-long conductive nanowires aligned along the surface reconstruction rows of In-terminated (001) c(8×2) face of InSb may be manufactured [1;2].

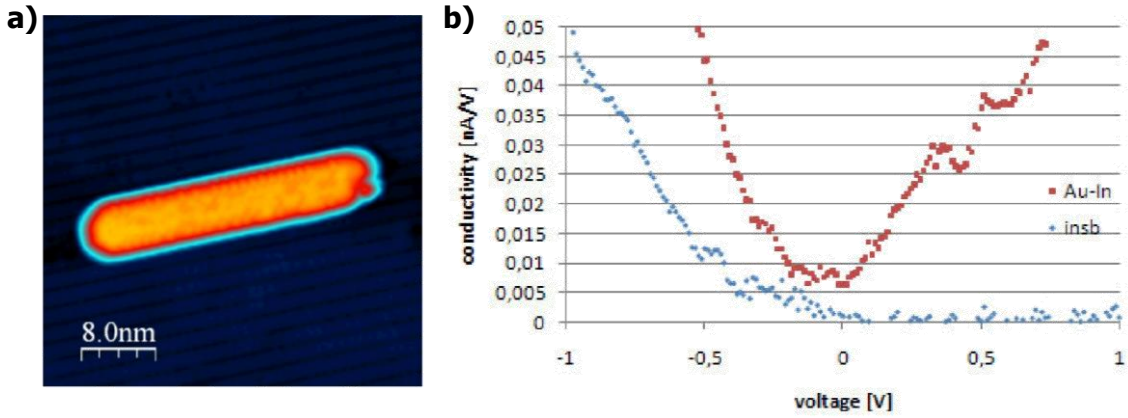

***Figure 1**: (a) High resolution STM image of gold nanowire formed on InSb(001) surface. Bias voltage: -0.5V, tunnelling current: 25pA. (b) Conductance as a function of bias voltage for gold alloy nanowire (red dots) and InSb substrate (blue dots)*

With use of various scanning probe methods (SPM) structural and electronic properties of the nanostructures have been studied in great detail. Experiment was performed in a ultra-high vacuum system equipped with a low temperature scanning tunnelling microscope (LT-STM) commercially designed by Omicron. Gold has been evaporated on atomically flat and clean terraces of (001) reconstructed surface of InSb crystal. Evaporation rate was controlled through a quartz crystal microbalance. InSb samples (Kelpin Crystals) were pre-annealed to 650-750 K and then hot samples were cleaned by ion sputtering with a 700 eV Ar^+ beam [2]. The quality of the surface was controlled with the low energy electron diffraction (LEED) and the STM techniques. During the evaporation several substrate temperatures in the range of 300-700 K were used, as well as, post-deposition thermal annealing. Image processing and analysis was done by means of WSxM software [3].
For a specific sample temperature window, i.e. 600-650 K, narrow, long, with a length up to 800 nm, structures were formed. The height of such nanowires was in the range

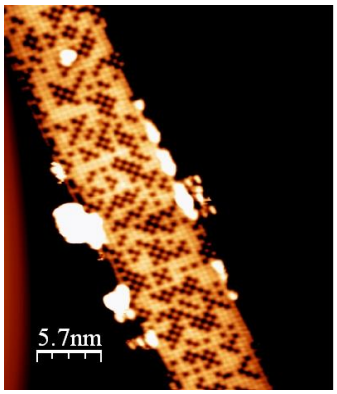

Figure 2: *High resolution image of $AuIn_2$ alloy nanowire; bias voltage: -2V, tunnelling current: 5pA.*

from 0.8 to 1.5 nm and their width was in the rage from 5 to 20 nm. In Figure 1(a) gold nano wire on InSb(001) is presented, its orientation along the [001] direction (atomic troughs of the reconstructed InSb(001) surface) is clearly seen, as well as, atomic resolution on the top of the wire. Spectroscopic data for the gold nanostructure and for the substrate are presented in Figure 1(b). Conductance vs. bias voltage plot indicates different electronic properties of the nanowire with respect to the sample, supporting an earlier conclusion on a metallic character of the former [1;2]. Moreover, detailed analysis of the nanowire structure with atomic resolution suggests, that during gold deposition a gold-indium alloy is created rather than a pure gold structure (see Figure 2).

As already noted, a crucial parameter appears to be the substrate's temperature during gold deposition. However, it was found that also the time of cooling of the sample plays an important role. During the Au deposition the substrate surface undergoes considerable reorganization and if the sample temperature after the evaporation process was quickly decreased, a distorted substrate could be observed (see Figure 3). Further annealing of the sample to the deposition temperature led to reconstruction of the substrate (see Figure 4). It could be noted in Figure 4(b), that lower terrace of the wire exhibits the same structure as the substrate and the upper terrace appearance is significantly different. The upper terrace also includes other than gold atoms as indicated by dark spots in Figure 4 in agreement with previous observation on the alloy nature of the wire (compare with Figure 1) Such an observation suggests, that the lower terrace is created during the reconstruction of the distorted surrounding of the nanowire, while the upper terrace is the intrinsic gold alloy nanowire.

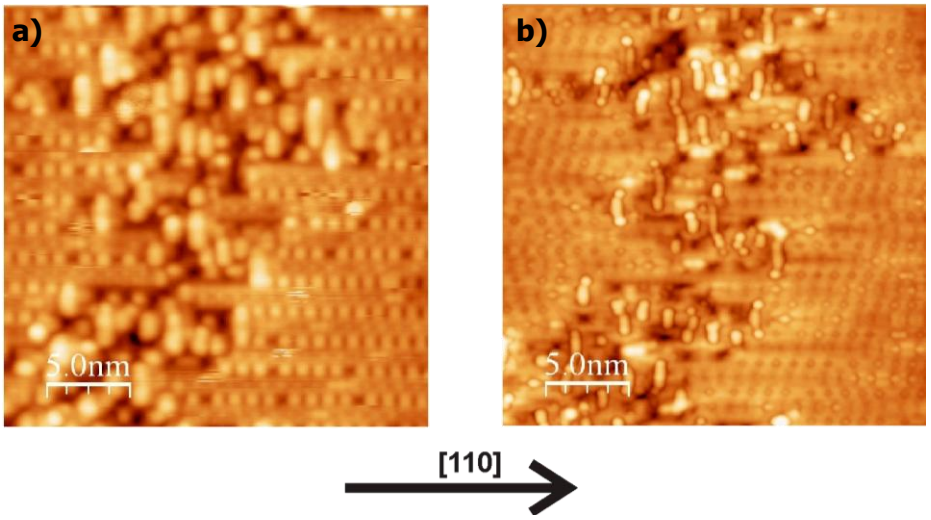

Figure 3: *InSb(001) surface distorted during gold deposition. The sample was relatively quickly cooled down after evaporation process was ended. (a) bias voltage: 2V, tunnelling current: 100pA; (b) bias voltage: -0.5V, tunnelling current: 100pA.*

One could expect similar temperature controlled assembling process for other atomically ordered surfaces of A_{III}-B_V semiconductors, such as InAs(001) or GaAs(001). However, gold deposition on InAs and GaAs surfaces under the same condition as for InSb did not lead to formation of wire-like structures. This observation could be attributed to the different reactivity of gold to the respective substrates [2].

Summarising, micrometer long, conducting nanowires could be fabricated via gold deposition on InSb for substrate temperatures during the deposition being in the range 600-650 K. Nanowires are perfectly oriented along the reconstructions troughs of (001) InSb face, as revealed by SPM measurements. Metallic character of the structures is confirmed by spectroscopic data and high resolution STM measurements suggest the gold alloy nature of the wire. During the gold deposition substrate undergoes considerable reorganization leading to the distortion of the surface reconstruction. The latter is restored via post-deposition thermal annealing. Gold nanowires could not be created for InAs and GaAs (001) surfaces.

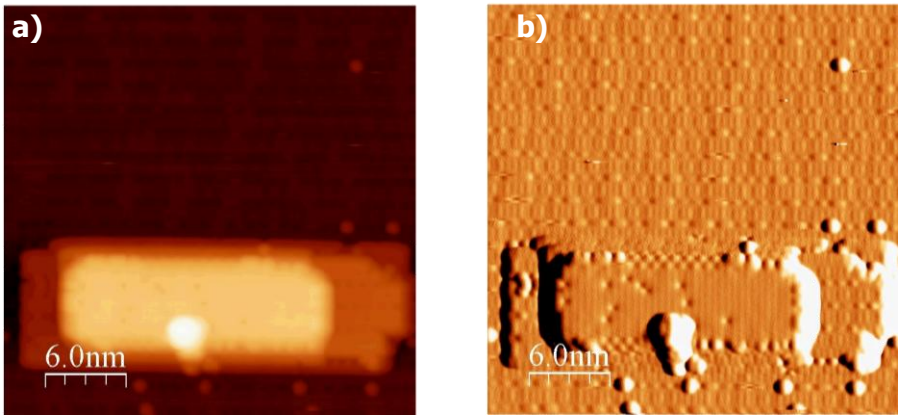

Figure 4: *STM scans showing gold alloy nanowire with surrounding substrate surface reconstructed via post-deposition annealing. Bias voltage: -2V, tunnelling current: 100pA. (a) topographic image; (b) error signal.*

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4d. Optic navigation and interconnection

Nano level to macro level interconnects through static and nanostencil techniques

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1-General description of the micro cleanroom for Pico-Inside

The aim of this part is to obtain an electrical contact of low resistance between a thin metallic pad 10 to 100 nm wide and a macroscopic wire. One possibility is to add each interconnect (3 to 5) by different techniques: the micro clean room developed in the Nanoscience Team of the CEMES institute at Toulouse is based on this solution. Indeed the interconnect 3 is obtained by dynamic nanostencil [1], the interconnect 4 by static stencil, and the last one by microcantilever array as shown schematically on the Figure 1. The two last steps 4 and 5 have been already tested in air using e-beam lithography nanowires ending by 2x2 μm^2 pads which are contacted with a metallic microcantilever array [2].

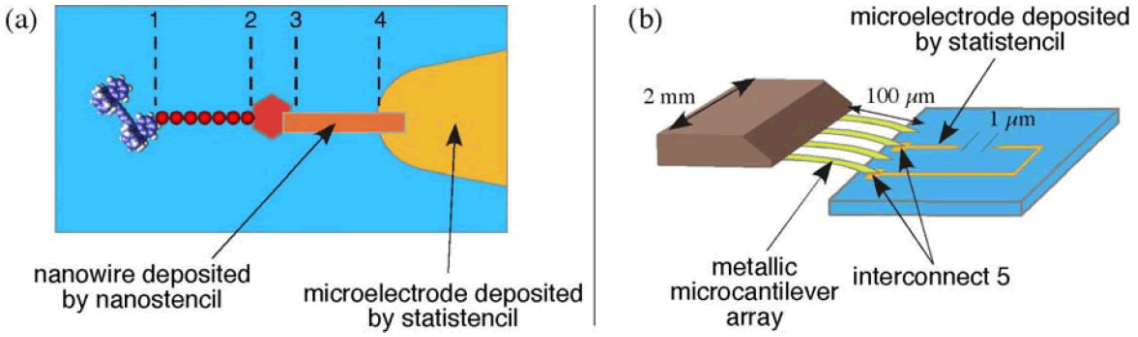

Figure 1: *In the GNS group of Toulouse, the interconnects 3 and 4 are made by nanostencil with the micro cleanroom (a), and the interconnect 5 consists of a metallic microcantilever array contacting pads at the end of microelectrodes deposited by the static stencil process.*

The first step is the growth of microelectrodes on the substrate by the static stencil process which is evaporation through a thin membrane bored by the desired pattern. Then the interconnects 3 and 4 between the end of one microelectrode and a thin metallic island are made by depositing a small wire with the nanostencil process which consists to use a drilled cantilever as a shadow mask to write on the surface [3]. And the last interconnect 5 is done by positioning the extremities of metallic microcantilevers array (microcomb) on pads at the end of the microelectrodes.
To do successfully all these steps, one needs to 'see' at different scale. For the last interconnect, the microcomb should be positioned at a micrometer scale, so a direct vision of the scene by the way of an optical microscope is sufficient. This optical microscope is also useful to approach the cantilever close to the microelectrodes array. However to find the area between electrodes, it is necessary to see at sub-micrometer scale but on a wide range of several tens of micrometers.
The UHV micro cleanroom developed in the GNS group of Toulouse has all these functionalities. As presented on the Figure 2, it is a commercial VT AFM/STM Omicron head which has been modified.
The first modification was to add a flexural-hinge guided (XY) table (100 µm x 100 µm with a repeatability of a few nanometers) which carries the Omicron sample plate. With this table, it is possible to do wide scale AFM/STM images, greater than those obtained

with the normal Omicron piezo tube which supports the tip or the cantilever. And the repeatability of a few nm allows a "blind" (ie without AFM imaging) positioning of the cantilever on the surface. Combined with an effusion cell highly collimated on the cantilever, it allows the growth of nanowires (nanostencil process). The positioning of the microcomb is realized by an (XYZ) piezo table under an optical microscope.

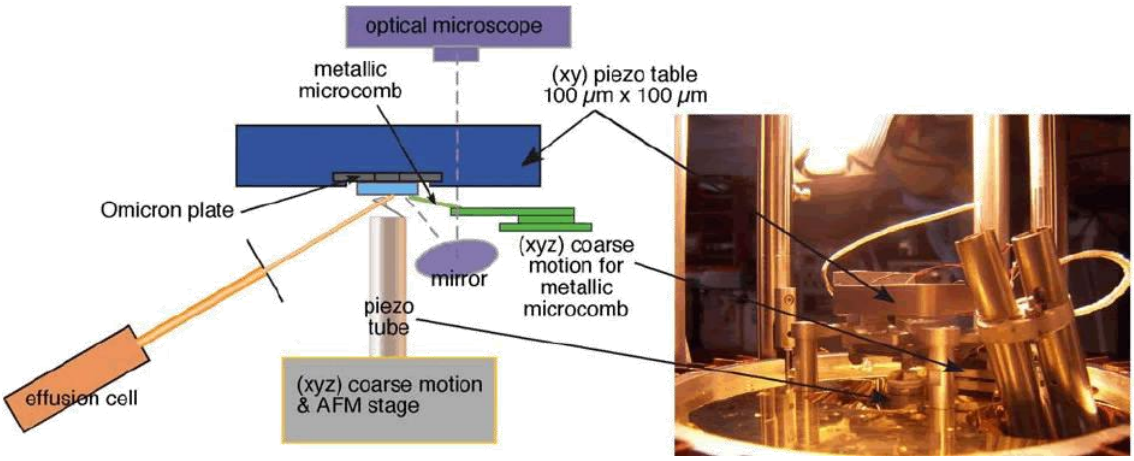

Figure 2: *The micro cleanroom developed in the GNS group is based on a VT AFM/STM Omicron head which has been modified: the Omicron plate is now placed on a (XY) piezo table allowing fine motion on a (100 µm x 100 µm) area, an (XYZ) table allows the positioning of the microcomb, and the scene is seen through an optical microscope.*

2-Technical description of the nanostencil stage

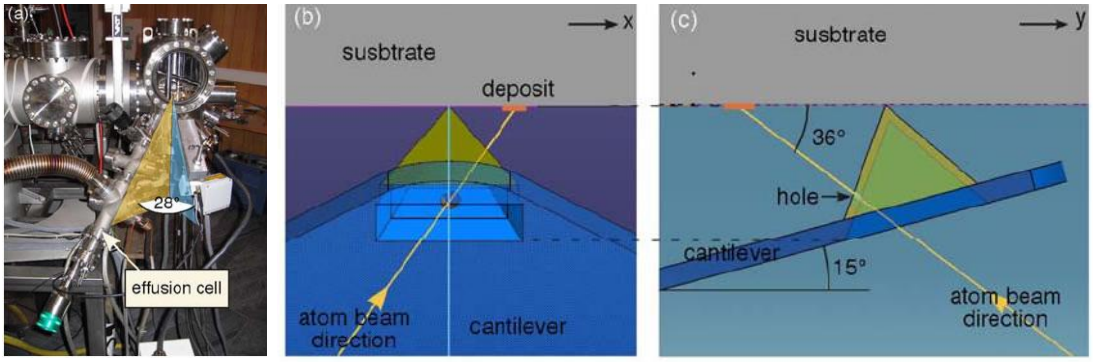

Figure 3: *(a) an effusion cell is mounted on the VT AFM/STM; (b) and (c) plane view of the cantilever tip on the surface along the y axis and x axis of scan respectively.*

The quality of the nanostencil process depends strongly on the geometrical position of the metal source, the drilled cantilever and the surface. Figure 3 presents our configuration.

The effusion cell is mounted directly on the VT AFM/STM UHV chamber: the geometry of the flange defines two angles for the atom beam direction. The first one is between the two vertical planes passing through the atom beam and the y direction of scan and is equal to 28°. The second one is defined by projection on the vertical plane passing through the y direction and is equal to 36°. This geometrical configuration is reproduced when fabricating the drilled cantilever by FIB. Indeed the

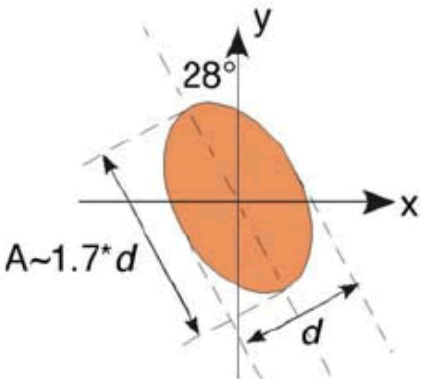

Figure 4: *The image of a circular hole made by FIB on the cantilever tip will be an ellipse on the surface sample.*

holes of the desired figures are drilled with a focused ion beam oriented in the same direction than the atom beam of the effusion cell. The image of a circular hole made on the cantilever tip will be an ellipse with the main axis oriented at 28° from the y scan axis as shown on Figure 4.

3-Some results obtained by the nanostencil process

To observe the distortion induced by the position of the effusion cell, an experiment was done with a cross drilled on the cantilever tip as presented on Figure 5(a). To decrease the clogging effect during metal evaporation, the first thing done by FIB is to thin the side of the cantilever tip until a thickness of around 100 nm. This leads to the formation of a box where the desired pattern is drilled. Here we choose a cross with eight lines having between them a similar angle of 45°. After deposition of 4 nm of Titanium on a silicon substrate, we evaporated 50 nm of silver through this drilled cantilever. Our (XY) sample table allows us to obtain wide scale STM images of the deposition as presented on Figure 5(b).

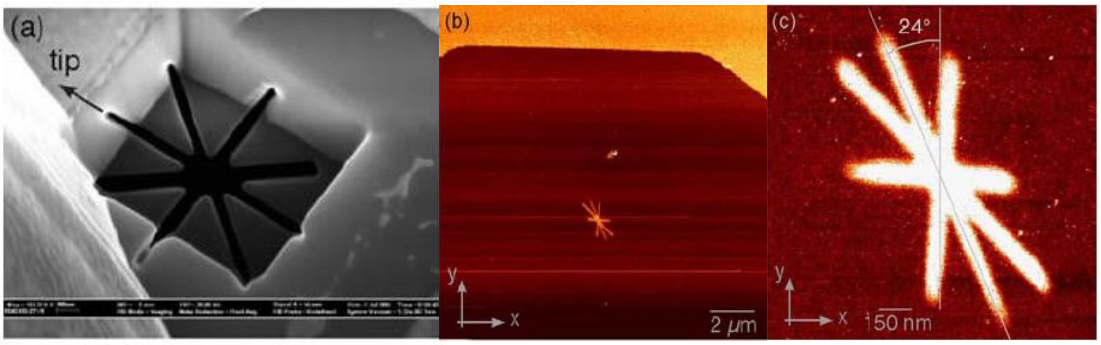

Figure 5: *(a) SEM image of the cross drilled by FIB on one side of a cantilever tip ;(b) wide scale STM image (15 µm x 15 µm) obtained by moving the sample with the (XY) table; (c) 1.5 µm x 1.5 µm STM image showing the silver cross deposited.*

The ability to do wide scale STM image allowed us to find rapidly the small cross: we can see on this wide scale STM image the shadow of the cantilever, and the silver cross deposited through the drilled pattern. A closer view obtained also by scanning with the (XY) table allows us to determine precisely the distortion induced by our geometrical configuration. For example we can measure the angle between the y scan direction and the line passing through the end of the cantilever tip. As this line should be in a vertical plane parallel to the y scan direction, we should obtain 28° after deposition. We measure only 24°, the difference is probably due to the misorientation of the cantilever during the gluing on the holder. Such a misorientation is observed on the wide scale STM image (see Figure 5(b)) and adds 2° to the measured angle, which gives a value of 26° closer to the 28° expected.
The nanostencil process allows us to deposit a desired pattern directly on a surface without using an etching process. To successfully contact a molecule we need to draw a thin line between a metallic pad and a microelectrode. This means that we will evaporate through a hole drilled in a cantilever tip while moving in the same time the substrate to connect the two objects. However the atoms of the beam stick also on the cantilever and after a while the deposit formed on the edge of the hole will clog it. This well known phenomenon [4] is the main disadvantage of the nanostencil process. To study it we drilled a cantilever tip with five holes of increasing diameter from 32 nm to 200 nm as presented on Figure 6(a).

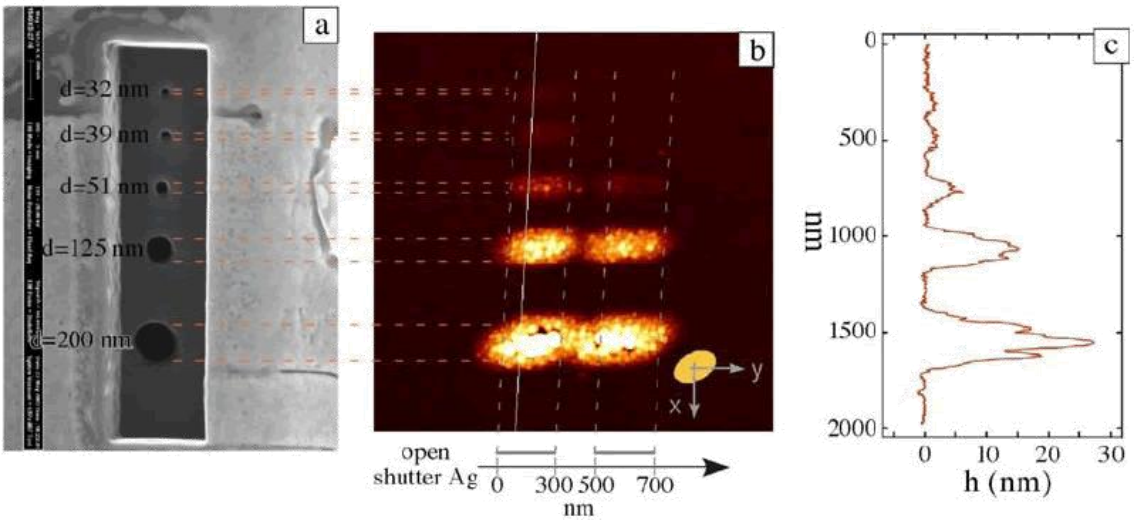

Figure 6: *(a) 5 holes of increasing diameter drilled on a cantilever tip; (b) AFM image after deposition of silver (48 Å/mn) while moving the substrate at 20 nm/mn; (c) cross section along the white line.*

We used this drilled cantilever to draw two lines of silver of 300 nm width, and separated by a gap of 200 nm. The silver flux is equal to 48 Å/mn and the sample is moving along the y axis with a speed of 20 nm/mn. The shutter of the silver cell was open and closed in order to obtain the described pattern. The AFM image presented on Figure 6(b) shows clearly large differences depending on the diameter of the holes. For the two small holes (32 and 39 nm), only the first line is drawn: after the two holes are clogged. The third hole (ø=51 nm) is clogged at the end of the second line and the two bigger ones are not clogged after the deposit of 120 nm of silver. A careful analysis of the pattern obtained with the smaller holes gives a thickness of clogging equal to three times the diameter of the holes. Another effect observed on the AFM image is the ellipsoidal shape of the lines due to the geometrical configuration of our system.

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