5. Conclusion

Mono-molecular electronics on a surface: challenges and opportunities

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1. Introduction

Technology continues to produce functioning transistors on ever smaller scales. The day will come soon, however, when there will not be enough atoms on the surface of a semi-conductor to define the structure of a transistor and, consequently, of complex electronic circuits. At this stage, new approaches and new technologies are necessary for building computers, memory or telecommunication devices [1]. Anticipating this challenge, researchers in a few laboratories around the world are now looking for the minimum number of atoms required to fabricate, for example, a calculating unit able to perform a computation by itself. This problem of creating an atom based technology is not limited to electronics or to telecommunication and encompasses all types of devices, including mechanical machines and transducers.

Meeting the atom technology challenge for ICTs requires new understanding in four now well identified fields of science and technology:

1. Learning the kinds of architectures for molecule-machines (or atom surface circuits) which will permit to perform for example complex logic operations stabilized at the surface of a solid where the required interconnection will be constructed.
2. Creating a surface multi-pads interconnection technology with a picometer precision, respecting the atomic order of the surface which is supporting the nano-system assemblage.
3. Cultivating molecular surface science accompanied with molecule synthesis (respectively atom by atom UHV-STM fabrication on a surface).
4. Creating a packaging technology able to protect a functioning atom-technology-based machine, while at the same time insuring its portability.

Those 4 topics were discussed during the 1st nanoICT mono-molecular electronics Working Group meeting in Toulouse, France between the 8th and the 10th of December 2008. Most of the participants of this meeting have worked 3,5 years

together on the Pico-Inisde project. So, this meeting was also a conclusion of the Pico-Inside project.

2. The architecture

As recalled in the introduction, Molecular devices i.e. hybrid molecular electronics are on the agenda of the micro-electronics roadmap since the seminal Aviram-Ratner paper in 1974 [2]. Until the turn of the century, such a futurist possibility of using molecules instead of solid state devices for electronics was just considered as a game for exploring the limits of calculating machines and memory devices. Approaching the end of the ITRS roadmap, things are now changing. Thanks to an intense experimental and theoretical effort, molecular electronics has now positively evolved from concepts to the first measurements and comparison with calculations [3]. There is now a real shift towards the full integration of a computing power in a single and the same molecule i.e. the mono-molecular approach [4]. This is now followed by exploring also the possibility of using atomic circuit fabricated on the surface of a passivated semi-conductor surface for implementing quantum dot based computer approach [5] and may be one day a mixture of both approaches.

The different possible architectures for a single molecule (or an atomic circuit) to compute include i) the design of single molecule circuits in a standard electrical architecture, ii) electronic wave-like atomic or molecule circuits located on the surface of a semi-conductor and iii) the quantum Hamiltonian like computing architectures. All those approaches are now studied by quantum chemistry software able to take into account the surface electronic structure, the interconnects and the local quantum structure of the computing circuit. Let us take the simple example of a logic gate.

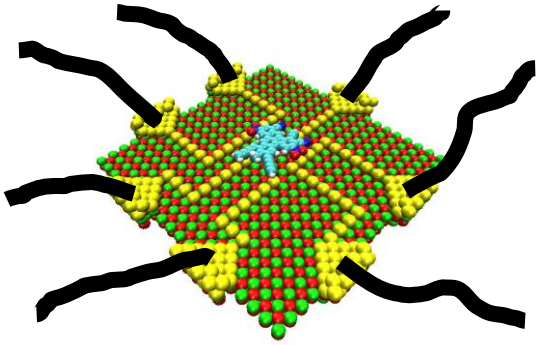

Figure 1: *A possible surface implantation of a molecule logic gate. The presented molecule half adder was designed following a Quantum Hamiltonian Computer approach [9]. The interconnection architecture is constructed using metallic atomic wires. The logic inputs are located directly on the molecular board, supposing 2 switchable chemical group current driven inputs.*

There are 3 ways of designing a logic gate at the atomic scale:

(1) The use of surface missing atom to fabricate an atomic scale circuit mimicking the topology of a macroscopic electronic circuit. Those surfaces are generally passivated semi-conductor surface with a relatively large gap. Atoms are extracted one at a time to create a specific surface electronic structure in the electronic surface gap. This new electronic structure will form the surface atomic circuit [6]. The STM vertical manipulation of the single surface atoms can be automated and proceed in parallel.

(2) The full molecule, instead of the surface can be the electronic circuit. In this case, it is the π system of such an extended molecule which will define the circuit and the σ skeleton will ensure the full chemical stability of the molecular architecture [7]. Such a molecule will have to be directly chemisorbed to the required number of nanometallic pads or in a very dedicated approach to surface atomic wires more able to interact with specific part of the π molecular orbitals.

(3) Molecular orbitals (from a large molecule or defined from a specific surface atomic circuit) can be manipulated by chemically bonding on the π conjugated computing board specific chemical groups able to shift the corresponding molecular states [8].

Switchable lateral group can be very active playing donor or acceptor group to modify very locally the nodes distribution of a give molecular orbital. Such an effect can be used to design single molecule logic gate (See Figure 1) without forcing the molecule to have the topology of an electrical circuit [9].

Solutions (1) and (2) have been proposed long ago but are not very compatible with the quantum level where those atom circuits or molecule logic gate are supposed to work. For solution (3), a quantum Hamiltonian design of AND, NOR and even halfas adder logic gates have been designed followed by proposal of chemical structure functioning on the manipulation of molecular orbitals [9]. Extreme care has to be taken here for the optimisation of the chemical structure of those molecule-gates taking into account their future adsorption for example on a passivated semi-conductor surfacepresented above [10]. In particular, the optimisation of the electronic contact between the surface atomic wires and the molecule will be obtained by selecting with care the chemical composition of the end group of the molecule [11] for running current through the gates with the objective to reaching peak values in the range of 10 to 100 nA.
All those architectures provide an indication of the richness of possible quantum behaviours able to be mastered to design a molecule like logic gate up to the complexity of a digital 2 by 2 full adder. At the Working Group meeting, the question was: to what extend the complexity of such a logic function embedded in a single molecule or in a small amount of dangling bond created on purpose on a surface can be increased up for example to a N x N full adder. There is no theoretical answer yet to this question. But the interesting fact is that a careful quantum design will certainly shift up the elementary physical unit of a logic circuit from the transistor level to a logic function level. For example, no gain at the gate level is required in the Hamiltonian logic gate approach. This will simplify a lot the interconnections and the wiring. But at the same time, cascading the building block at the logic gate level will certainly require some power gain. This will consequently increase the complexity of the interconnection procedure in between the logic gate units. The quantum designer will have to define the most interesting building block complexity (of course beyond the transistor) to find an optimum between the computing power on board of a molecule and the required interconnects. There is no solution yet for designing dynamic memory cell at the atomic scale.

3. N-Interconnects

Creating ultra precise interconnects on a single molecule has often been a bottleneck for molecular electronics [4,12]. But there are now two well-known avenues to realize a full interconnection scheme depending if the supporting surface is a small or large electronic band gap semi-conductor. The first tentative characterization of a single molecule switch was reported already in 1988 using an HV-STM machine [13]. Since then, a lot of progresses have been accomplished using the end atom of the STM tip apex as a pointer to contact one atom [14], one molecule [3,15] and to practice single atom or molecule manipulation [16,17]. The first measurement of the conductance of a single molecule was realized in 1995 with a single C60 molecule using an UHV-STM machine [3].

In parallel, nanolithography has been developed to quit the vertical STM interconnection configuration for a fully planar configuration. In year 2001, what is considered now as the nanolithography limit was reached. The world record of an inter-electrode distance of 2 nm was obtained between 2 metallic nano-electrodes fabricated on a silicon oxide [18]. But this nanotechnology technique was progressively

abandoned because (1) it is limited to a maximum of 2 to 3 electrodes [19] and (2) the use of resists and chemical in the process to define the nano-fabricated pattern is not clean enough with respect to the size of a single molecule and the order of the surface atoms. As a variant, break-junctions are also now used because of the very unique precision in the tuning of inter-electrode distance [12,20]. But it was analysed by the participants of the meeting that this fantastic technique will progressively be abandoned because there is no way to determine the number of molecule in the junction, because the conformation of the molecules located in this junction is unknown and because it is difficult to foresee a multinano-electrodes version of the break junction technique.

In 1999, a new planar nano fabrication technique, the nanostencil was introduced in an attempt to solve the surface cleanness problem [21]. Then, nanostencil was proposed as a new way to interconnect electrically a single molecule. Nanostencil has a great advantage over nanolithography because it is supposed to preserve the atomic cleanness of the surface supporting the planar interconnection electrodes. By varying systematically all the parameter of the nanostencil technique, including the testing of a large variety of surfaces from SiO_2 to NaCl or mica, it was demonstrated that on good surfaces, this technique reaches its limits in the 20 nm range with no possibility to master the atomic structure at the end of the so fabricated nano-pads [22].

Facing this interconnection problem, lab scale experiments were performed: the fabrication of a pseudo-planar interconnection on metal surface taking benefit from native mono atomic step edge and designing specific Lander molecules with legs to level up the molecular wire as compared to the mono atomic step edge [11,15,23]. Those low temperature UHV STM experiments unambiguously demonstrated the need for an ultra clean atomic scale mastered interaction between for example the molecular wire end and the conducting contact entity [24].

It seems that all the standard planar interconnection strategies explored since the end of the 80's like e-beam nano lithography, nano-imprint and Nanostencil will soon be abandoned for mono-molecular electronics. A new surface science approach respecting the exact atomic order of the surface with an interconnection precision better than 0.1 nm between the atomic wire (or the molecular wire) and the atomic scale pads will have to be developed. This challenge triggers a new approach for interconnects, a formal generalization of the technique developed at Bell labs in the 50's to interconnect a bar of a Germium semiconductor material (See Figure 2). At that time, 4 probes measurement were practiced using 4 metallic tips approaching the semiconductor bar under an optical microscope. The bar was manipulated by micro metric screws together with the tips and stabilized by metallic springs [25].

In our days, atomic scale interconnection machines are starting to be built in a few labs around the world. There are basically low temperature (LT) UHV machines made of 3 LT UHV interconnect separated chambers, one for the atomic scale preparation of the supporting surface, one for single atom or molecule manipulation and one for the atomic scale to mesocale or more interconnection procedure. Depending on the surface, the navigation on the surface is still using an optical microscope completed by a NC-AFM for a large surface electronic gap (See Figure 2). For small gap passivated semiconductor surface, the navigation is ensured by an UHV-SEM with a resolution generally around a few nanometers (See Figure 2). For the nano interconnection step, well faceted and ultra flat metallic nano-island are now in use. Those nano-interconnect pads are positioned at will with a 0.1 nm precision on the surface using the manipulation ability of the STM [26]. For the nano to meso and more interconnection stage, one technique for small gap semiconductor is to use multiple

conducting STM tips in a top or back surface approach. For large gap surfaces, the nanostencil technique can still be used at its 20 nm in width limit and in its dynamic form [27].

Those interconnection machines are so new that it is not clear how one can build up a roadmap to anticipate how many contacts it will be possible to achieve. In the case of multiple STM tips positioned under the SEM, 4 is the actual limit for stability of the interconnects even if system up to 12 STM tips have been proposed (See Figure 2).

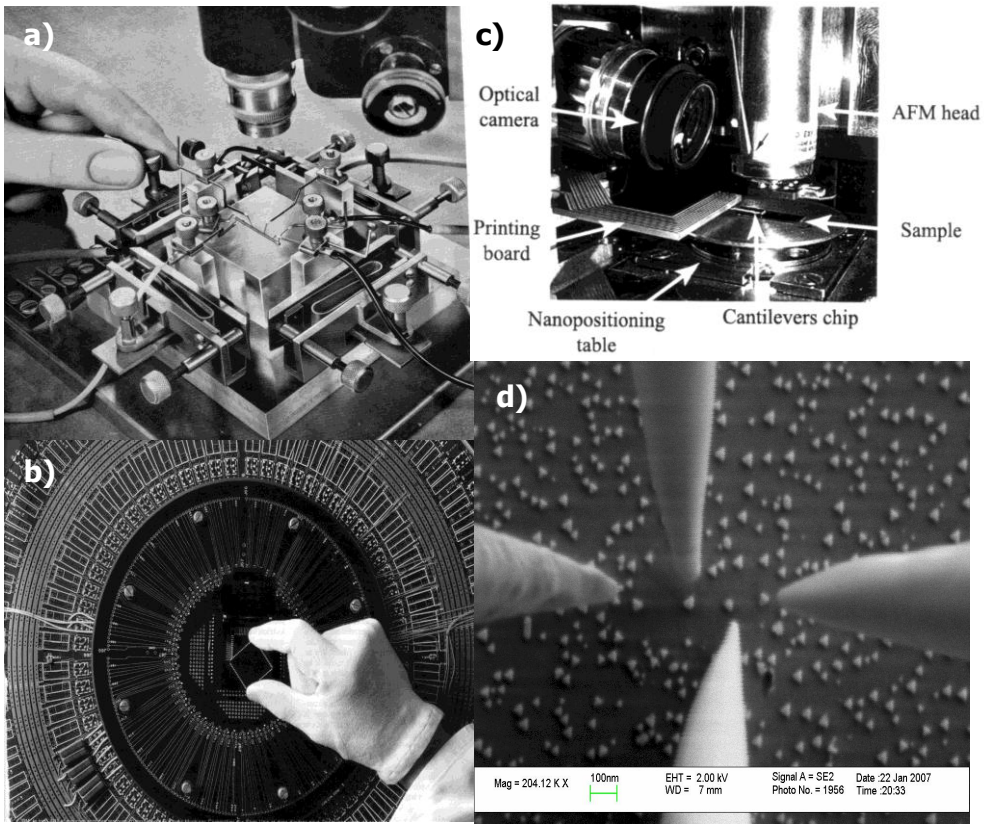

Figure 2: *History of planar multi-electrodes interconnects. (a) 1950's Bell Labs system equiped with an optical microscope and 4 electrodes for germanium interconnects [25]. (b) the 20th century multi-probes chip interconnects technology (courtesy of IBM). (c) A new generation of interconnection system involving an optical microscope plus an AFM microscope using 10 metallics cantilever positionned under the AFM head [28]. (d) A more recent version where the optical microscope had been substituted by an UHV scanning electron microscope and the metallic cantilevers subsituted by nanoscale apex STM tips [26] (courtesy of the A*STAR VIP Atom tech project, Singapore).*

For the optical microscope-NC-AFM case, 10 interconnects seems to be a good number [28]. There is here clearly a need to roadmap the computing power capacity increase embedded in a single molecule or with a surface atomic circuit and the number of possible interconnects converging towards this ultra small computing unit [19]. For example, it may happen that a well designed molecule offers too much computing power locally in regards with the maximum number of interconnects that one can physically be achieved in parallel on a surface. Then, a multiplexing like approach may be more appropriate, asking for more bandwidth and pushing the technology towards optical interconnects. Thus, efforts should be made in the future to extend experiments which aim to combine optics and local probe microscopy in an ultra clean environment with a prospect of a fully planar technology.

4. Atom and Molecule Surface science issues

The stabilization of an atomic scale computing machinery on a surface (be it self stabilized by its chemical structure or by the surface itself) requires a gigantic effort in exploring the properties of a large molecule of a surface at the atomic scale. During the 3 years of Pico-Inside, a lot of questions were discussed in this context starting from the choice of the surface. Of course, those discussions were targeting lab scale logic gate handling and interconnects. For a fully packaged molecule logic gate, a more realistic choice of surfaces is actually out of the range of what can be discussed (see the corresponding section below).

Depending of the atomic scale interconnection machine to be used, a first delicate problem is the choice of the supporting surface. A list of criteria were discussed in Pico-Inside: the electronic surface gap, the stability of the atomic surface structure, the stability of metallic nanoisland on the surface. For example, we know 2 extreme cases of passivated semi-conductor surface: SiH(100) and MoS_2. SiH(100) has a surface gap around 2.1 eV. The surface H atoms can be vertically STM manipulated one at a time to create p dangling bond like surface atomic wires or Hamiltonian computing structures [5,6]. But depending on the bulk doping, those H surface atoms are not so stable with temperature which precludes a thermal growth process to shape the contacting metallic nano-island. The lamellar MoS_2 compound has a self passivated semi conducting surface with a surface gap around 1 eV. The surface S atoms are extremely difficult to vertically STM manipulate [29]. But if manipulated, they also offer the possibility to create surface atomic wires with a band structure much more complicated that the SiH(100) [30]. The surface MoS_2 surface is extremely stable up to 1200 °C [31] and metallic nano-pads can easily be shaped and manipulated to construct any multi-electrode interconnections pattern with an atomic scale precision [26]. But the low surface gap of this material will certainly preclude its direct use as a supporting interconnection surface. A better exploration of the surface properties of diverse semi-conductor surfaces (See for example Figure 3) and their possible passivation is here urgently needed.

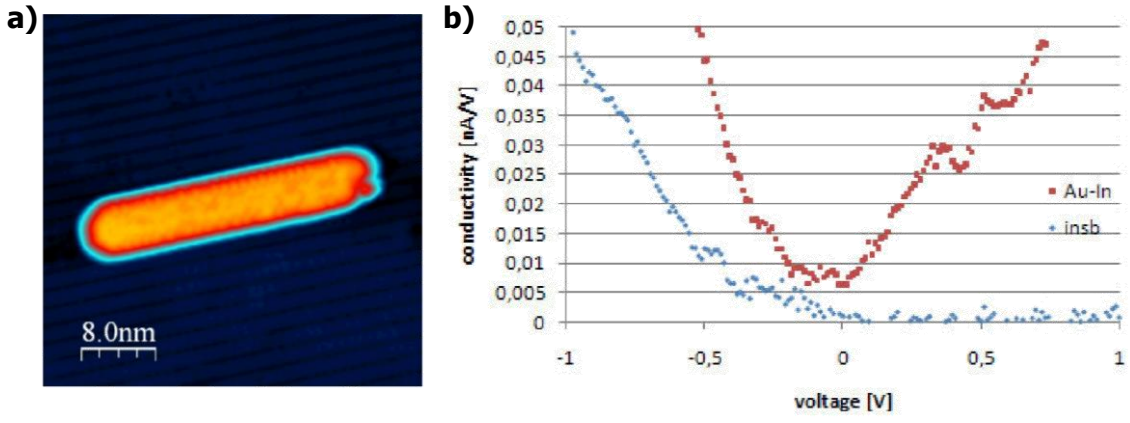

Figure 3: *Exploring the surface science of interconnects: fabrication of Au nanowires on the InSb(001) surface in the UHV to be interconnected on a Fig. 2D UHV interconnection machine. (a) High resolution STM image of Au alloy nanowire formed on InSb(001) surface by a good selection of the surface anneling temperature. Bias voltage: -0.5V, tunnelling current: 25pA. (b) STS conductance measured using an STM tip as a function of bias voltage on an Au alloy nanowire (red dots) and directly on the InSb substrate (blue dots) (Courtesy of the Jagiellonian University, Krakow).*

Large electronic gap surface are even less explored than their semi-conductor counter parts. The nice property of those surfaces is the fact that leakage surface current

between 2 metallic nano-pads adsorbed on the surface will be very low, well below the fA range, an advantage as compared with the above mentioned semi-conductor surface. The drawback is that there is no easy solution to fabricate or stabilize atomic wire on those surfaces. During the Working Group meeting, two solutions were discussed to bypass this problem: the use of molecular mold to stabilize metallic atomic wires or the use of long molecular wires between the metallic nano-pads and the central computing units. This second solution may be a good way to boost the research on long molecular wires characterized by an extremely small tunneling inverse decay rate [32].

Graphene, the new comer was not on the Pico-Inside agenda and was discussed in Toulouse as a mean to pass directly from the mesoscopic to the atomic scale with a "perfect" chemical like continuity between the 2 scales. This will be another choice of surface self supporting the interconnection and the computing unit. The open question is whether or not progresses in the fabrication techniques will allow an atom by atom fabrication technique respecting the absolute atomic scale precision required for such a circuit [33].

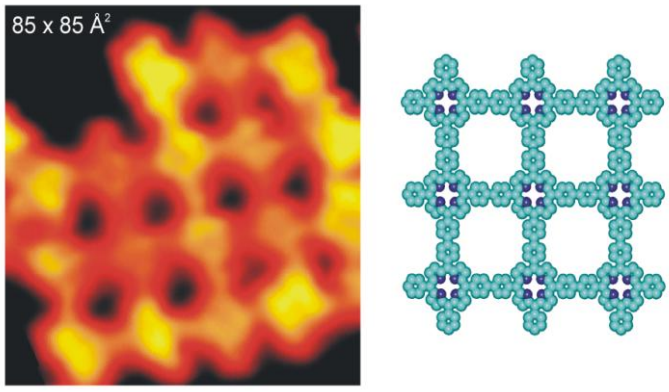

Figure 4: *Playing with single molecules on a surface. Instead of sublimating a large molecule on a surface, it may be better to bring first the monomers and to make them self reacting with each others by controlling the spontaneous 2D diffusion. STM image (left) of a molecular network on a Au(111) surface with the corresponding scheme (right). The network is grown from single porphyrin (TPP) molecules monomers ("on-surface-synthesis") by forming covalent bonds between the individual building blocks [35].*

It is also not clear how far can we go by playing with a single and large molecule adsorbed on a surface be it the one of a semi-conductor or of a bulk insulating materials. There is the difficult challenge of sublimating of a large molecular weight molecule on a surface in an ultra clean manner respecting the integrity of the molecule [34]. May be better to perform the chemistry in situ sublimating only the monomers and playing with them after to construct or assemble the final large molecule (See Figure 4 and [35]). It remains to be explored if such an approach can be performed for example at the surface of a semi-conductor.

Discussions in Toulouse about molecular surface science indicate how far we are from a very good understanding of molecular processes and behaviors of a large molecule on a surface at the atomic scale. There is here a wide range of understanding and know how which need to be acquired before creating a full atomic scale technology for molecular computing.

5. Packaging

In Pico-Inside, packaging was not on the official agenda. Off site discussions about packaging indicate that we are far from being ready to study those questions simply because even the lab scale interconnection machines are just about to be assembled. Packaging is always associated with the number of interconnects which have to be stabilized by the encapsulation technology selected for the circuit [19]. There is not yet

a clear path on how to create a packaging technology for surface mono-molecular electronics. A specific mono-molecular NanoICT seminar may be dedicated in the future to this very strategic problem. But it is so advance and so strategic [36] that it may turn out to be very difficult to trigger an open discussion about packaging.

6. Conclusion

The first mono-molecular nanoICT Working Group seminar was the occasion to cluster in a very Cartesian way all the 4 major issues under grounded in the monomolecular approach of molecular electronics which were worked out during the 42 month of the Pico-Inside project. In all areas of technology, the construction of a complex system by assembling elementary pieces or devices leads to a Moore's law like trend when analyzing the complexity growth of the system per year, a trend which appears threatened in the near future for microelectronics. The mono-molecular approach of molecular electronics with its compulsory atomic scale technology offers way to push past possible limitations in miniaturization, and to gain further increases in computing power by orders of magnitude by relying of a full development of an atom or molecule based technology for both electronics and machines. To reach this stage, each of the 4 issues illustreated in this concluding paper will require a specific discussion and more than that a specific research and technological development program.

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