Atomic Functionalities on Silicon Devices AFSID

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In AFSID, we wish to take advantage of a fundamental figure-of-merit of CMOS transistors, the doping modulation. We propose to investigate new functionalities arising from the control of a single charge and spin on individual dopants in silicon. The ultimate electrical switch is an atomic point contact. It has been realized and operated several times in laboratories at low temperature under the form of Quantum Point Contacts QPC), metallic break junctions and molecules placed in an air gap. However a silicon atomic switch has not been realized yet. The devices will be manufactured within a mature technology on state-of-the-art CMOS platforms. In contrast to bottom-up approaches, there is usually an unavoidable dispersion in the average number and location of dopants, using masking and implantation CMOS techniques. Nevertheless several approaches are now addressing this problem for top-down devices, which we will exploit in this proposal. Therefore, we will study single atomic devices, either real (i.e. dopant) or artificial (i.e. quantum dots), with a manageable dispersion by considering three generic cases: devices without dopant, devices with a targeted concentration of one dopant and devices with many dopants. Devices without dopant will be based on the ultimate silicon Single Electron Transistor (SET). A targeted size of 10 nm is realistic, allowing operation at low temperature (but much above 4.2K). These devices are fully controlled and scalable. Devices with one dopant or two dopants will be identified and selected from their electrical characteristics and then studied thoroughly. Relatively high operating temperatures up to room temperature are expected using donors with large ionization energy. These devices are the smallest possible switches using silicon technology. Because our ultimate SET present the decisive advantage of an immediate integration in the CMOS process, the AFSID project will prove the validity of hybrid SET-CMOS approach by building a SET-FET hybrid device on chip.

Beneficiary no.	**Beneficiaries organisation name**	**Short nº**	**Country**
1 (Coordinator)	Commissariat l'Energie Atomique	CEA	France
2	TU Delft	TUD	The Netherlands
3	Uni-Tübingen	UTU	Germany
4	CNR-INFM	MDM	Italy
5	Hitachi Cambridge Labs	HIT	United-Kingdom
6	University of Melbourne	MEL	Australia