CANDICE: CArbon Nanotubes Devices for Integrated Circuit Engineering

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The overall objective of this 3-year project was to develop a CMOS-compatible industrial process for the fabrication of field effect transistors and circuits based on carbon nanotubes (CNT-FETs).

The project brings together 4 European partners, namely CNRS/Ecole polytechnique (prime), Cambridge University (Electrical Engineering Department), Thales Research & Technology and Fraunhofer Institute ISiT .

In order to solve the CNT manipulation and placement problems, two approaches based on template growth in engineered porous structures are investigated.
In the first one, rather "bottom up", CNTs are grown (using Chemical Vapour Deposition-CVD) inside porous alumina templates obtained by anodic oxidation of Al films. Pores can be synthesised either perpendicular to the surface of the substrate (as usually performed) or parallel to it, using a novel technique of lateral anodic oxidation.
In the second approach, clearly "top-down", CNTs are grown in vertical pore structures obtained by nanolithography and reactive ion etching.
In both cases, the catalyst particles (necessary for the nucleation and growth of CNTs at low to medium temperature) are electrodeposited at the bottom of the pores prior to CVD growth of the CNTs.

Moreover, by using monocrystalline substrates underneath the pores, we deposit the catalyst particles in an epitaxial-type mode, which leads to a controlled structure on large scale. Although we do not claim chirality control, our first experiments of CNT growth on controlled (epitaxial) catalysts will be presented and analysed.
Figure 1 below shows the two transistor structures studied in the present project. Note that the vertical structure can also be fabricated by using alumina templates.

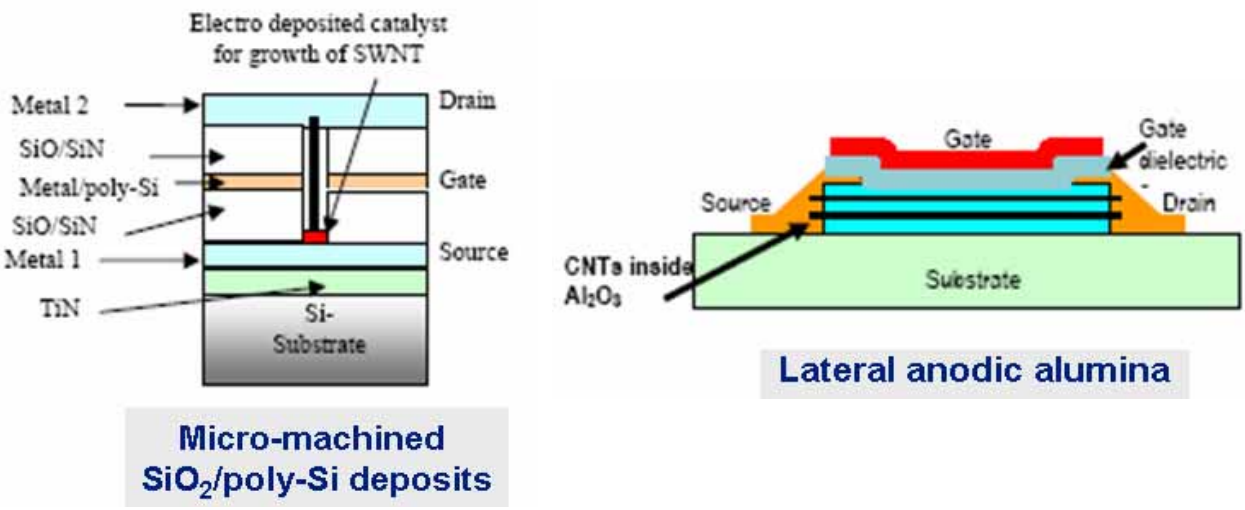

***Figure 1**: Vertical and lateral transistor structures studied in CANDICE.*

Figure 2 shows examples of vertical templates in which Ni clusters have been electrodeposited (before CVD growth of CNTs).

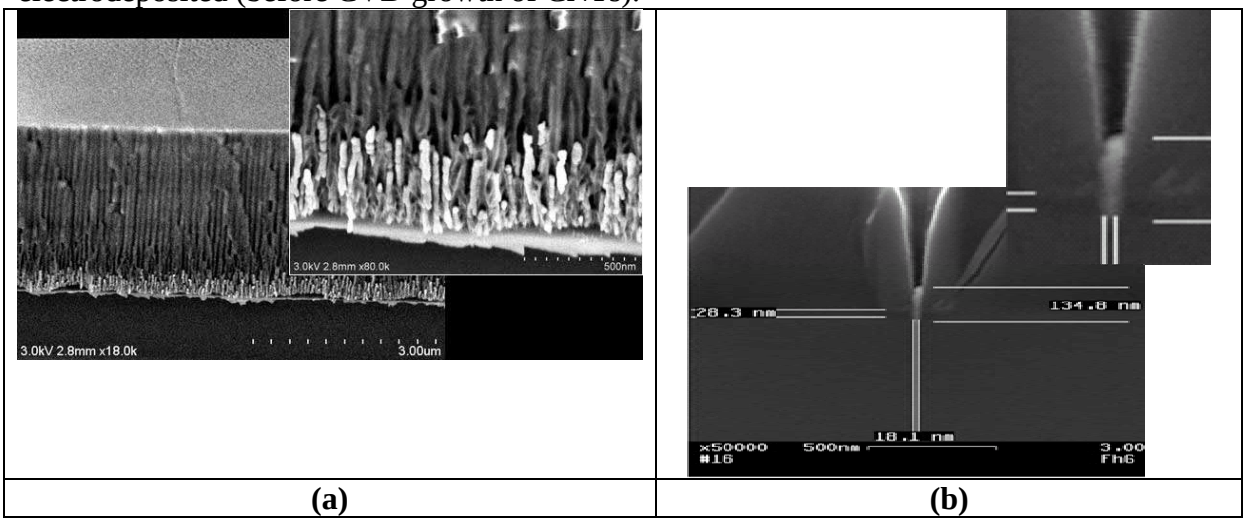

***Figure 2**: (a) Vertical alumina membrane (obtained by anodic oxidation) after Ni electrodeposition. (b) Vertical membrane etched in amorphous-Si/SiO_2. In both cases the pore diameter is below 20 nm.*

Figure 3 shows different views of CNTs grown inside vertical membranes using electrodeposited Ni as catalyst material. As the pore (and catalyst) size was ~ 15 nm, essentially multiwall carbon nanotubes have grown. Note the CNT emerging from a pore on figure 3-c.

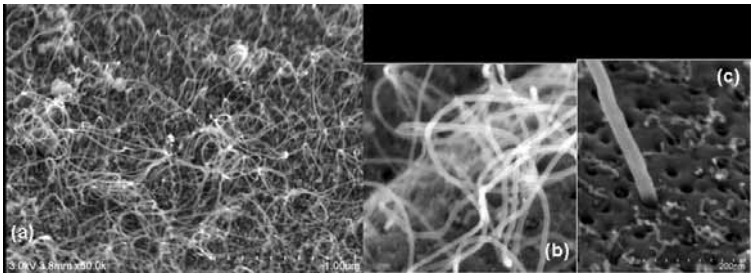

***Figure 3**: (a) CNTs that have grown out of a vertical membrane. (b) Enlarged view. (c) Detail of a CNT emerging from a pore.*

Finally, figure 4 presents various lateral templates obtained by controlling the Al thickness and anodic oxidation conditions.

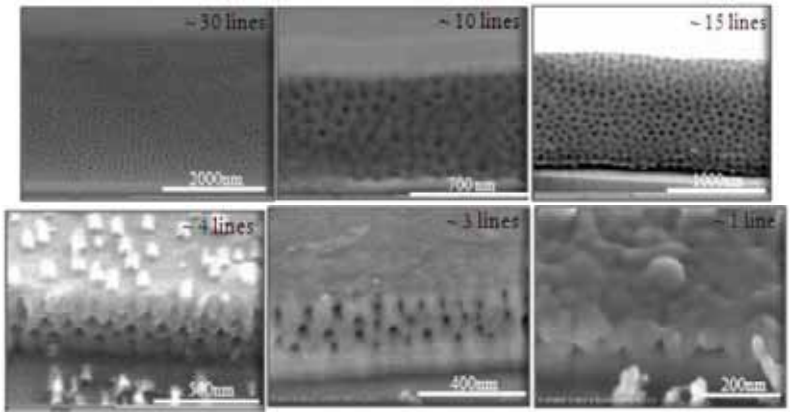

***Figure 4**: Control of lateral pores obtained by anodic oxidation of encapsulated Al films. From left to right and top to bottom, 30 pore rows down to 1.*