Advances on the path to a Ge dot field effect transistor

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The project **"Disposable Dot Field Effect Transistor for High Speed Si Integrated Circuits"** (d-DOT-FET) is an initiative to accomplish a prototype transistor compatible with CMOS technology, but with a strained Si channel in an all Si approach. Thus no relaxed SiGe buffer layer or buried SiO2 layer will be used. The channel will be fabricated from a freestanding Si bridge stabilized by the gate stack. Ge dots will be used as stressors to obtain locally in the gate area a strained Si channel. The bridge is formed by disposing the Ge dot underneath the channel after the gate processing. The device is expected to outperform current Si CMOS technology in terms of speed, i.e. gain, as well as power managing (heating).

The ordering of Ge islands on a templated Si substrate has been successfully mastered by several techniques. The combination of advanced optical lithography and CVD deposition of Ge dots allows processing close to industrial standards. The positioning of the transistor gates aligned to the buried Ge islands is a crucial task for the successful implementation of device concept. To this end a special marker technology for e-beam lithography has been established permitting alignment accuracy better than 10 nm.

The fabrication technology of the d-DOT FET requires low temperature processing throughout the whole fabrication process to avoid Si-Ge intermixing, i.e. to maintain the strain in the Si channel. Special emphasis was put on the development of a suitable gate stack, the result of various approaches will be reviewed.

Strain-dependent mobility models have been implemented in device simulations. A physically based low-field bulk mobility model and an empirical surface mobility model are combined to estimate the mobility in the strained channel. The calculations predict an enhancement of the drain current of up to 43% if the Ge dot is removed and the strain is maintained in the Si bridge.