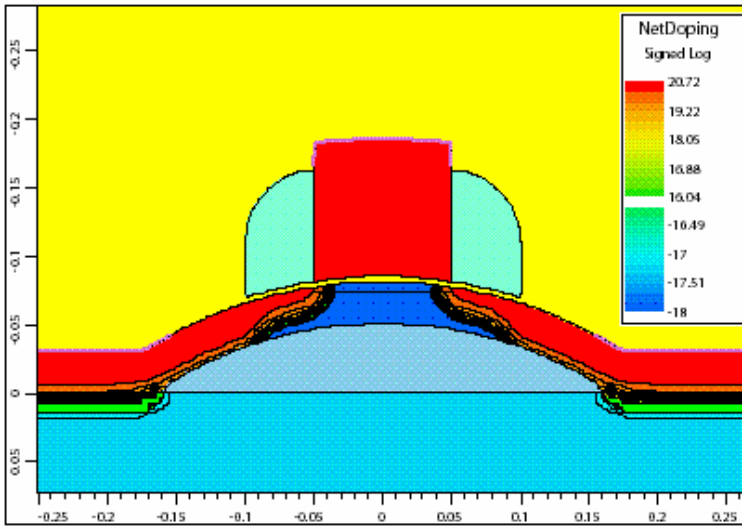
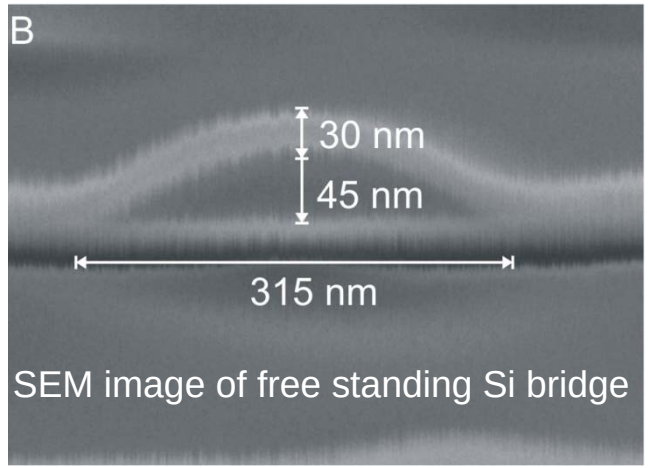
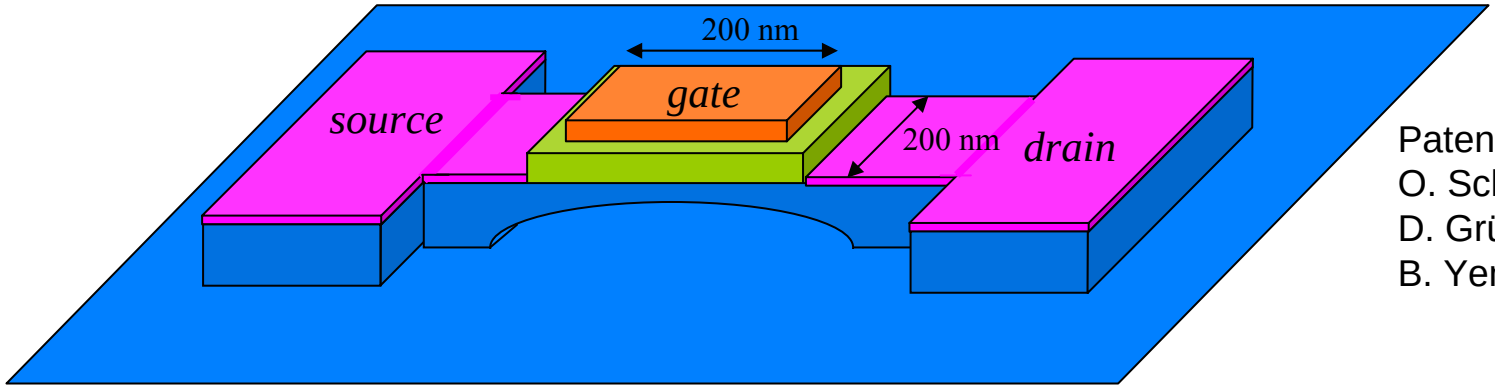
Disposable Dot Field Effect Transistor for High Speed Si Integrated Circuits

Towards D-Dot Field Effect Transistor

Concept



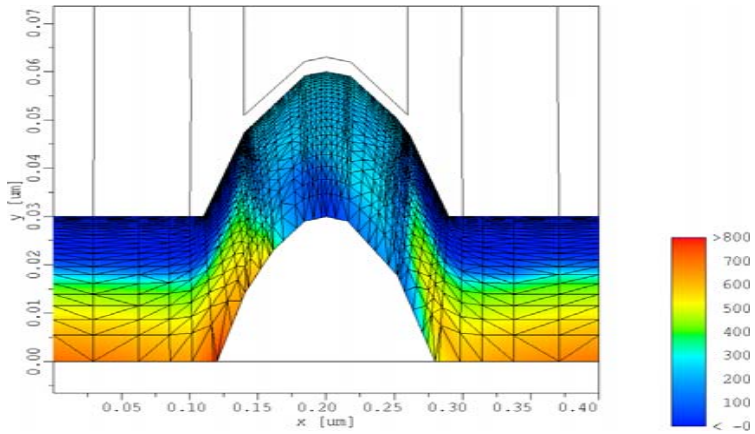


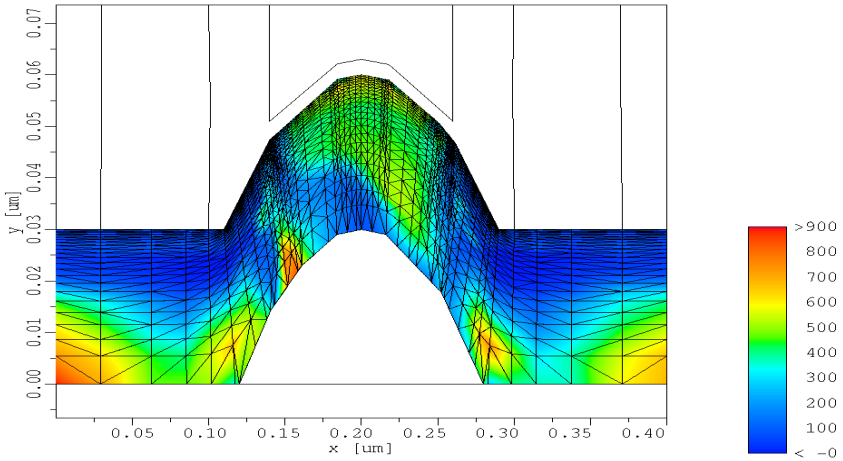


Patent:
O. Schmidt (IWF)
D. Grützmacher (FZJ)
B. Yen et.al. (Freescale)

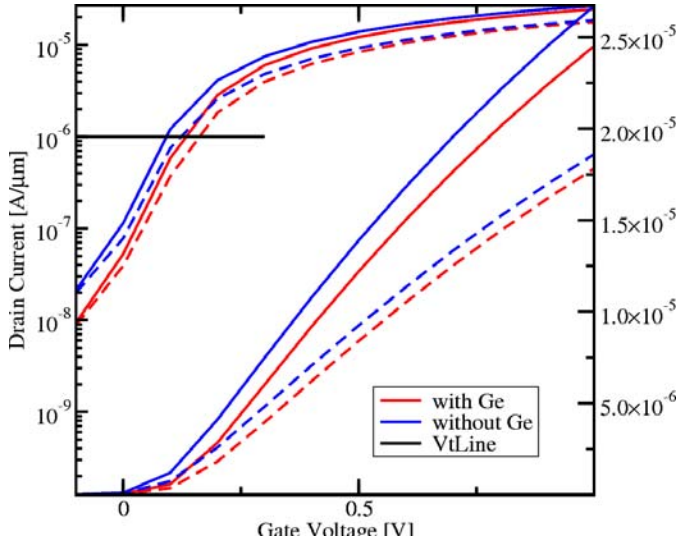
Coherent, defect free structure with tensile strain > 0.25% in Si

Drive current improvement





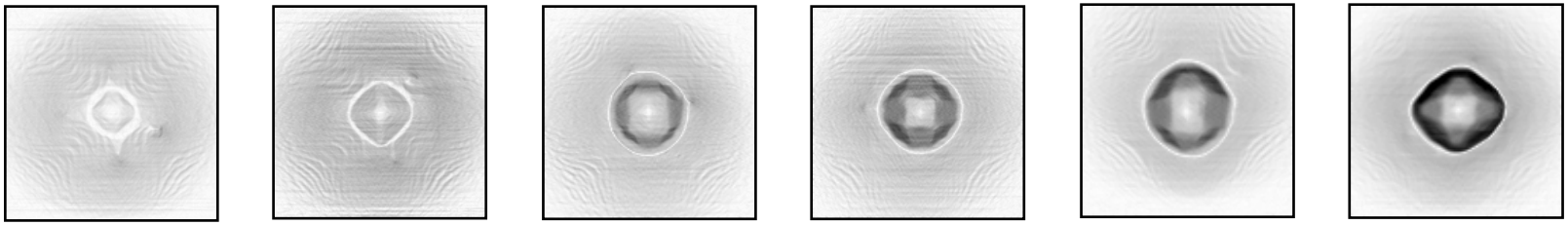
70% increase in channel mobility
43% increase in drain current

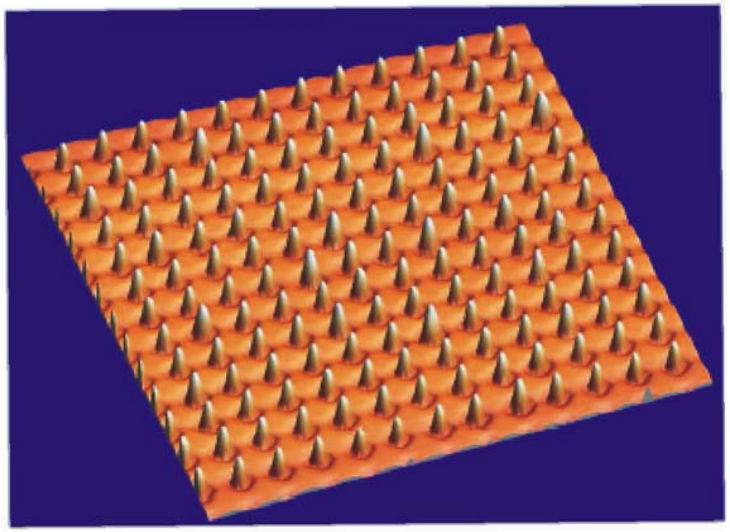


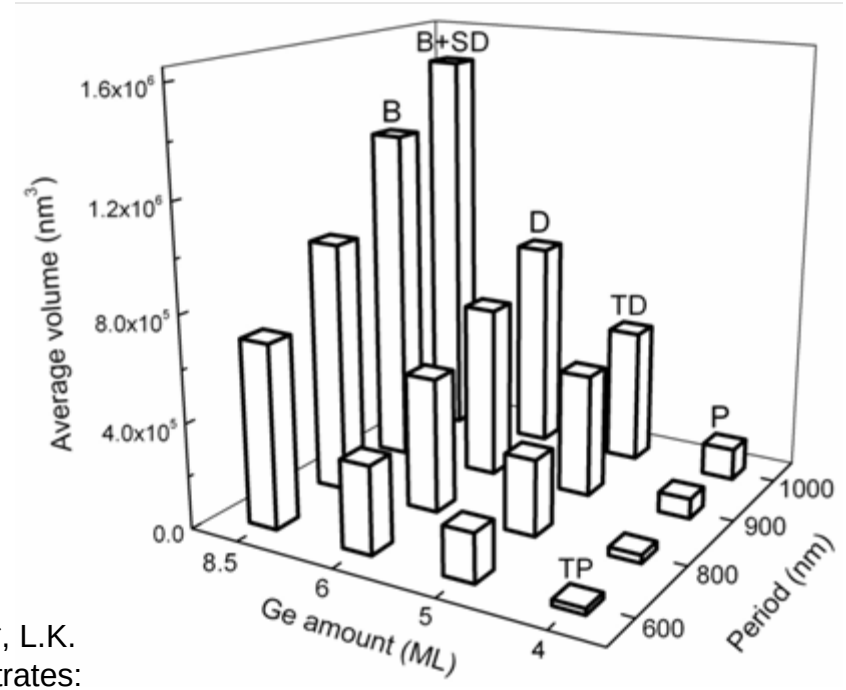
S. Dhar, E. Ungersböck, H. Kosina, T. Grasser, S. Selberherr, Electron Mobility Model for <110> Stressed Silicon Including Strain-Dependent Mass; **IEEE Transactions on Nanotechnology, 6 (2007), 1; 97 - 100.**

E. Ungersböck, S. Dhar, G. Karlowatz, V. Sverdlov, H. Kosina, S. Selberherr, The Effect of General Strain on the Band Structure and Electron Mobility of Silicon; **IEEE Transactions on Electron Devices, 54 (2007), 9; 2183 - 2190.**

Ordering of Ge dots

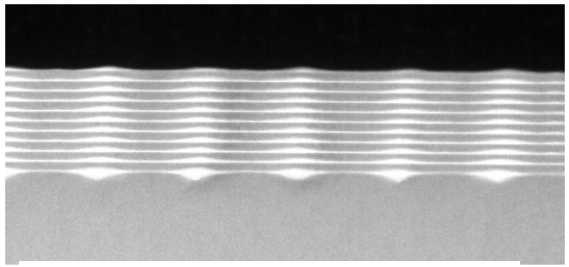


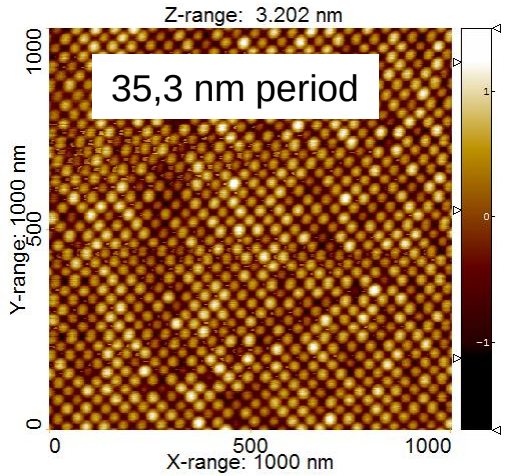


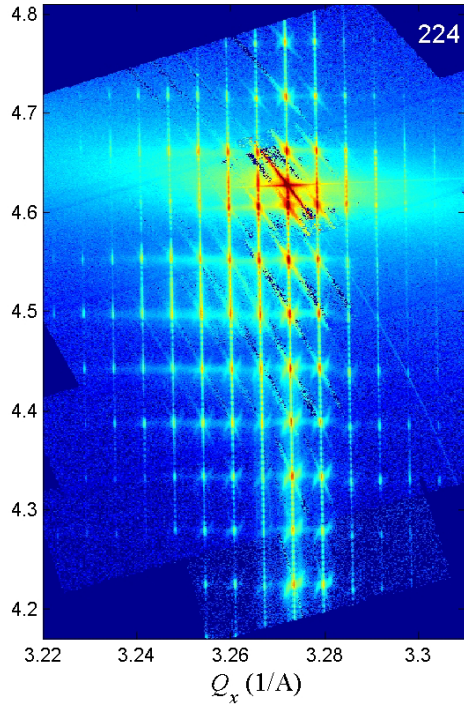


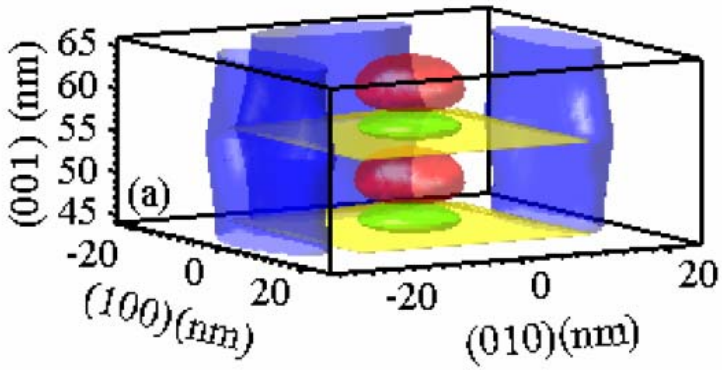
J. J. Zhang, M. Stoffel, A. Rastelli, O. G. Schmidt, V. Jovanovi*, L.K. Nanver, and G. Bauer, SiGe growth on patterned Si(001) substrates: Surface evolution and evidence of modified island coarsening, **Appl. Phys. Lett. 91, 173115 (2007)**

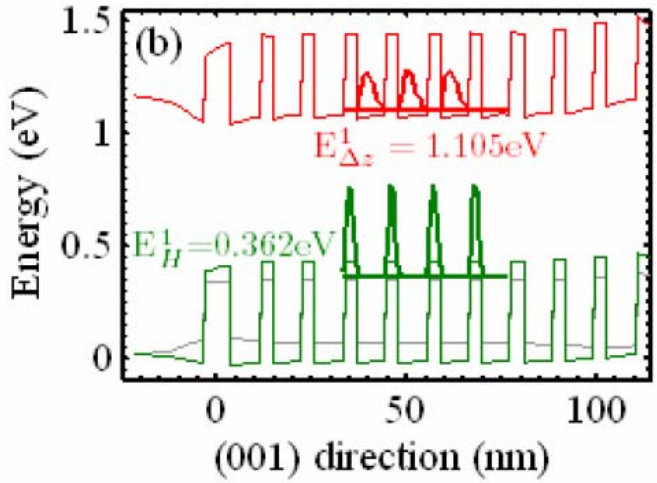
3-d Ge dot crystal







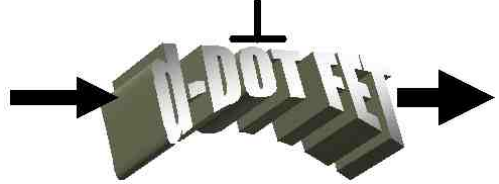


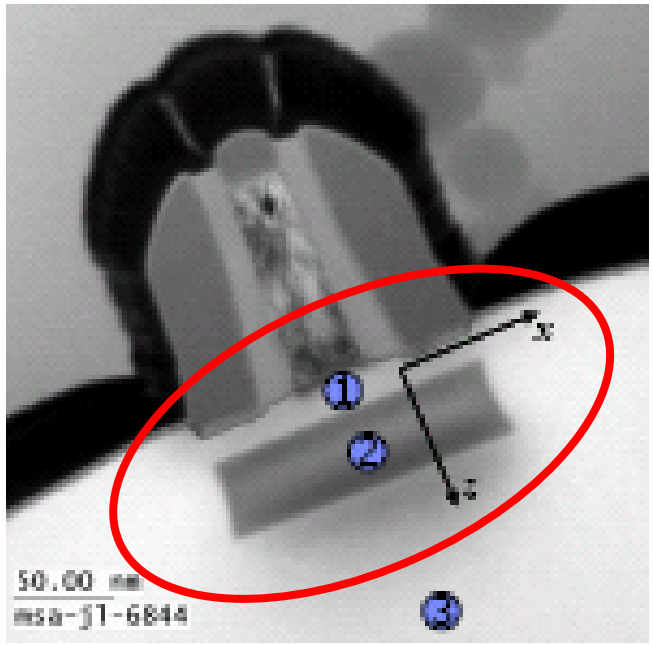


Grützmacher D, Fromherz T, Dais C, Stangl J, Mueller E, Ekinci Y, Solak H, Sigg H, Lechner R, Wintersberger E, Birner S, Holy V, Bauer G, Three-dimensional Si/Ge quantum dot crystals. **NANOLETTERS 7 , 3150 (2007)**

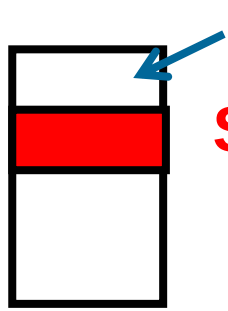
Highlight in Photonics Spectra December 2007

The d-DotFET competitors





R.A. Donaton et al.,
IEDM Tech. Dig. , pp. 465 (2006)



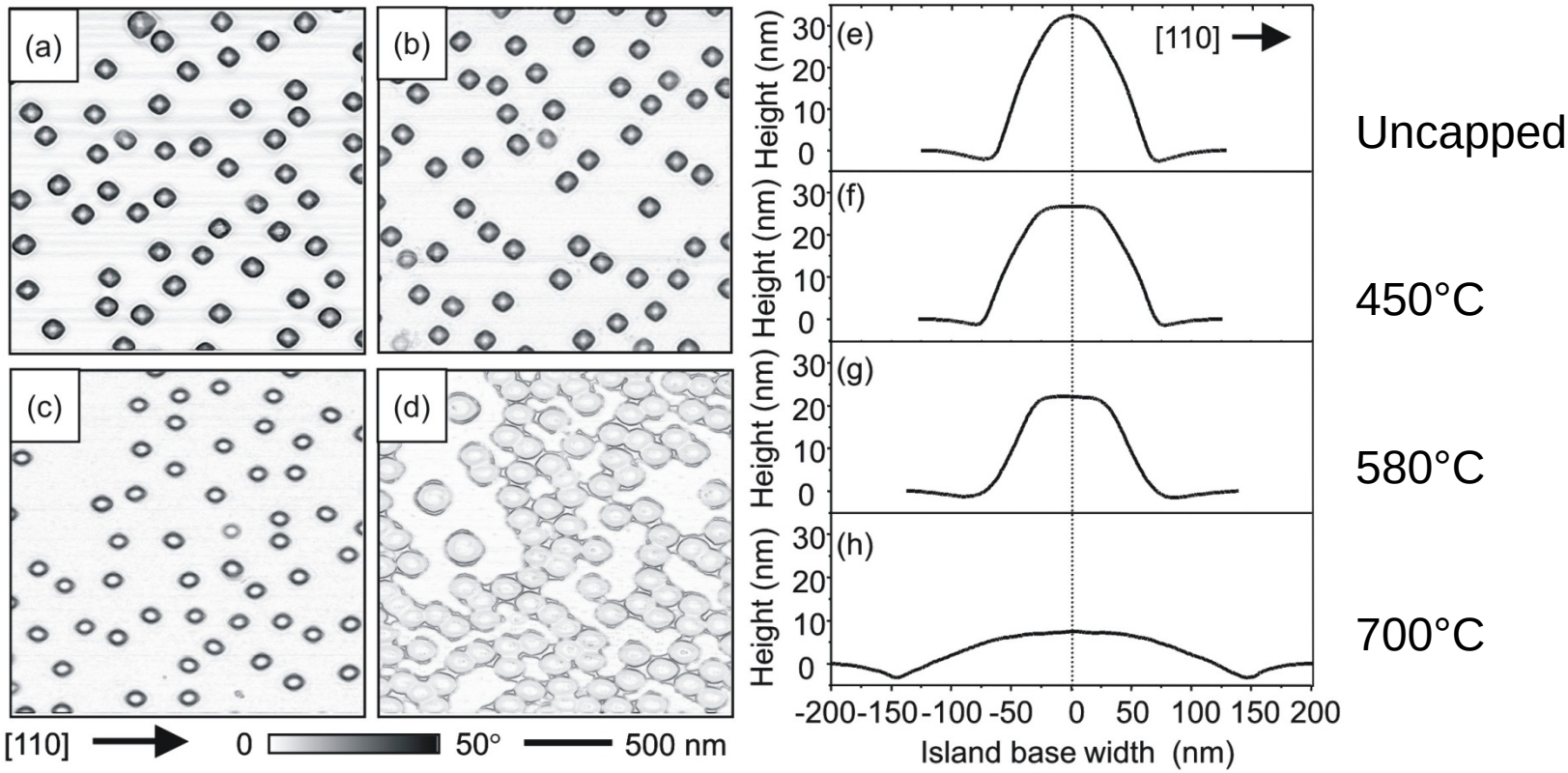
Si channel

$Si_{1-x}Ge_x$

x = 25%

Device	Strain in channel
d-DotFET, barn Ge = 60%	+0.005
IBM, Ge = 30%	+0.0028
IBM, Ge = 25%	+0.0024
d-DotFET, mound Ge = 30%	+0.0020

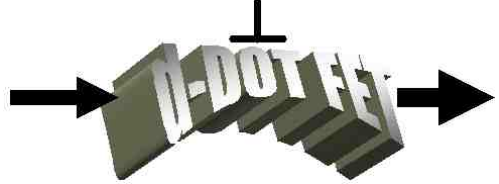
Impact of capping on Ge barns

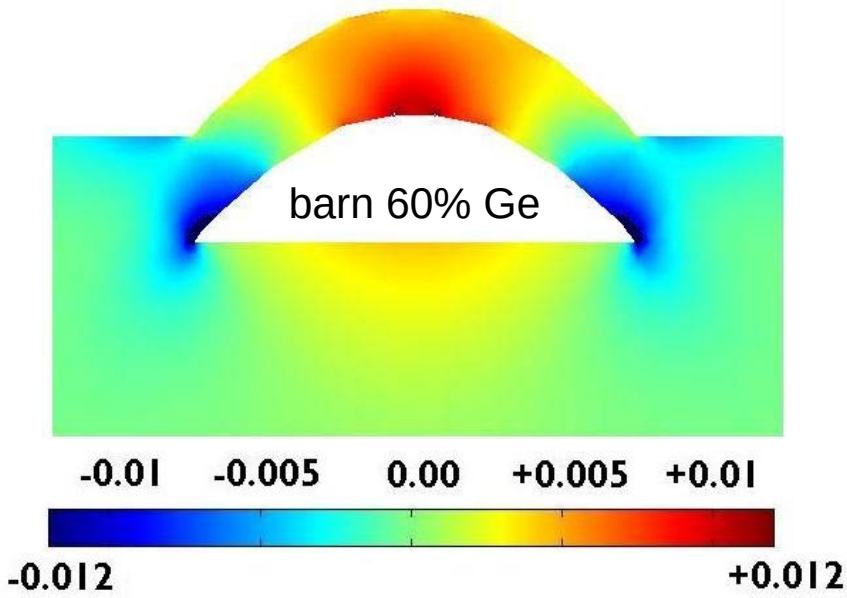


Low temperature capping preserves shape and strain of island

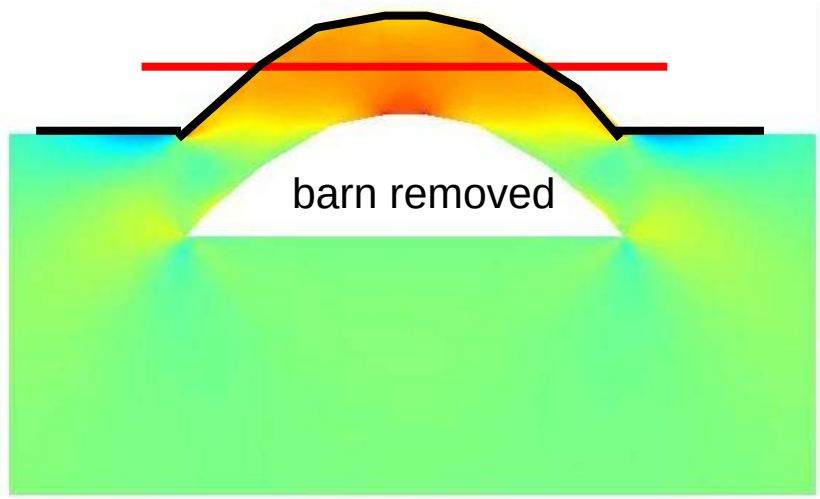
M. Stoffel, A. Rastelli and O. G. Schmidt, Surface evolution and three dimensional shape changes of SiGe/Si(001) islands during capping at various temperatures
Surf. Sci. 601, 3052 (2007)

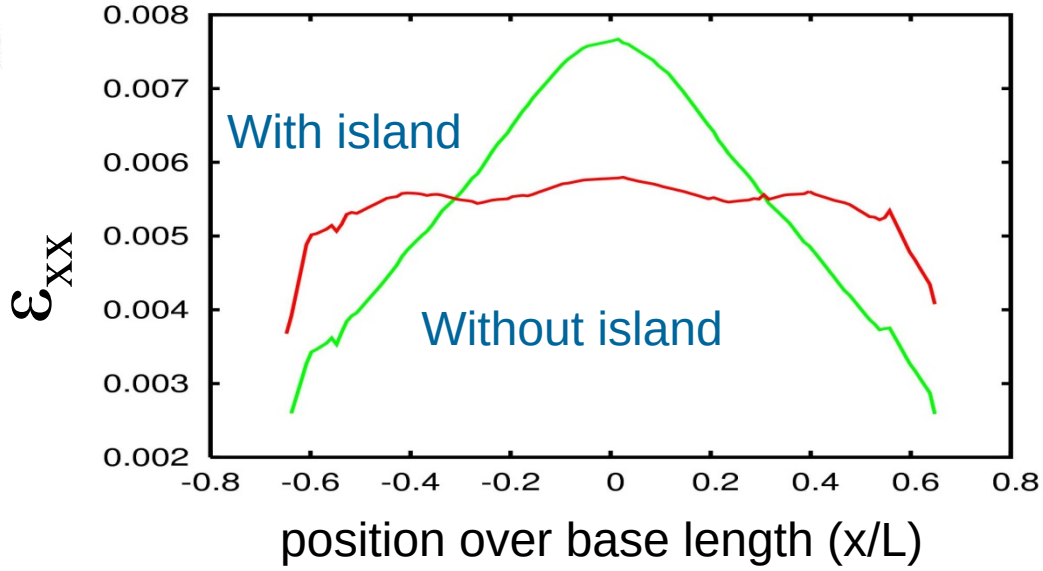
Effect of island removal



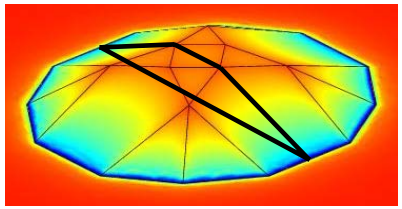


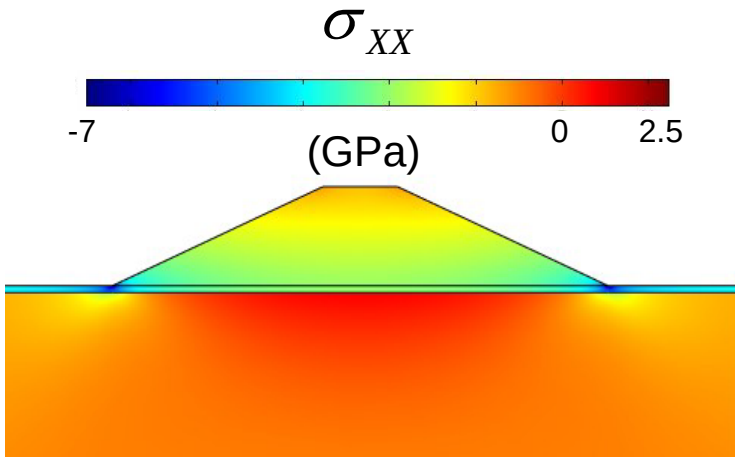
ε_{xx}





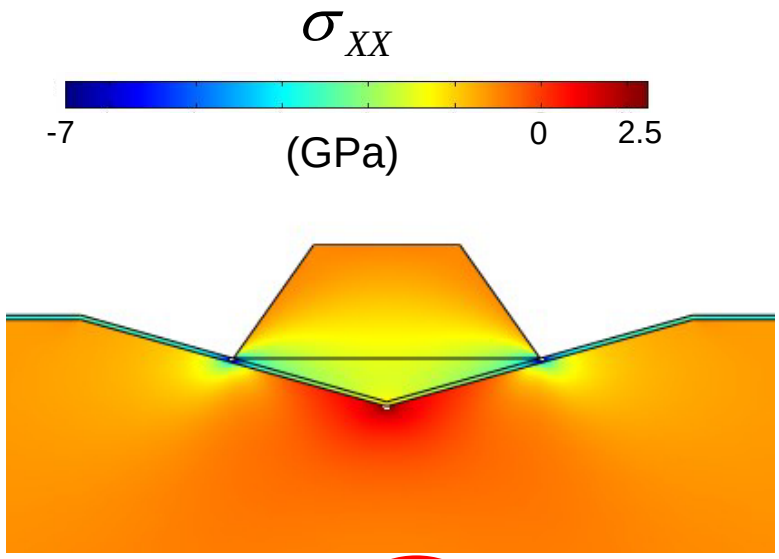
Critical island size for plastic relaxation





$V_c = 1.1 \cdot 10^4\ nm^3$

T = 620°C **x_{Ge}= 0.55**



$V_c = 1.3 \cdot 10^5\ nm^3$

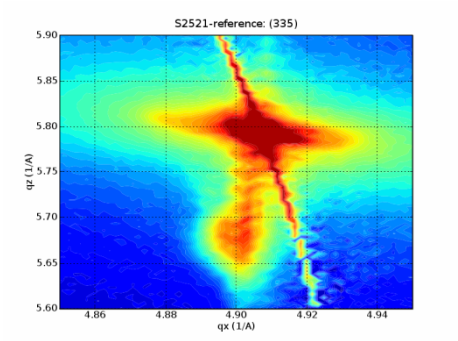
Delayed plastic relaxation on patterned Si substrates: coherent SiGe pyramids with dominant {111} facets
Zhenyang Zhong; Schwinger, W.; Schaffler, F., et al.
Physical Review Letters, **vol.98, no.17** Pages: **176102/1-4** (**2007)**
Critical shape and size for dislocation nucleation in Si1-xGex islands on Si(001)
A. Marzegalli, V.A. Zinovyev, F. Montalenti, A. Rastelli, et al.
Physical Review Letters, in press.

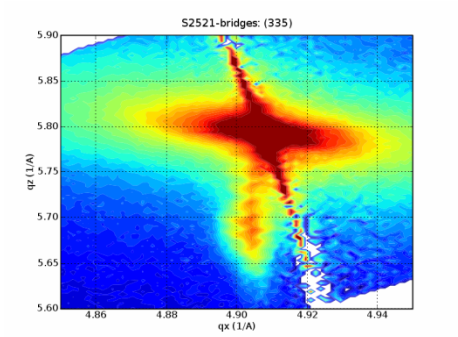
Stabilizing strain in Si bridges with SiN_x

- Ge content of islands 30%
- in-plane strain before dot removal 0.2%
- in-plane strain after dot removal (exp.) : 0.1%

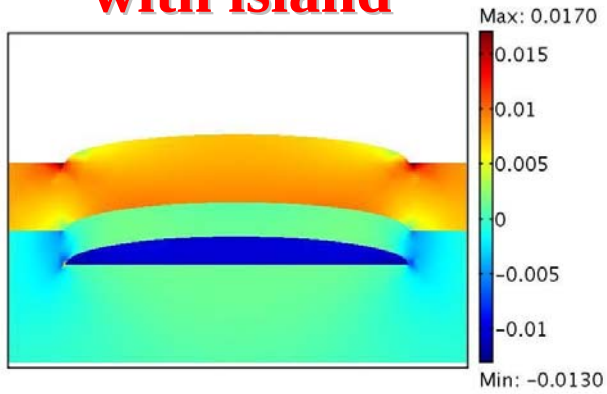
  in good agreement with simulations

  (for 60 nm Si_3N_4, 1.2GPa) 0.13%

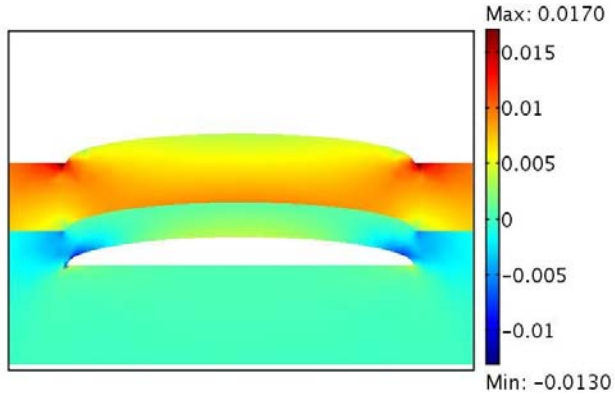




with island

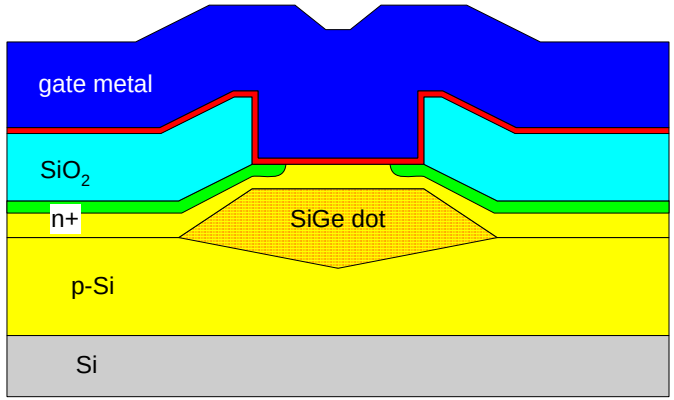


without island



Towards the DOT FET

The new process flow retains the SiGe dot:



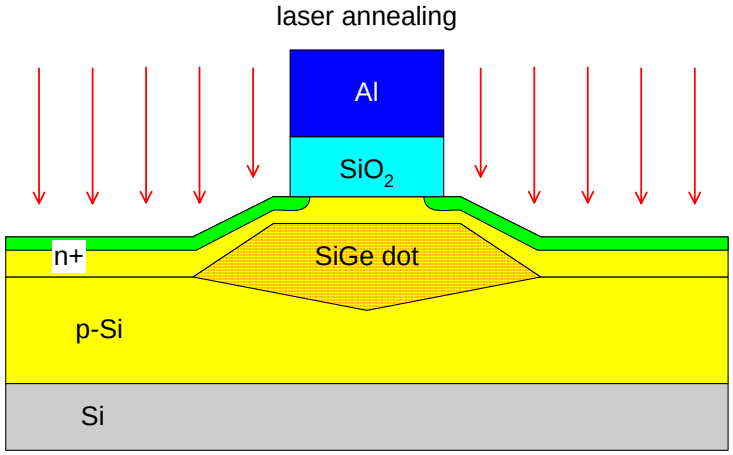
therefore low-temperature processing of gate and source/drain is needed to prevent Ge diffusion

2 new advanced process modules are used that are
on the ITRS roadmap for 32 – 20 nm gate length CMOS generations

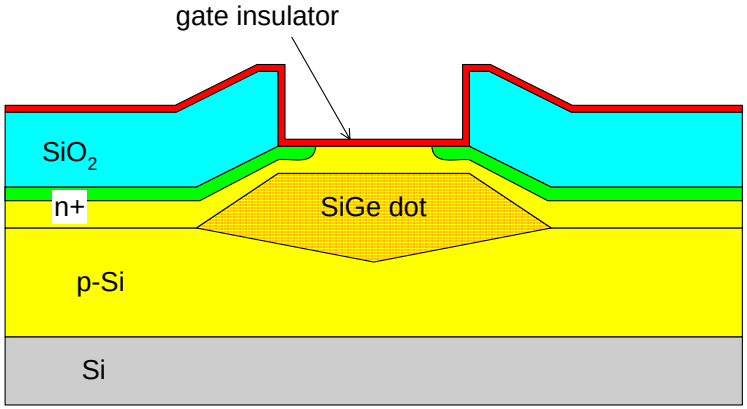
1) ultra-shallow implanted S/D junctions activated by laser annealing

2) gate stack with metal-gate and high-k dielectric

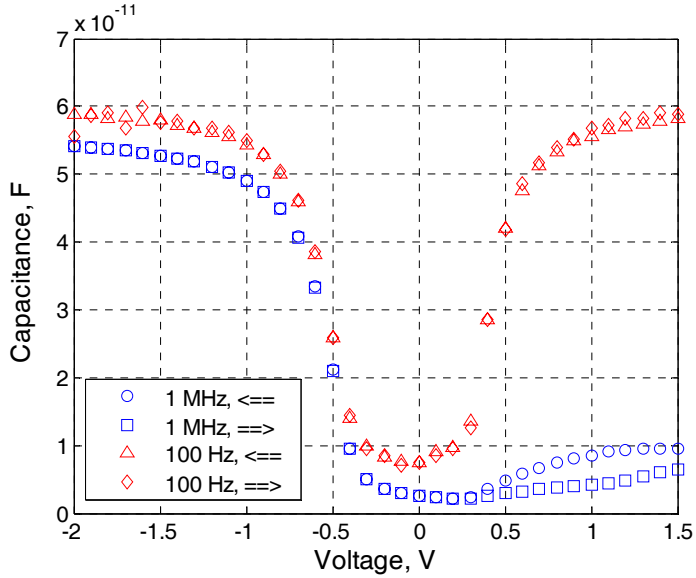
Low temperature process modules



Implantation of S/D – arsenic, 1015 cm-2, 5 keV
Laser annealing of S/D → 20 nm deep junctions.



Gate insulator deposition (EOT=5 nm)



- Capacitance-voltage measurements of gate stack with aluminium oxide deposited by ALD at 300ºC and aluminium (1% Si) gate. Interface to silicon is very thin silicon dioxide grown at 700ºC.

Conclusions

Building blocks developed for DOT FET

- **Coherent, defect free structure with tensile strain > 0.25% in Si**

- **potential for 0.5 % in Si**

- **geometry induced shear strain component improves mobility due to mass reduction**

- **new material: 3-d quantum dot crystal**
  electrons - photons - phonons