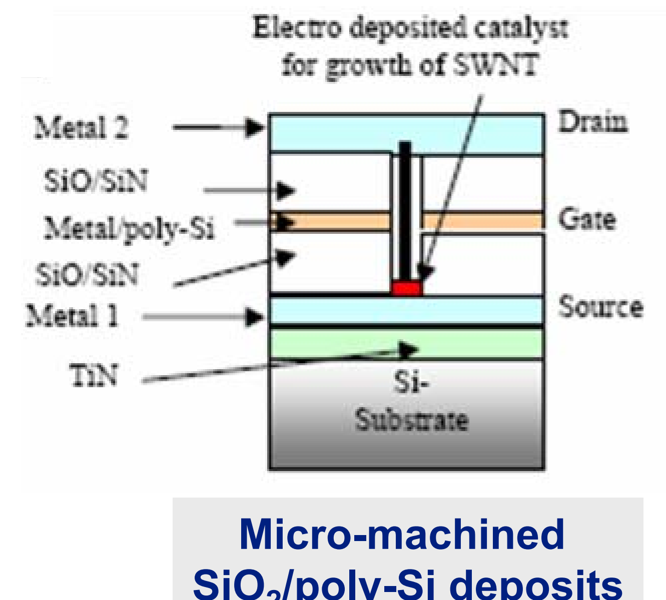
CArbon Nanotube Devices
for
Integrated Circuit Engineering

Project outline



Micro-machined SiO_2/poly-Si deposits

Aims:

1- Organisation of CNTs in templates

- Vertical templates: top down process
- Lateral templates: rather bottom up

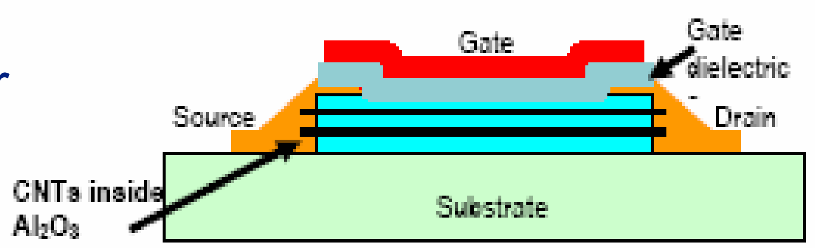
2- Chirality control?

1- CNRS/Ecole Polytechnique: Coordinator

2- Cambridge University

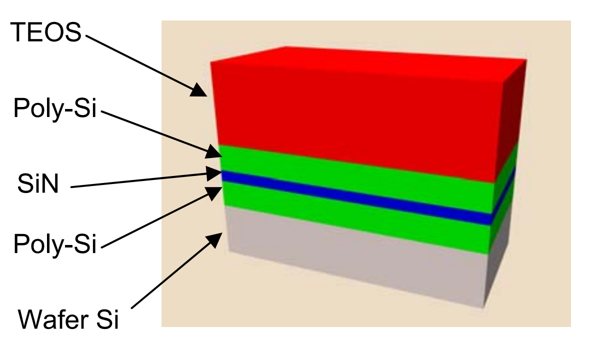
3- Thales Research & Technology

4- Frauhofer ISiT

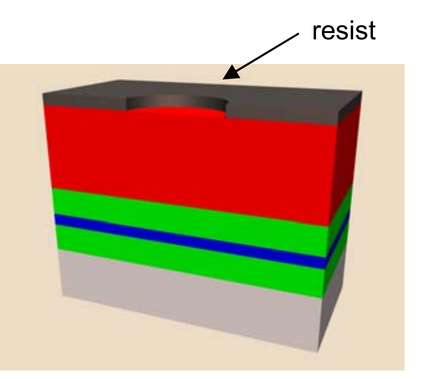


Lateral anodic alumina

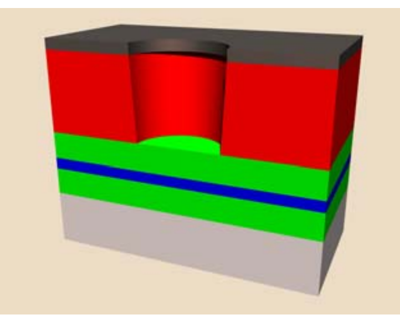
Process outline- Vertical templates



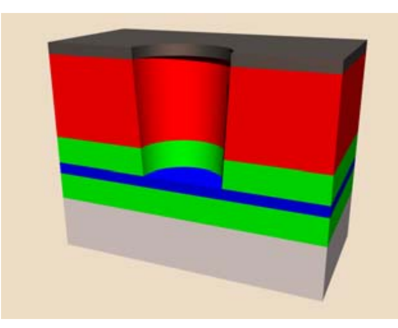
deposition of layers



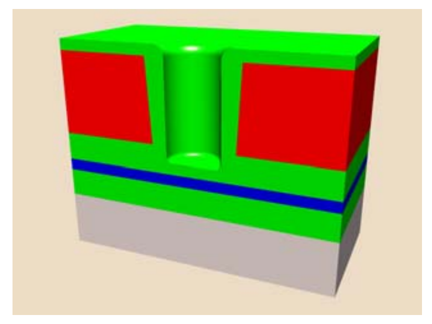
Structure resist



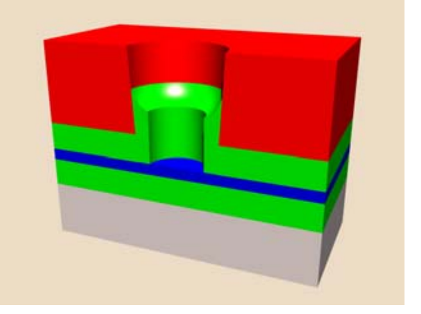
open LPCVD TEOS-layer



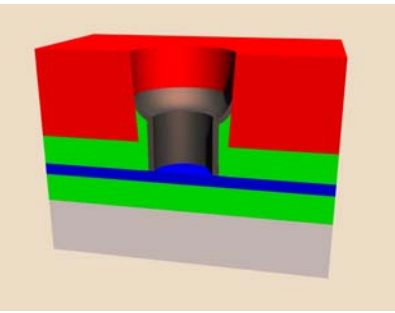
open gate-layer



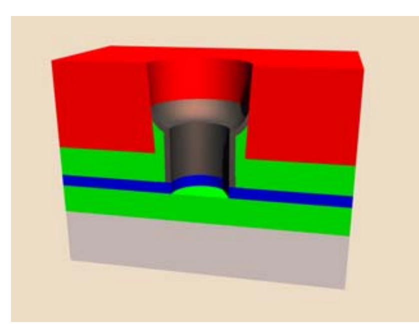
deposition of poly-si



etche poly-si spacer



Oxidation of poly-si spacer



open LPCVD- SiN

Vertical templates

Oxidized Gate Poly-si

TEOS

SiN

Poly-Si: Gate

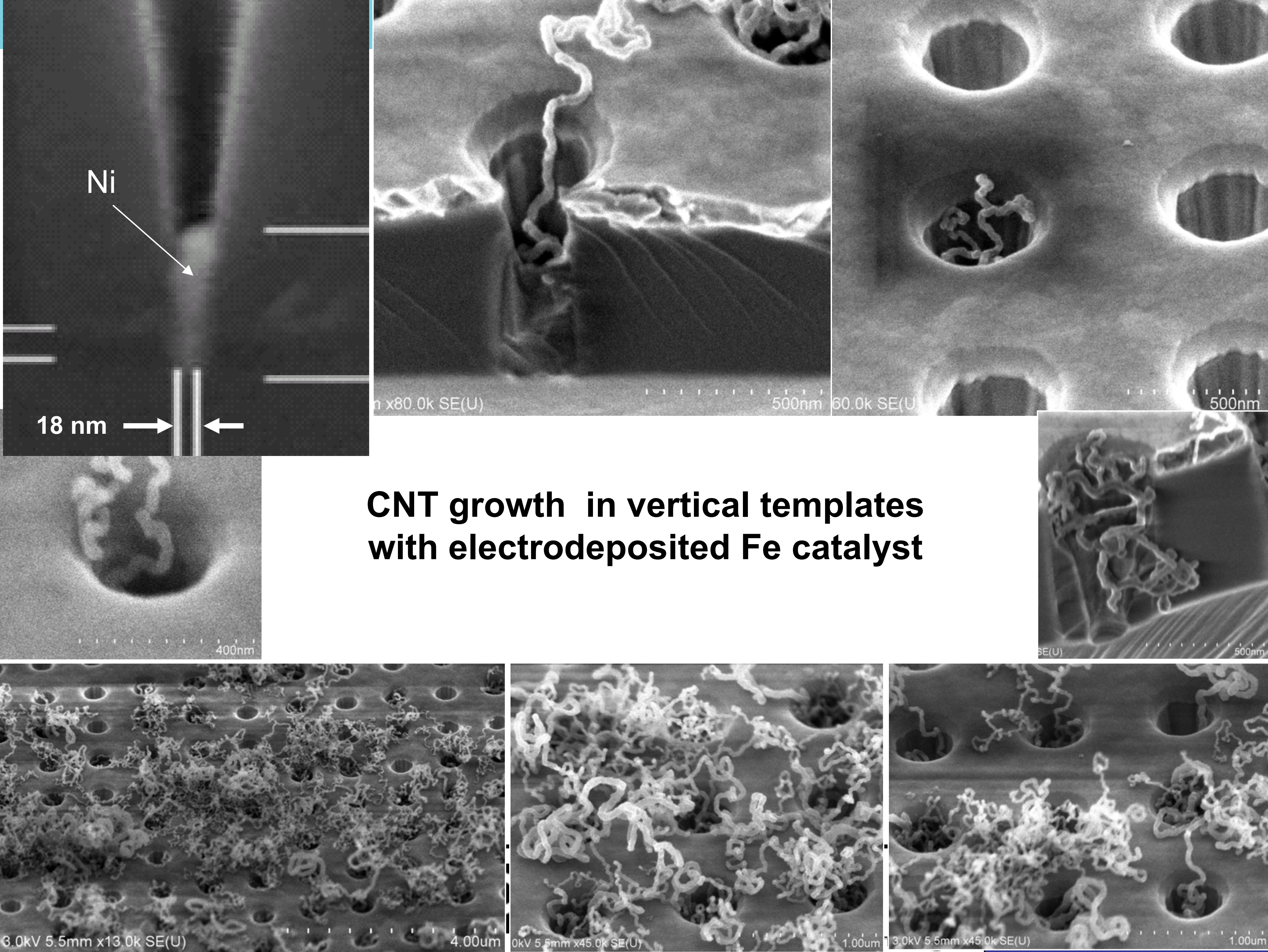
Poly-Si: Source

Wafer Si

Vertical templates

amorphous Si

Poly-Si


Ni
18 nm
x80.0k SE(U)
500nm
60.0k SE(U)
500nm
400nm
SE(U)
500nm
CNT growth in vertical templates
with electrodeposited Fe catalyst
3.0kV 5.5mm x13.0k SE(U)
4.00um
0kV 5.5mm x45.0k SE(U)
1.00um
3.0kV 5.5mm x45.0k SE(U)
1.00um

Process outline- Lateral templates

SiO_2
Si (100)
Al stripes
a)

SiO_2
SiO_2
SiO_2
Si (100)
Si (100)
Al stripes
b)

e^-
+
V
−
e^-
E
cations
anions
c)

Al
SiO_2
SiO_2
Si (100)
porous
Al_2O_3
d)

Results – different pore diameters

Sulphuric /10V/Ø~11nm
900 nm

(a)

Oxalic /20V/Ø~16nm
500 nm

(b)

Oxalic /25V/Ø~22nm
1000 nm

(c)

Oxalic /40V/Ø~36nm
700 nm

(d)

Oxalic /50V/Ø~62nm
2000 nm

(e)

Phosphoric /100V/Ø~87nm
900 nm

(f)

*Ø - errors will be in the range of <5nm and the decimal values are rounded off.

Results – different arrays

2000nm/20V/~ 30 lines
2000nm

(j)

1000nm/25V/~ 15 lines
1000nm

(k)

1000nm/40V/~ 10 lines
700 nm

(l)

250nm/40V/~ 4 lines
500nm

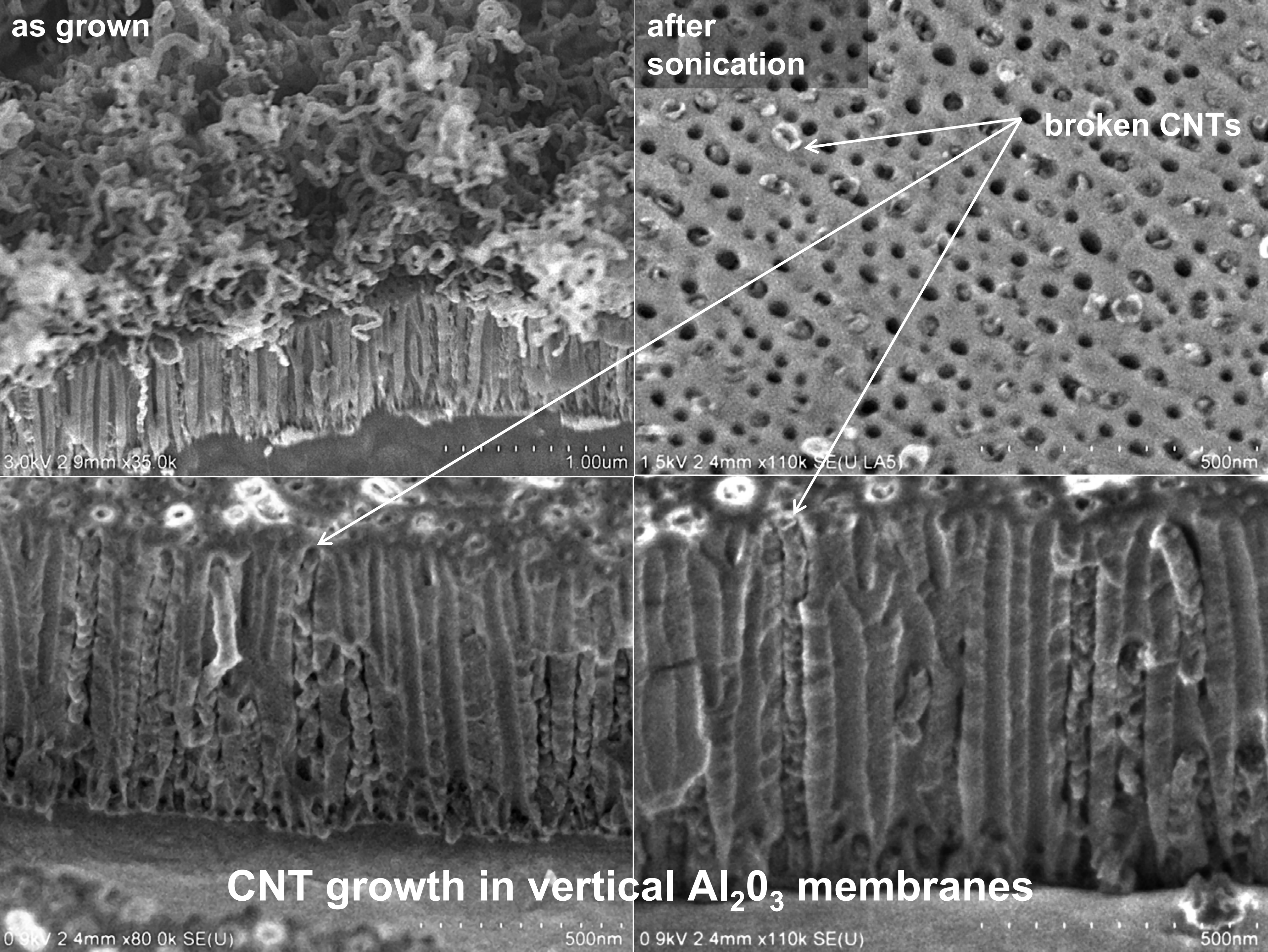
(g)

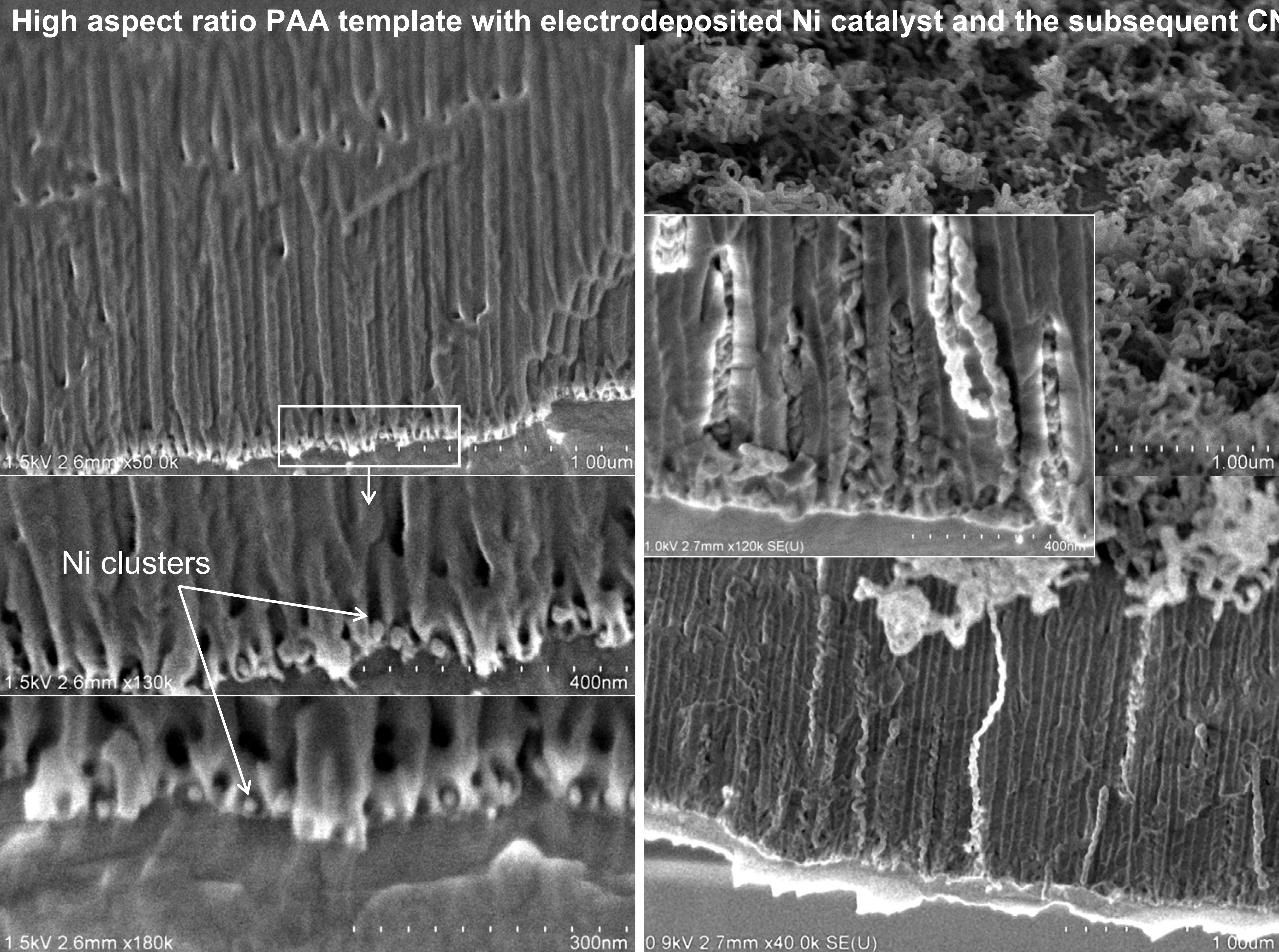
200nm/40V/~ 3 lines
400nm

(h)

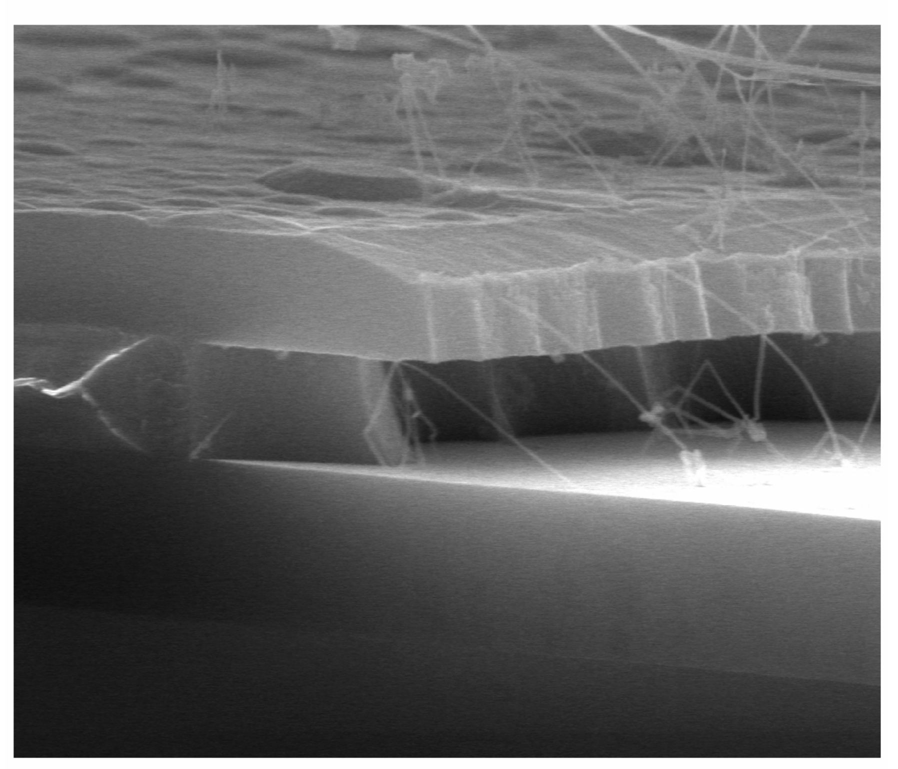
50nm/20V/~ 1 line
200nm

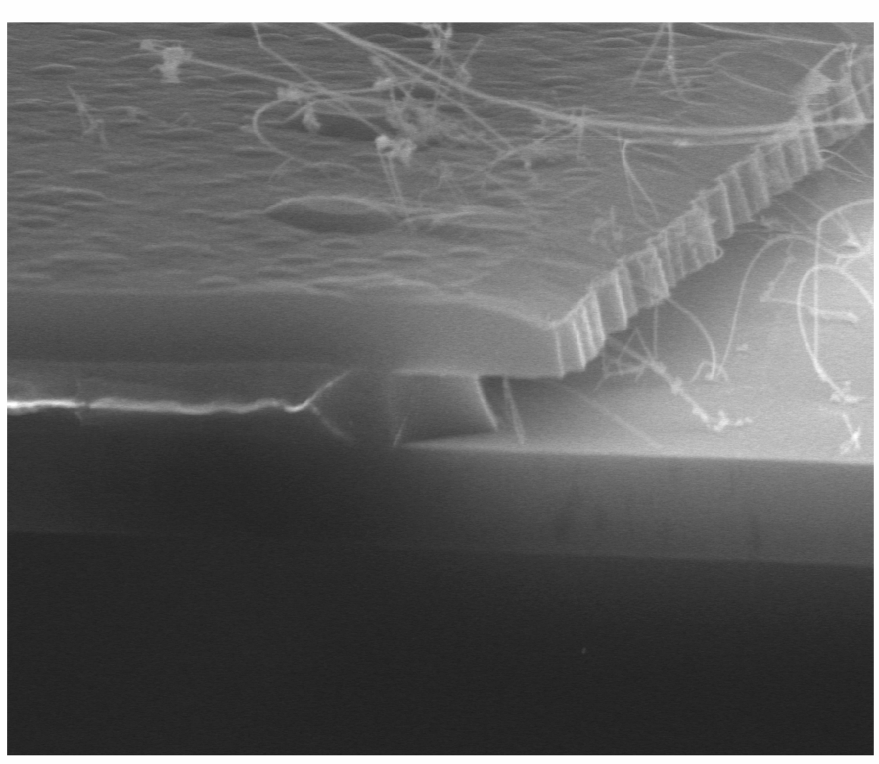
(i)


as grown
after
sonication
broken CNTs
3.0kV 2.9mm x35.0k
1.00um
1.5kV 2.4mm x110k SE(U,LA5)
500nm
CNT growth in vertical Al203 membranes
0.9kV 2.4mm x80.0k SE(U)
500nm
0.9kV 2.4mm x110k SE(U)
500nm


High aspect ratio PAA template with electrodeposited Ni catalyst and the subsequent CN
1.5kV 2.6mm x50.0k
1.00um
Ni clusters
1.5kV 2.6mm x130k
400nm
1.5kV 2.6mm x180k
300nm
1.0kV 2.7mm x120k SE(U)
400nm
1.00um
0.9kV 2.7mm x40.0k SE(U)
1.00um

Growth in lateral membranes: first trials (1)

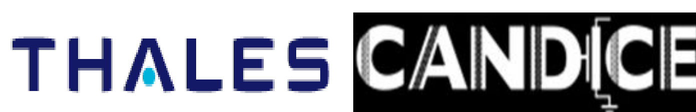




Growth in lateral membranes: first trials (2)

800 nm

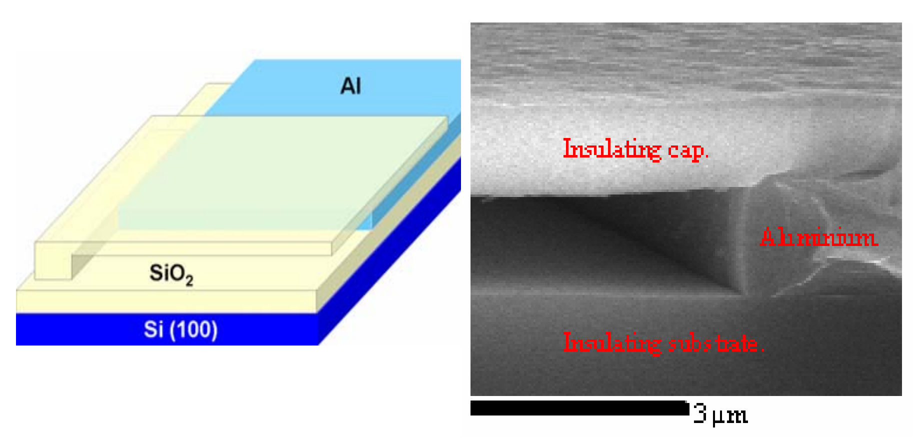
600 nm



Conclusions

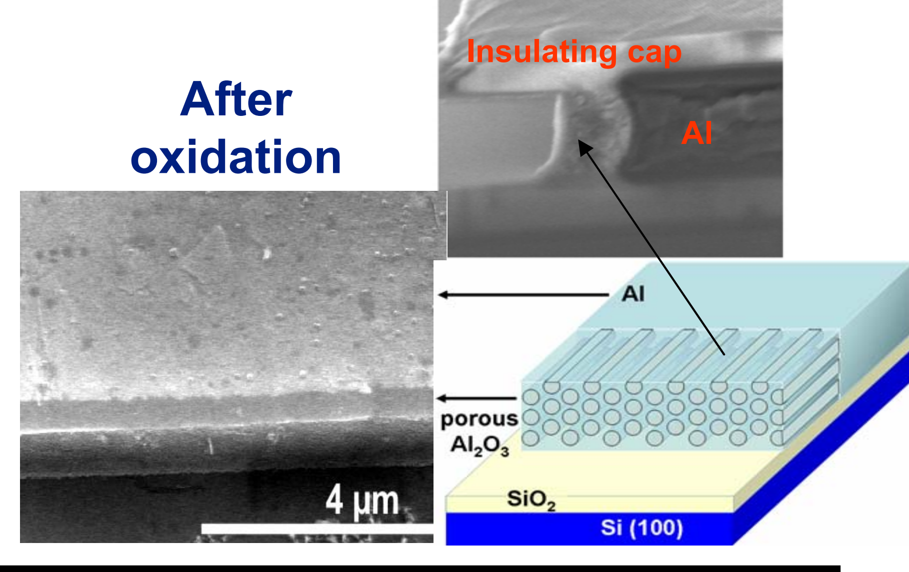
- Templates fabricated according to expectations
- CVD growth inside templates
  - OK for vertical FET structure
  - Needs to be calibrated for lateral growth
- Vertical devices will be realised in the next few months

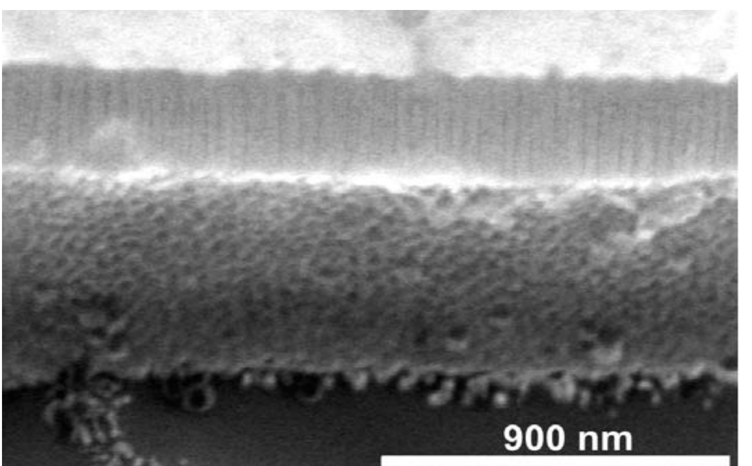
SEM observation of lateral anodic alumina templates

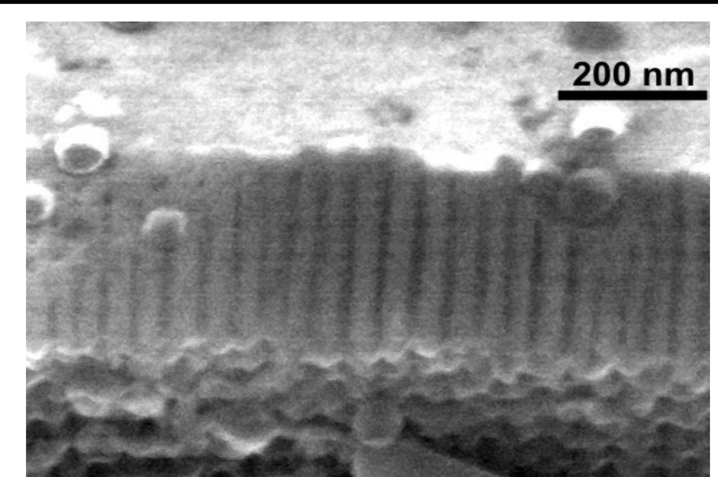


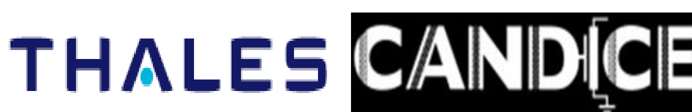
Before oxidation

After oxidation









TEM observation of lateral anodic alumina templates

50 nm

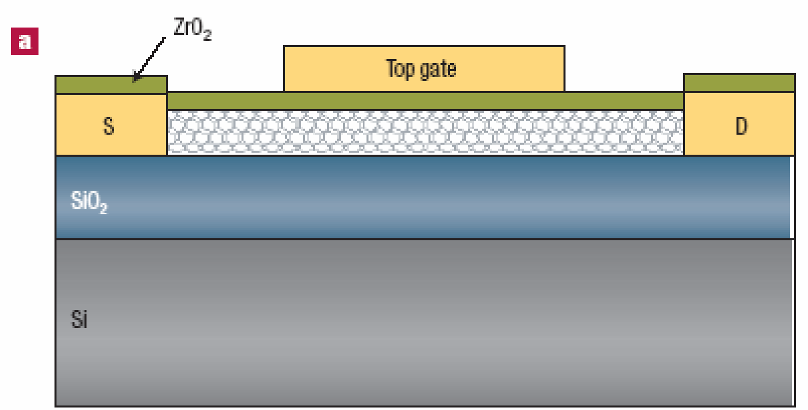
Pores filled with Te

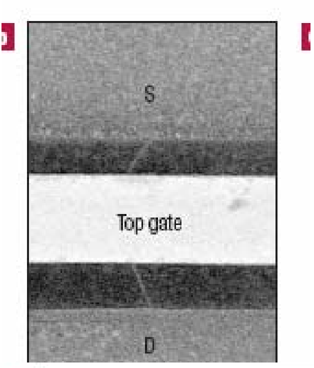
10 nm

5 nm, MEHR

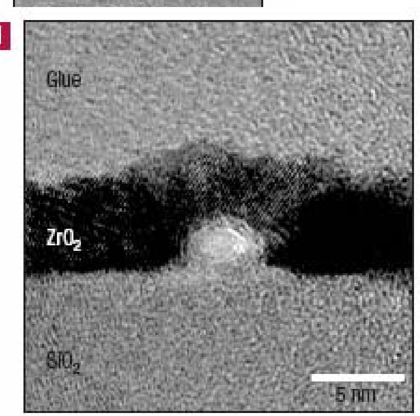
Pore size < 5 nm

CNT-Field Effect Transistor (FET)





HfO_2, ZrO_2
~ 3nm.
Top gate
and top contacts.



μ ~ 3000 cm^2/Vs.
Transconductance:
~ 6000 S/m.
S ~ 70 mV/decade

Dai's group, *Nature Mat*., 2002
Avouris' group, *Proc. IEEE*, 2003

Characteristics of CNT-FETs

Gate leakage

Dai,
Nature Mat.

$\mu \sim 3000\ cm^2/Vs$.
Transconductance:
~ 6000 S/m.
S ~ 70 mV/decade

Comparison between CNT-FETs and ultimate MOSFETs

Comparison between CNT FET and ultra-scaled planar Si FET

Transistor parameter	p-Type CNFET [7]	p-Type silicon MOSFET [8]
Physical gate length (nm)	260	15
Gate oxide thickness (nm)	15	1.4
Threshold voltage V_t (V)	−0.5	∼−0.1
On-state current I_{ON} (μA/μm)	2100	265
Off-state leakage I_{OFF} (nA/μm)	150	<500
Subthreshold slope (mV/dec)	130	∼100
Transconductance (μS/μm)	2321	975

Yu & Meyyappan, *Solid St. Electr.* 2006

The most common situation for CNT-FETs: Schottky contacts at Source and Drain

a) off-state

i) ii) iii)

E_c

E_v

source

drain

qV_{ds}

b) on-state

E_c

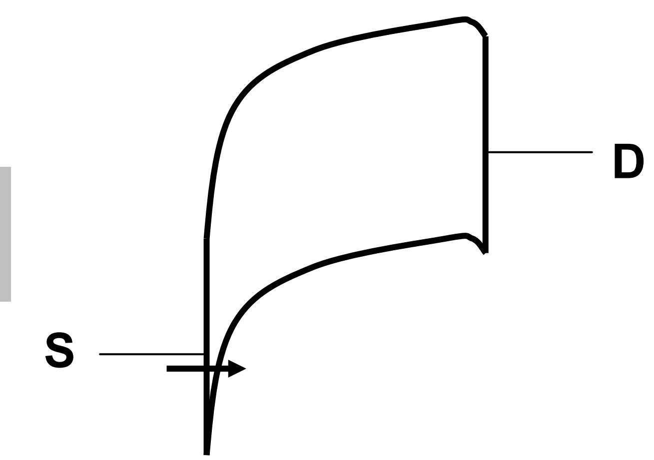
E_v

source

drain

h

Summary for CNT-FETs



General situation:
Current limited by the contact Schottky barriers

If L < λ (~ 20 nm): ballistic regime.
Channel resistance: R_Q = h/4e2 = 6.5 kΩ
(I_{on} ~ 25 µA/nanotube)

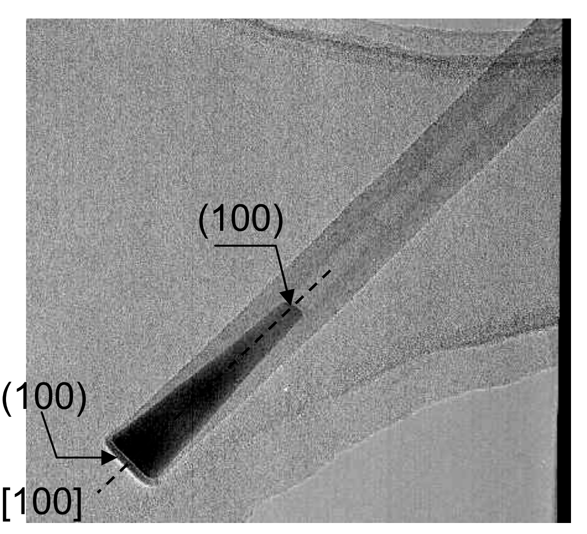
Ohmic contacts

D

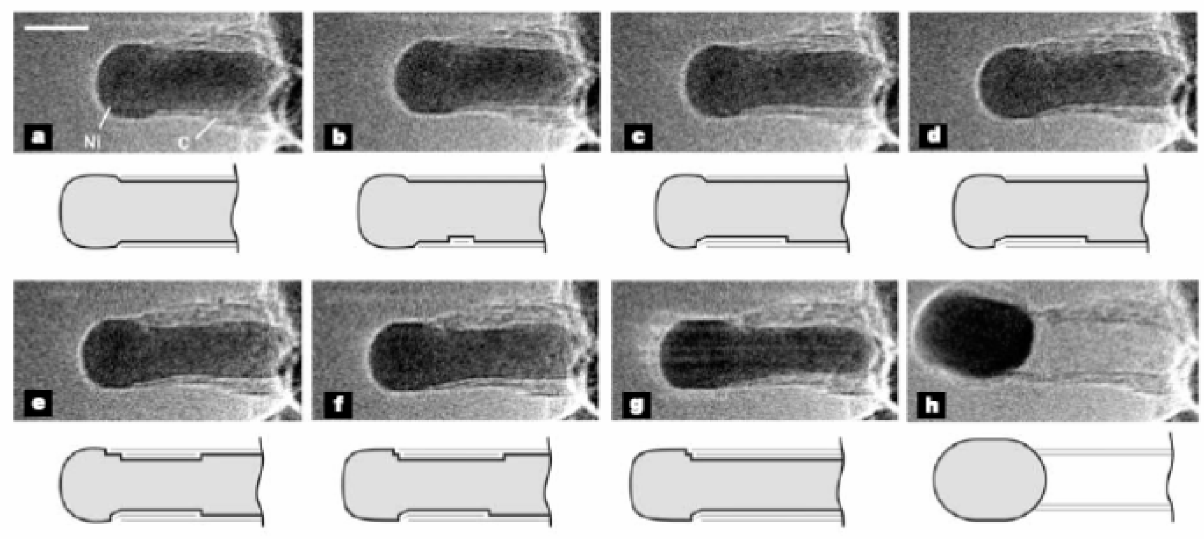
S

If L > λ: diffusive regime.
High carrier mobility

Chirality control?

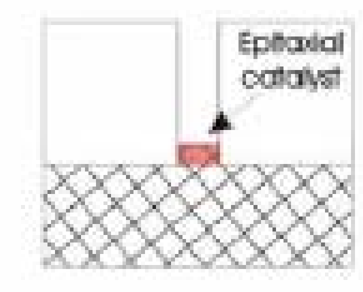


Orientation relation between a Fe catalyst particle and the CNT (after growth)



CNT nucleation on solid Ni particle T~ 480°C

« Epitaxial » catalyst

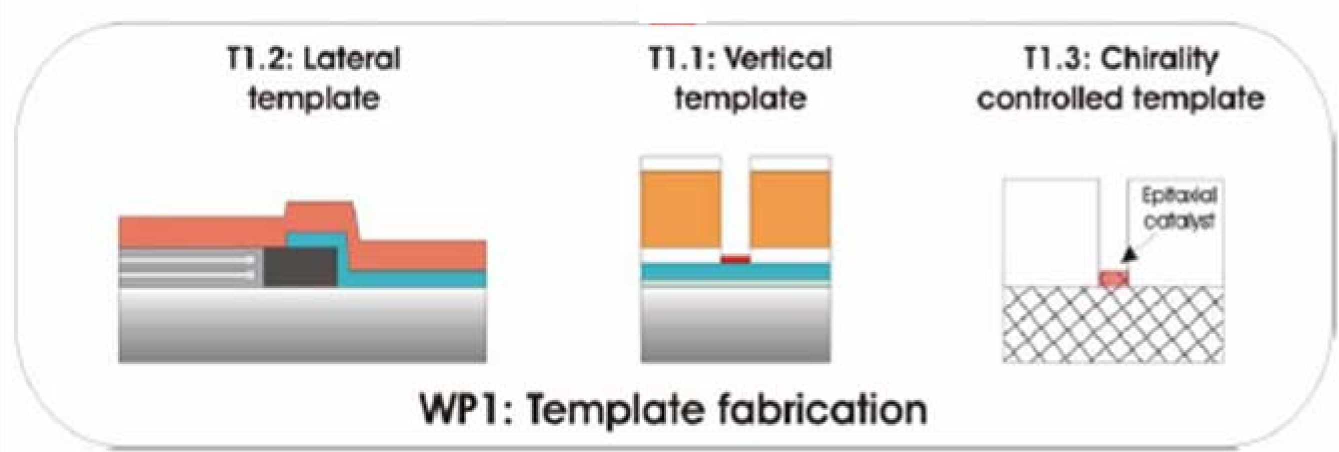


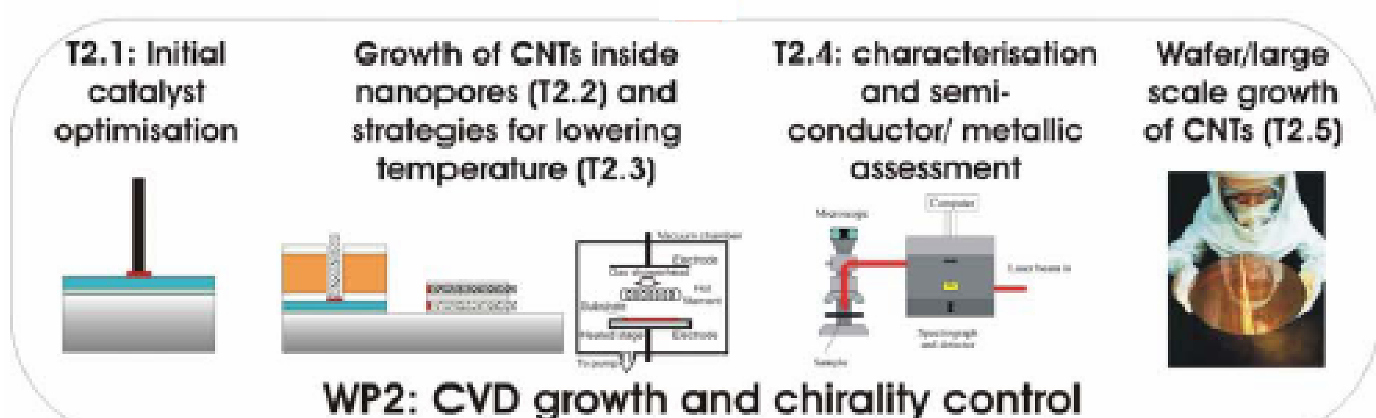
Vertical pores

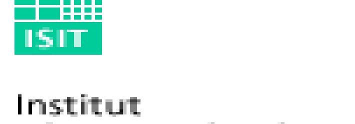
Ni, Co, Fe film
Insulating substrate
Resist
Al thin film
(1)
(2)
(3)
(4)
(5) CMP
(6) Etching
(7) Anodic oxydation & electrodeposition of catalysts
(8) Carbon nanotubes growth by CVD

Lateral pores

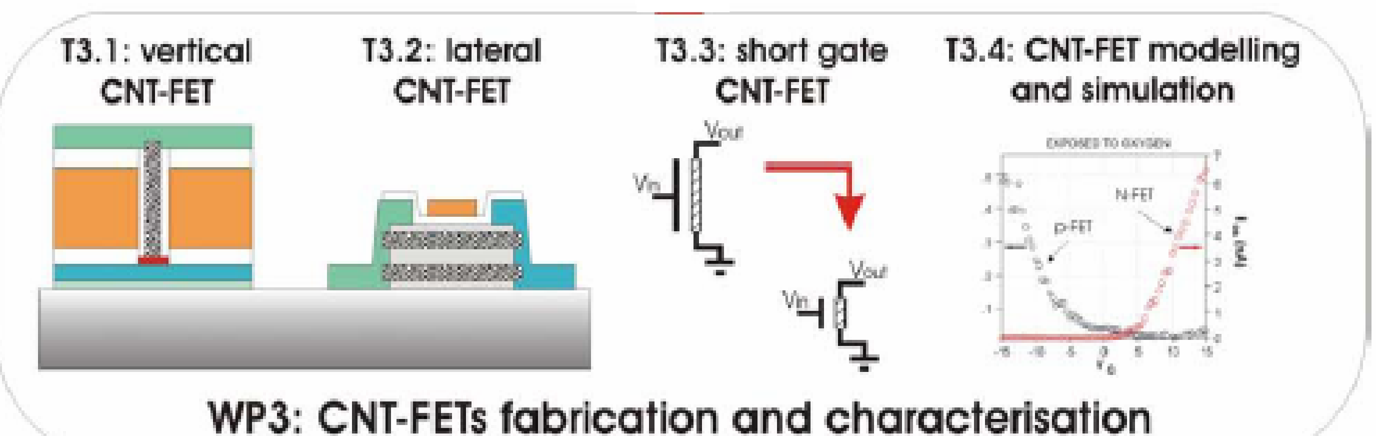
WP structure (1)

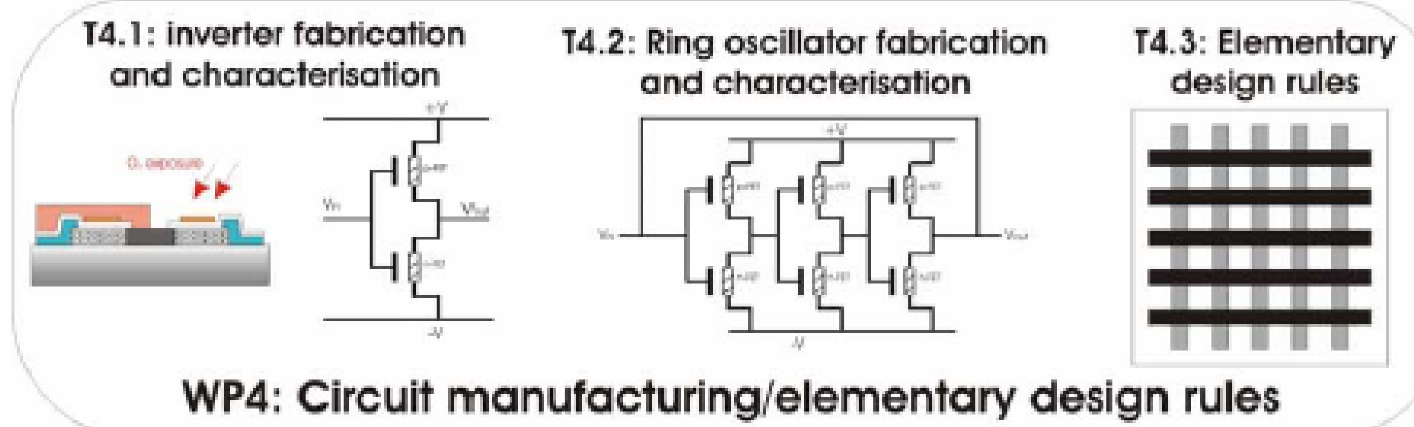






WP structure (2)





Project bar chart

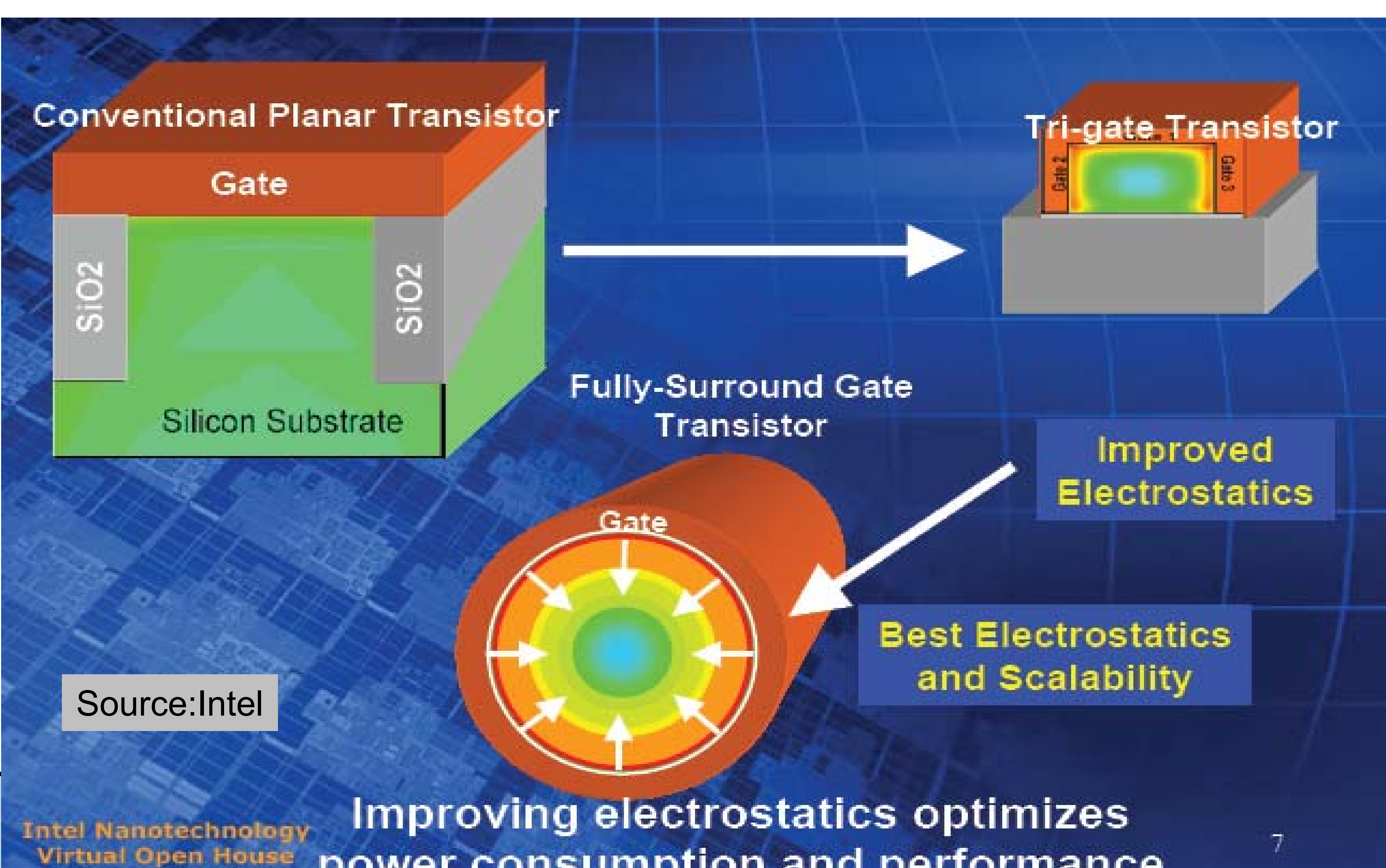
Workpackage description		Partner mm 1	2	3	4	T
WP1	**Template fabrication**					
T1.1	Vertical templates				15	15
T1.2	Lateral templates	12		3		15
T1.3	Templates for chirality control	5		4		9
WP2	**CVD growth and chirality control**					
T2.1	Initial catalyst optimisation		10	3		13
T2.2	Growth of carbon nanotubes inside nanopores	5	12	1		18
T2.3	Lowering growth temperature for chirality control	12	10			22
T2.4	Charact. and semiconductor/metallic assessment	4	9	3		16
T2.5	Wafer/large scale growth of carbon nanotubes		7			7
WP3	**CNT-FETs fabrication and characterisations**					
T3.1	Vertical CNT-FET	1			9	10
T3.2	Lateral CNT-FET	6		6		12
T3.3	Short gate CNT-FETs		13		5	18
T3.4	CNT-FET modelling and simulation	10			3	13
WP4	**Circuit manufacturing/Elementary design rules**					
T4.1	Inverter fabrication and characterisation	6	6	2	1	15
T4.2	Ring oscillator fabrication and characterisation	6	6	2	1	15
T4.3	Elementary design rules	1			1	2
T4.4	Assessment of CMOS compatibility	1	1	1	1	4
WP5	**Project management**	6	1	1	1	9
	Totals	75	75	26	37	213

Duration: ……….Year1……… ……..Year2…….. ……..Year3……..

We have been working on CNTs as well as on Si nanowires

Question: Can we include NWs in the project as well?

Evolution of device technology



Trigate/multichannel transistors

(b)
Source
Drain
Si
body
Gate

Non-planar
Tri-Gate
Architecture
Drain
Gate
Source

Source:Intel

The Ideal MOS Transistor

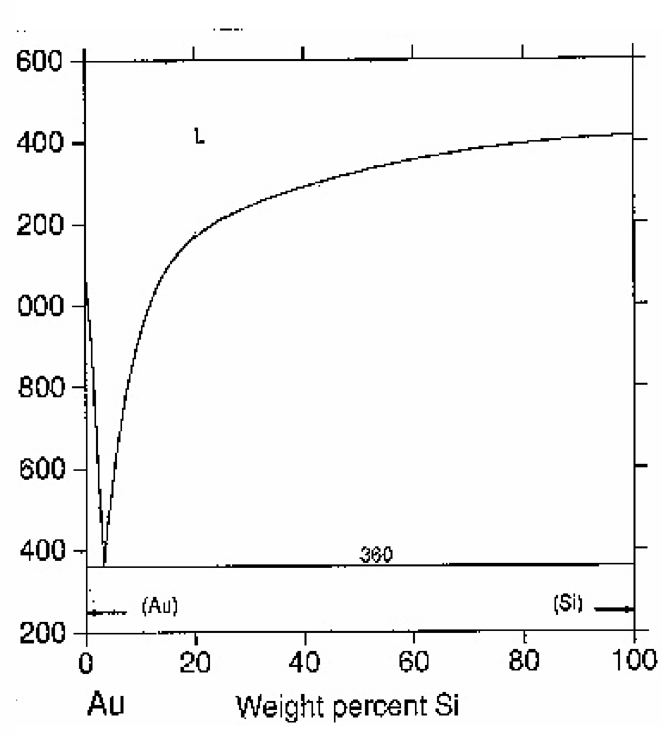
Source:Intel

Principle of the VLS Growth method

Weight % Si
Au 2 4 6 8 10
Temperature (°C)
600
400
363
300
(Au) + Liq.
Liq.
A
B
19.0
(Au) + (Si)
a) Au 10 20 30 40
Atom % Si

SiH4 vapor
Au-Si liquid alloy
substrate
b)

SiH4 vapor
Silicon crystal
c)



In principle:
Φ Crystal = Φ Au drop

VLS growth of Si whisker arrays