MAM2025

MARCH 24-27 • LEUVEN (BELGIUM)

ABSTRACTS BOOK

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FOREWORD

On behalf of the Organising and Scientific Committees, we take great pleasure in welcoming you to this new edition of the Materials for Advanced Metallization International Conference (MAM2025). MAM2025 will be the 32nd in a series of conferences devoted to research on materials and processes for the back and front end of the line, including interconnect and silicide materials.

Starting as a workshop on refractory metals and silicides in the 1980s and moving towards materials for advanced metallization in 1995, the objective of the conference is to provide a forum for open discussions across fundamental and applied sciences and industrial applications. It is dedicated to international material scientists, process and integration engineers, and students has attendees from universities, research institutions and industries. To meet the progressive downscaling of device dimensions and the demand for more functionality, the challenges fall to material solutions. New and extensive materials research is needed to further allow chip scaling as well as to develop novel nanoscale devices.

This year's conference is held in the De Hoorn, Leuven (Belgium). Leuven is known as a town steeped in academic history and De Hoorn is a former brewery, with a mythical place in the Belgian beer cultural heritage. In October 1925, Stella Artois was brewed there for the first time. Now 100 years later, surrounded by the original kettles and fermenters, we will be inspired with four days sharing new scientific results, rich discussions, and meetings between old friends adding to our own history and shaping the future.

The conference will be opened with keynotes by Paul Besser, Entegris, Shinichi Ogawa, AIST and Reinhold H. Dauskardt, Stanford University each giving their unique insights on the state of the materials industry and open three days of technical presentations and discussions across twelve sessions on research for the properties and interactions of Interconnect and Silicide materials. A further 19 invited talks will be given by scientific and technical leaders in key areas presenting the current state-of-the-art and to stimulate technical discussions.

Prior to the technical sessions of MAM2025, a workshop will spotlight Atomic Layer Deposition (ALD) as the enabler of the industry scaling roadmap. We have 8 distinguished speakers from both industry and university to talk about the ways ALD will help in different logic and memory and devices, support pattering scaling, enable 3D device architectures, realise new 2D based materials and enable other application drivers in emerging areas.

We are indebted to JX Advanced Metals for their financial support. Furthermore, we are grateful to the Phantoms Foundation for their organisation and logistical support. Lastly, we also would like to thank all the speakers, poster presenters, exhibitors and participants that joined us in person this year to make the conference a success.

Hope to see you again in the next edition of MAM.

Christopher J. Wilson - General Chair MAM2025

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- Top and bottom electrodes
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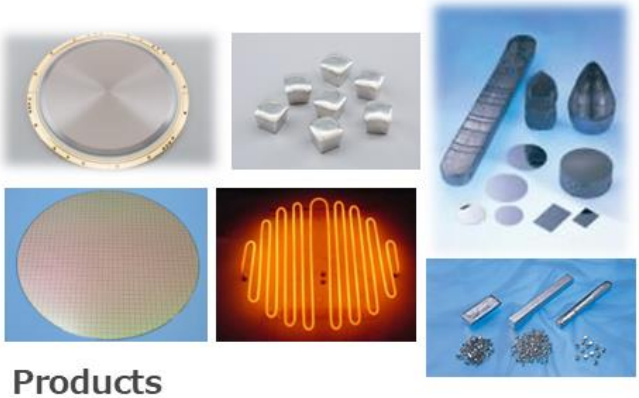

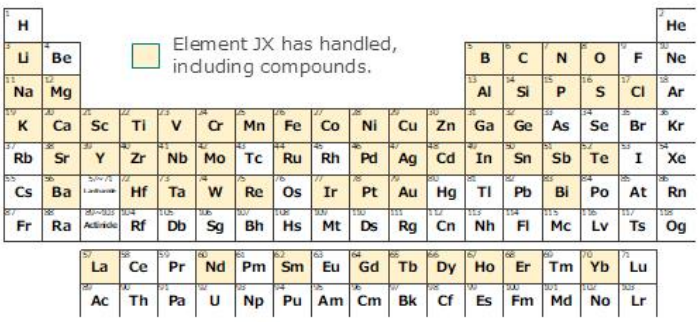

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Materials Innovations Driving AI

Dr. Paul R. Besser
Enterprise Fellow
Entegris, Inc.

A search engine describes AI as the ability of machines to perform tasks that typically require human intelligence. However, to semiconductor technologists, AI is composed of multiple, high performing logic/graphics processors working in parallel with hyper fast interconnections to stacked high bandwidth memory.

AI pushes processor performance and technology innovation to their limits. Device manufacturers accomplish this by reducing dimensions of the features, inserting novel architectural improvements and introducing new materials and processes. In this presentation, the evolution of processors will be highlighted, with particular emphasis on the novel materials necessitated as technologies scale. Changing one material in the process can have a cascading effect on subsequent processing steps, and the development of a yielding, manufacturable process requires a fundamental understanding of these process interactions as new materials are introduced to enable AI.

Directed Self-Assembly Exploiting Combustion Synthesis for Next-Generation Nanomanufacturing

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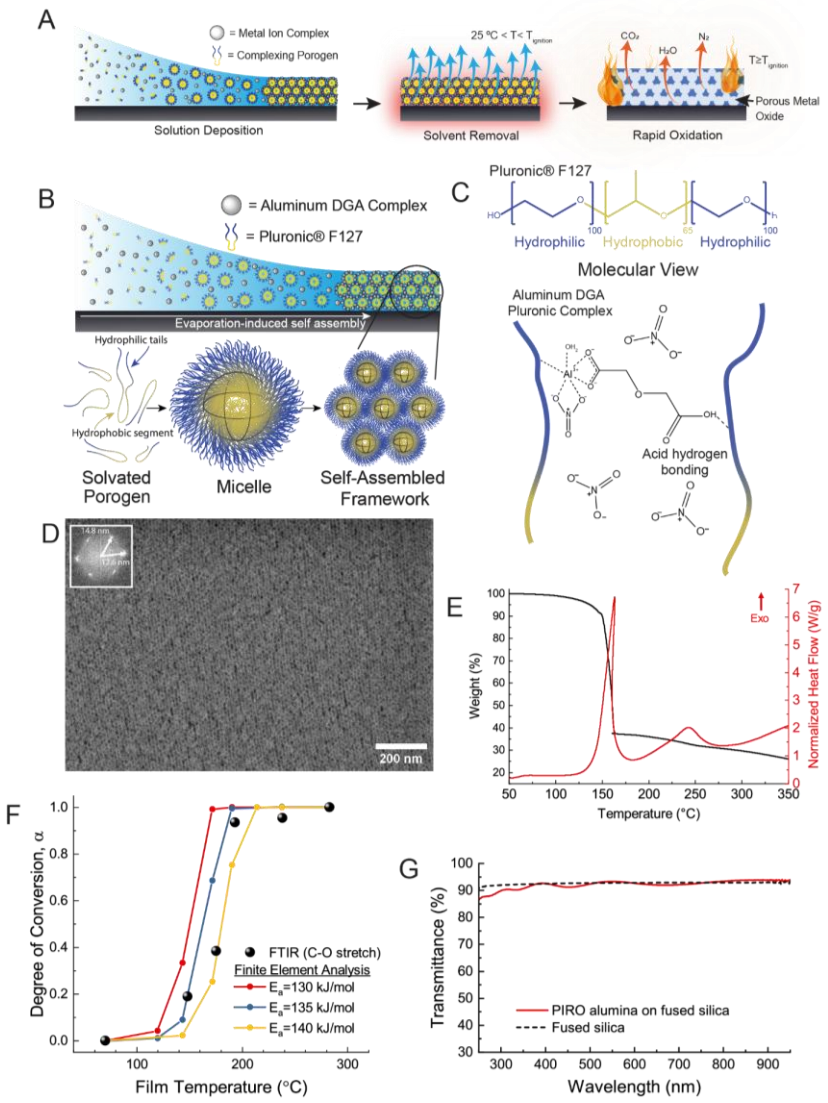
Structured metal oxide films have promise in optoelectronics, sensing, energy storage, and catalysis, however, current manufacturing techniques to form the mesoporous oxides involve expensive and low-throughput fabrication techniques. Porous metal oxides generated via traditional sol-gel approaches often require aging and sintering processes over many hours or days to yield controlled, meso-scale porosity at the cost of manufacturability.

I will describe research showing how we use a self-assembling polymer to act as the fuel source in a combustion reaction to generate highly structured nanoporous aluminum and other transition metal oxide films at <250°C in a matter of minutes through a process we term porogen-integrated rapid oxidation (PiRO). The resulting films show an open-cell, face-centered cubic structure of spheroidal pores. Further, an additional ligand can be coordinated to the metal cation to control the self-assembly step.

Finally, we demonstrate roll-to-roll manufacturing with PiRO on flexible polymeric substrates. The nanoporous metal oxide films can be filled with a second phase polymer phase to produce nanocomposite films with desirable mechanical, thermal and dielectric properties. Our method therefore offers a tunable, scalable, low temperature, and hence lower-cost method to generate large area structured nanoporous and nanocomposite metal oxide films.



Porogen integrated rapid oxidation (PiRO) greatly enhances manufacturability of thin film transition metal oxides with ordered nanoporosity.

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Materials, Processes, and Characterization: Insights from the Past for Advancing Interconnect Developments

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A multilayer CMOS device with laser-recrystallized Si islands was presented at the 1983 IEDM (Fig.1) [(1)]. Polycrystalline Si and W interconnects withstood high-temperature processing (900°C), but achieving reliable ohmic contacts remained a challenge (Fig.2). Today, engineers focus on commercializing 3D-structured devices, while research on 2D material devices is also gaining momentum. However, metal-2D material contacts remain problematic [(2)], indicating that the issue of "contact" persists.
The Ti/Si contact interface was studied in correlation with barrier height using high-resolution microscopy (HRM) [(3)]. A 1 nm electron probe enabled interface analysis for the first time, revealing a thin Ti-Si alloy even in the as-deposited state (Fig.3 (a), (b)). Crystallization began above 430°C, forming C49 TiSi at 460–625°C. Near the Si interface, the alloy remained amorphous but approached a $TiSi_2$-like composition, reducing the electrical barrier height around 460°C.
This new 1 nm probe also facilitated crystallinity characterization within a precise 1 nm area, aiding structural and electrical analyses of dry-etched low-k patterns (Fig.4). [(4).] These HRM advancements in the 1990s significantly contributed to interconnect technology development.

Helium ion microscopy (HIM), a prototype developed in 2006, has been used to manipulate the electrical properties of ultrathin 2D and superconducting materials for novel device fabrication. Graphene, now employed as a capping layer for Cu interconnects (Fig.5) [(5)], holds significant potential. A 0.35 nm diameter helium ion beam creates crystal defects in graphene or superconducting films—typically undesirable in semiconductors—but opens new possibilities for defect engineering.
The helium ion irradiation has been shown to transform graphene into a semiconductor or dielectric with 0.1–2% defect concentrations, enabling graphene transistors (Fig.6) [(6)]. In h-BN films on Au wires, it generated boron vacancies with nanometer precision, which acted as quantum sensors for magnetic fields (Fig.7) [(7)]. In YBCO superconductors, oxygen disordering induced by the irradiation converted films into metals or insulators, forming 1–2 nm width Josephson junctions [(8)].
HIM also enables precise graphene etching, similar to Ga FIB but with less damage, producing 18 nm-pitch nanopore arrays that induce an energy gap and control thermal transport (Fig.8) [(9)].

New materials, such as 2D materials and superconductors, will be integrated into 3D devices. Despite challenges, small electron probes and innovative characterization methods will overcome obstacles and advance defect-engineered processes for next-generation devices.

References

1. S. Akiyama, S. Ogawa et al. "Multilayer CMOS Device Fabricated on Laser Recrystallized Si Islands", IEDM Tech. Dig. p.352 (1983)
2. Contacts in 2D. *Nat Electron* **5**, 255 (2022). https://doi.org/10.1038/s41928-022-00783-1
3. S. Ogawa, et al. "Interface micro-structure of titanium thin film/silicon single crystal substrate correlated with electrical barrier heights," J. Appl. Phys 70, 827 (1991)
4. M. Shimada, S. Ogawa, et al. "2-Dimensional Distribution of Dielectric Constants in Patterned Low-k Structures by a nm-probe STEM / Valence EELS (V-EELS) Technique", Proc. of IITC, p.88 (2005)
5. T. Matsumoto, Low-Dimensional Nano-Carbon Material Synthesized by Microwave Plasma CVD for Cutting Edge Interconnects: Proc. of ISPlasma2025/IC-PLANTS2025, 07aB01I (2025)
6. S. Nakaharai, S. Ogawa, et al. "Conduction tuning of graphene based on defect-induced localization", ACS Nano, 7, pp. 5694-5670 (2013)
7. A. N H. Gu, S. Ogawa, et al. "Systematic characterization of nanoscale h-BN quantum sensor spots created by helium-ion microscopy", PHYSICAL REVIEW APPLIED 22, 054026 (2024)
8. S. Ogawa, et al. "Formation of Lateral-Type High-Tc Superconductor Josephson Junction by Helium Ion Microscopy", Proc. of IITC, P.8 (2024)
9. M.E. Schmidt, S. Ogawa, et al. "Structurally Controlled Large-Area 10 nm Pitch Graphene Nanomesh by Focused Helium Ion Beam Milling", ACS Appl. Mater. Interfaces 10, pp. 10362-10368 (2018)

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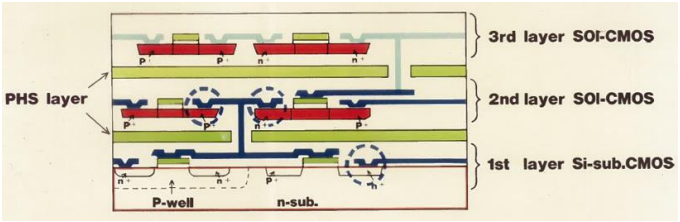


Fig. 1

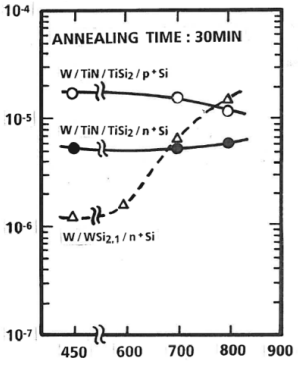


Fig.2

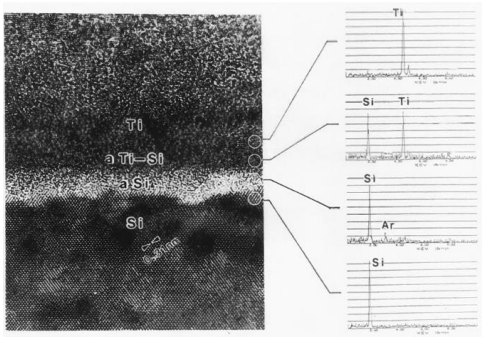
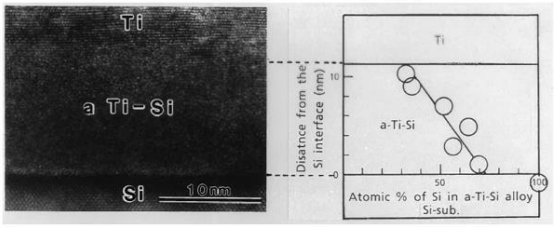


Fig. 3(a)



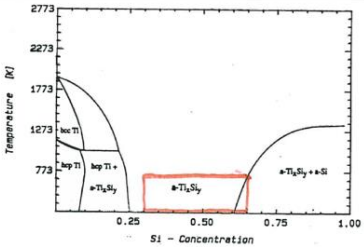


Fig. 3(b)

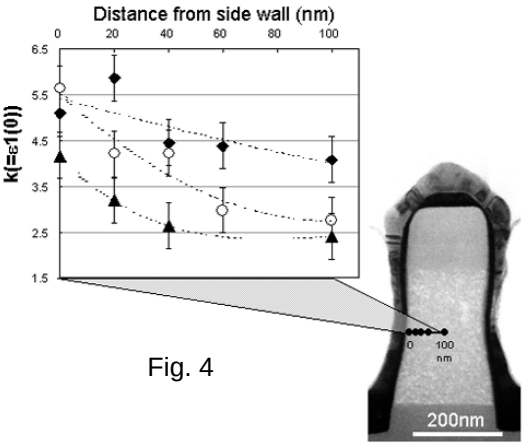


Fig. 4

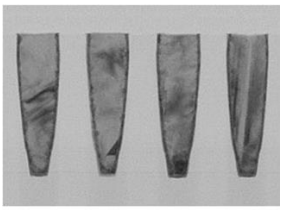


Fig. 5

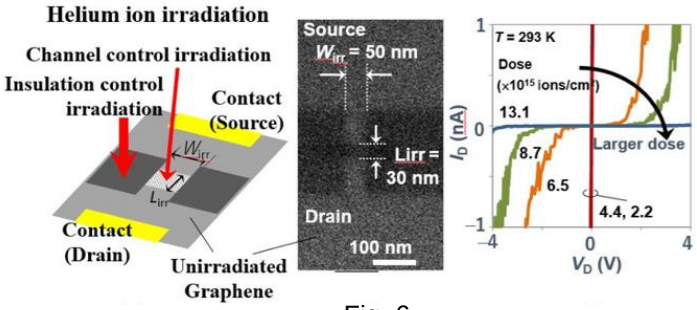


Fig. 6

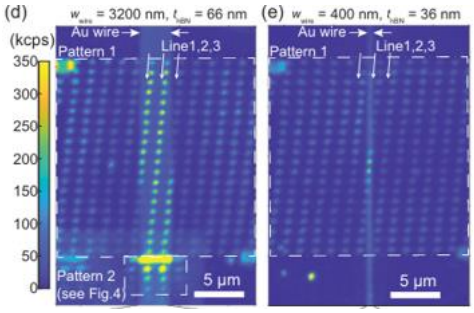


Fig.7

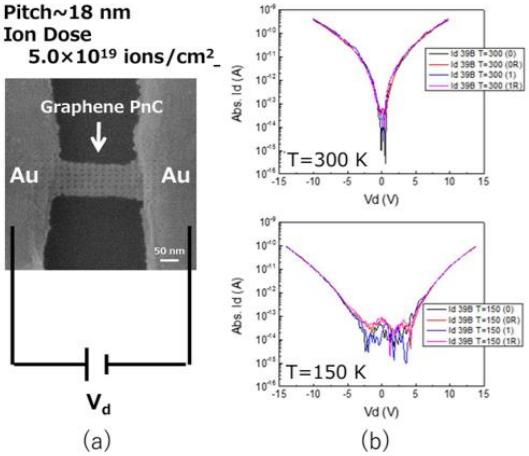


Fig. 8

Defects in Action: Real-time TEM observation of Nickel Silicide Propagation in Silicon Nanowires

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Nickel silicide nanowires (NWs) exhibit low resistivity, high structural stability, and excellent compatibility with silicon technology, making them highly attractive for use as interconnects in nanoelectronics [1,2]. In this study, we present a solution-based synthetic [3,4] approach to fabricate Sn-catalyzed, defect-rich silicon (Si) NWs grown from nickel (Ni) NW stems. This synthesis approach provides a unique platform to investigate the reaction kinetics and mechanistic understanding of silicide formation in more complex NW architectures.

To probe the transient dynamics of Ni silicide formation within these Si NWs, we employed *in situ* heating electron microscopy. Our real-time observations reveal varying degrees of non-uniform silicide formation depending on the NW morphology, surface conditions, and crystallographic defects. Furthermore, we captured the process of interfacial segregation in the Ni silicide system, induced by the nanowire catalyst. These results provide new insights into defect-mediated metal diffusion and phase transformation in NW systems, offering crucial guidance for the design, optimization, and reliability of silicide-based nanodevices [5].

References

1. W. M. Weber *et al*., *Nano Lett.* **6**, 2660 (2006)
2. Y. Song *et al*., *Nano Lett.* **7**, 965 (2007)
3. C. A. Barrett *et al*., *Chem. Commun.* **47**, 3843 (2011)
4. M. Sheehan *et al*., *Nanoscale* **10**, 19182 (2018)
5. T. E. Adegoke *et al*., *ACS Nano* **18**, 10270 (2024)

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Eco-design in ST: a Sustainable Journey

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We will present here a summary of STMicroelectronics (ST) Sustainability Journey that have started in 1987. We will zoom into ST sustainable product life cycle, ST responsible product definition and criteria. We will present some examples of ST product Life Cycle assessment (LCA) describing carbon footprint from cradle to grave. We will explain what ECO Design practices in ST are, why links with data & management system are key. We will conclude with future challenges we are facing in this domain. Strategic move we are doing is by a shift left approach to anticipate as much as possible sustainability criteria into product R&D & multiple associated engineering fields.

Table 1: ST Responsible product criteria

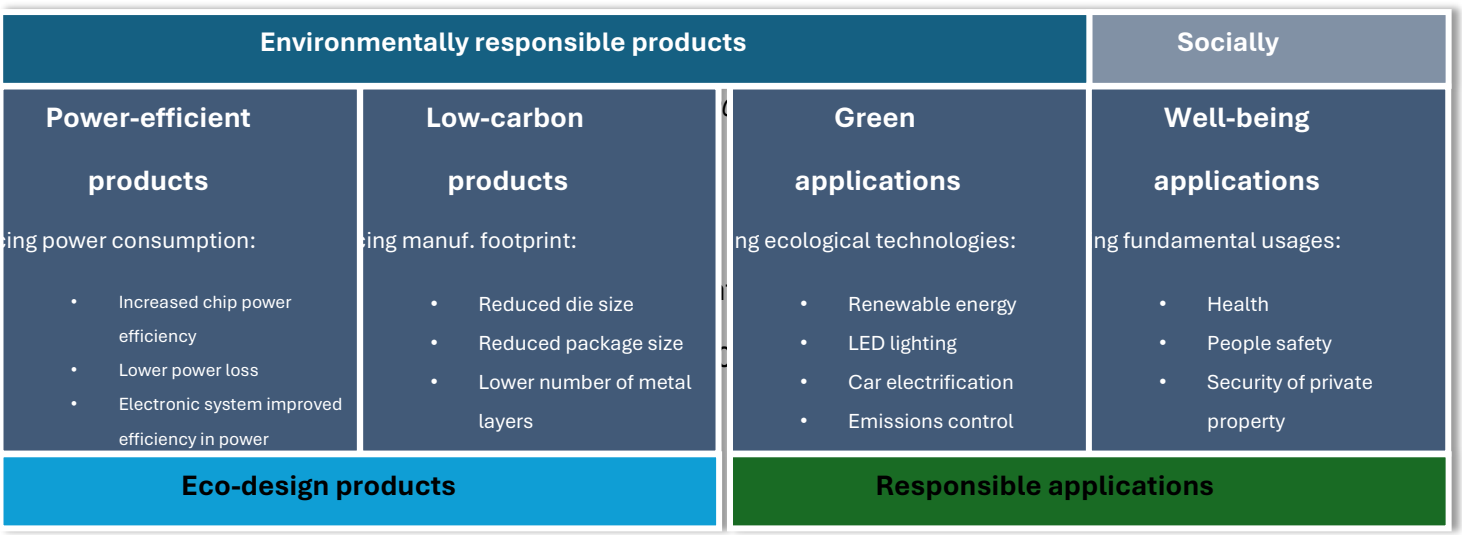

Table 2: ST ECO-Design criteria

	Wafer Technology	Package Technology	Chip Design	Software development	Test engineering
Environmental KPI	✓	✓	✓	✓	✓
Direct / Indirect material consumption	✓	✓			✓
Energy consumption	✓	✓	✓	✓	✓
Water usage	✓	✓			
CO2 equivalent KPI	✓	✓	✓	✓	✓

Back-end-of-line integration of emerging memory technologies for neuromorphic edge computing

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The transition from cloud-based data classification to edge computing has facilitated real-time data processing in closer proximity to sensors, thereby reducing latency and enhancing efficiency. However, this paradigm introduces stringent constraints on power consumption, compactness, and performance [1, 2]. Addressing these challenges necessitates unconventional hardware solutions capable of meeting these demanding requirements.

Brain-inspired architectures, notably spiking neural networks (SNNs), present a compelling solution to low-latency, stateful, and energy-efficient computation [3]. Nevertheless, existing implementations primarily depend on digital or mixed-signal Complementary Metal-Oxide-Semiconductor (CMOS) technologies, which are unable to satisfy the rigorous memory, area, and power constraints of edge computing. The integration of emerging memory technologies at the back-end-of-line (BEOL) of CMOS circuits od in 3D arrays offers a compelling opportunity to enhance neuromorphic hardware [1, 4]. Indeed, emerging non-volatile memory devices hold the promise to enable energy-efficient, massively parallel computing architectures due to their CMOS-compatible operating voltages and analogue behaviour [2, 4, 5]. These properties facilitate the hardware implementation of efficient neural dynamics and synaptic plasticity [4, 6], which are key attributes for hardware-based brain emulation. However, realising this potential requires overcoming critical challenges, including fabrication compatibility, device variability, reliability, scalability, and system integration [4, 5].

This presentation underlines the necessity of design-technology co-optimization (DTCO) to enable the seamless integration of emerging memory devices with CMOS circuits, providing a design foundation for future memory systems based on BEOL and 3D integration of emerging memory devices. It will address challenges and opportunities in the collaborative design of devices, circuits, and architectures, emphasising the necessity for a holistic approach to fully realise the potential of neuromorphic computing at the edge.

Acknowledgments
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References

1. E. Covi et al., Front. in Neurosci. **15**, 611300 (2021).
2. D. V. Christensen et al., Neuromorph. Comput. Eng. **2**, 022501 (2022).
3. E. Chicca et al., Proc. of the IEEE **102**, 1367 (2014).
4. D. Ielmini and S. Ambrogio, Nanotech. **31**, 092001 (2019).
5. A. Amirsoleimani et al., Adv. Intell. Sys., 2, 2000115 (2020).
6. E. Covi et al., Neuromorph. Comput. Eng. **2**, 012002 (2022).

* *corresponding author e-mail:* e.covi@rug.nl

Engineering electronic and optical properties of semiconductors by tuning the population of dopant defects: first principles simulations of Chalcogen hyperdoped Si

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Since Mott's work the insulator-to-metal transition (IMT) in doped semiconductors has been studied both for its interest in fundamental physics and for its relevance in technological applications. In this framework, hyperdoping (i.e., doping beyond the solubility limit of the impurity) creates a new materials playground to investigate impurity mediated IMTs in semiconductors and provides a key material in forthcoming devices based on Si and Ge technology.

Hyperdoping is currently being used to engineer new materials with unique and exotic properties: rectifying junction and photodiodes with S and Se hyperdoped Si. Furthermore, Si and Ge hyperdoped with chalcogens (Ch=S, Se, and Te,) are considered promising candidates as building blocks for infrared absorbers and intermediate band photovoltaics. Hyperdoping is also a promising technique to reach density of the order of one carrier per cubic nanometer, which may be necessary to develop nanometer-sized ballistic devices. Unfortunately, at hyperdoped concentration, the elements usually employed to dope silicon -like P, As, or Sb- form complexes that acts as electrical deactivation centers, producing the phenomena of carrier saturation, thus preventing to reach the carrier density needed for nano-devices.

Among dopants, chalcogens provide superior electronic properties (high carrier concentration, and no saturation) than traditional column V dopants [1] (see Fig.1). Within the framework of density functional theory, by plane-waves pseudopotentials techniques and the supercell method, we systematically investigated chalcogen hyperdoped Si by computing, for different types of Ch complexes, the formation energy as a function of Ch concentration.

We enlightened the microscopic mechanisms responsible for the disappearance of electrical deactivation defects as the chalcogen density approaches the critical concentration, x_c, at which the IMT occurs. Our study showed that, as the Ch concentration approaches x_c, the electrical deactivation defects are energetically unfavored due to their formation energy significantly higher (1 eV or more, depending on the type of defects) than the ones of donor complexes, identified as the Ch monomer (a single substitutional dopant), Ch-Ch dimer (two nearest neighbor substitutional dopants), and the VCh3 (VCh4) complexes formed by a Si vacancy having 3 (4) nearest neighbor substitutional Ch (Fig.2). We discuss the electrical properties of Ch complexes in Si, finding the best doping range in which the Ch density can be tuned to engineer both x_c and the optical properties of the material.

By combining our first-principles data with a random distribution model for estimating the relative percentage of distinct types of S complexes in S-hyperdoped silicon, we predict an unprecedented tunability of the IMT transition at the critical dopant concentration, with a key role played by the relative abundance of the different complexes. By assuming the possibility to tune the latter during the sample synthesis, we predict that optical absorption spectra of S-hyperdoped Si can be engineered from the short wavelength infrared to far infrared region.

References

1. M. Wang, A. Debernardi, Y. Berencén, et al, Phys. Rev. Appl. 11, 054039 (2019).
2. A. Debernardi, Phys. Chem. Chem. Phys., 23 24699-2471 (2021).
3. A. Debernardi, Semicond. Sci. Technol. 38, 014002 (2023).

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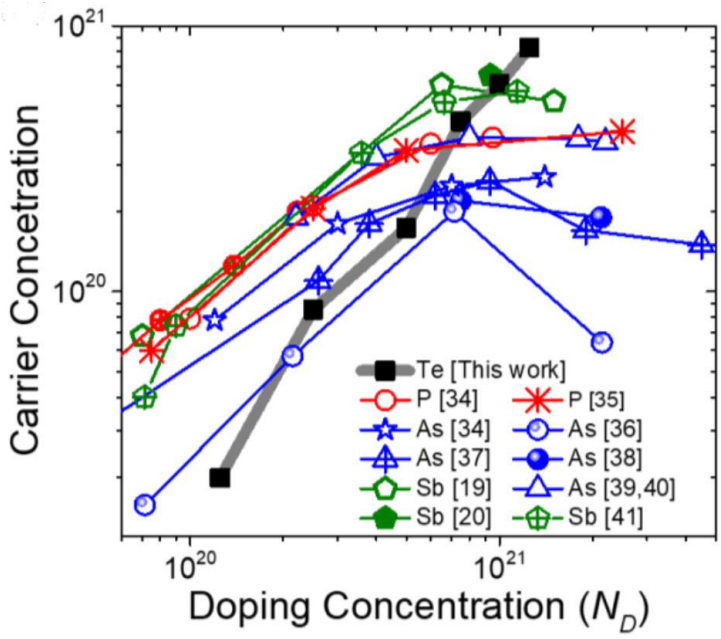

Figure 1. Electron concentrations as a function of dopant concentration in hyperdoped silicon for different types of dopants [adapted from Wang et al. Phys.Rev.Appl. 11, 054039 (2019) (Ref. [1])]

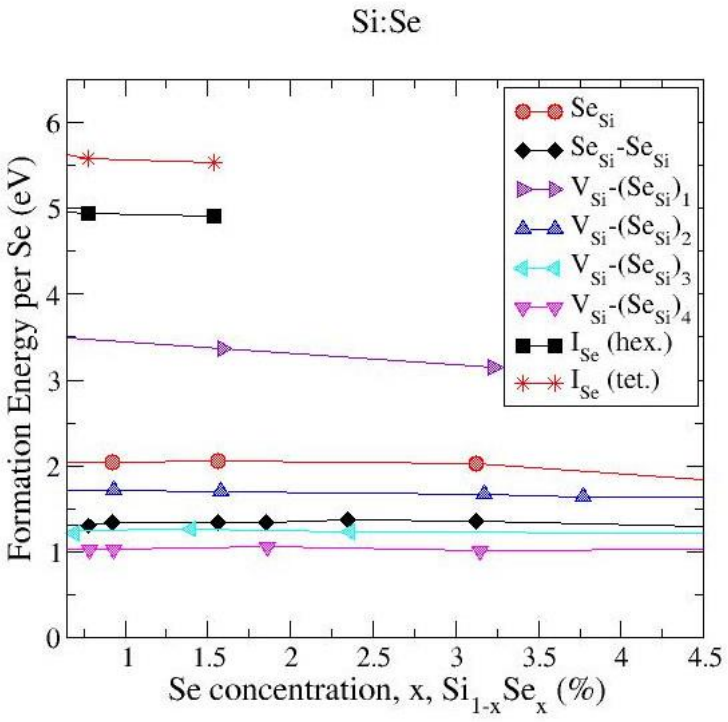

Figure 2. Symbols: first principles formation energy as a function of dopant concentrations for different types of complexes in Se hyperdoped Si (Ref.s [2,3]). Solid lines are a guide for eyes.

Photoluminescence Imaging: Shedding Light on the Invisible Defects in Silicon

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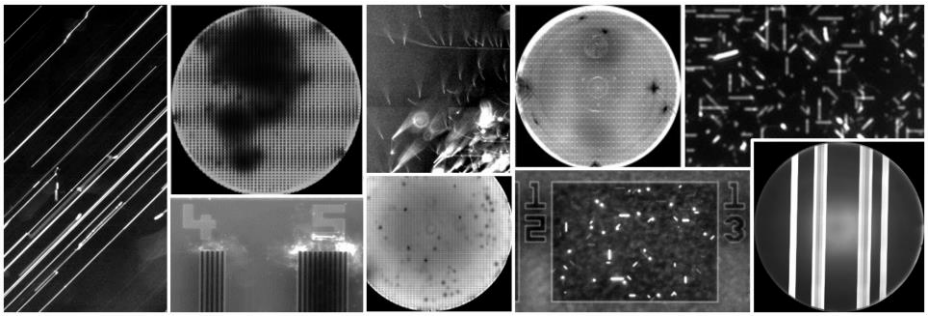
Photoluminescence (PL) stands as a powerful optical method for characterizing silicon and III-V semiconductors, providing valuable insights into material quality, semiconductor band-gap, and local dynamics. Originating in the photovoltaic industry, the specific PL imaging technique has now permeated silicon CMOS manufacturing, reshaping defect analysis through its non-destructive capabilities.
Unlike traditional PL spectroscopic methods, room temperature PL imaging leverages bandpass optical filters to swiftly capture spatially resolved data integrated across a wide range of wavelengths. This approach enables rapid acquisition of large sample areas with spatial resolution and sensitivity surpassing the limitations of conventional scanning PL systems with in-line observation of non-visual buried defects being a typical CMOS application.
During this presentation, STMicroelectronics' expertise in PL imaging will be illustrated, highlighting its pioneering role in detecting and characterizing silicon defects induced by ionic implantation [1-3] and exploring novel applications within the CMOS manufacturing environment:

- Silicon crystallographic defects originating from epitaxy [4], thermal treatments [5] and stress induced by patterning
- Substrate defectivity: BMDs, Oi precipitates
- Substrate metallic contamination [6, 7]

Embark on a journey into the realm of photoluminescence to uncover the transformative potential of this technology in semiconductor manufacturing.



1. Duru, R., et al. (2017, May). Photoluminescence for in-line buried defects detection in silicon devices. In 2017 28th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) (pp. 262-266). IEEE.
2. Duru, R., et al. (2018). Photoluminescence imaging for buried defects detection in silicon: Assessment and use-cases. IEEE Transactions on Semiconductor Manufacturing, 32(1), 23-30.
3. Joblot, et al. (2018, September). Characterization of Heated Ion Implantation for non Amorphizing Conditions and Correlation with Kinetic Monte Carlo Simulations. In 2018 22nd International Conference on Ion Implantation Technology (IIT) (pp. 121-124). IEEE.
4. Frascaroli, et al. (2022). Automatic defect detection in epitaxial layers by micro photoluminescence imaging. IEEE Transactions on Semiconductor Manufacturing, 35(3), 540-545.
5. Duru, R., et al. (2022, May). Photoluminescence imaging for slip line detection and characterization in silicon substrates. In 2022 33rd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) (pp. 1-6). IEEE.
6. Nassiet, T. (2021). Photoluminescence industrielle : Une application innovante pour le développement et le contrôle des technologies imageur (Doctoral dissertation, Université de Lyon).
7. Alcaire, T., et al. (2022, May). Full Wafer Process Control Through Object Detection Using Region-Based Convolutional Neural Networks. In 2022 33rd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) (pp. 1-5). IEEE.

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The role of interface chemistry and crystalline defects on the reliability of 4H-SiC MOSFETs

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The need of high efficiency energy conversion systems is expanding the silicon carbide (4H-SiC) device demand in applications with high reliability constrains (i.e. automotive etc). This imposes the scientific community to acquire a deeper comprehension of the physical phenomena affecting the device integrity under prolonged stress, with a particular focus on the impact of the crystalline defects in the semiconductor epitaxial layer. However, threshold voltage (Vth) instability phenomena and poor field effect channel mobility (μFE) are still observed in 4H-SiC MOSFETs, and can be only partially mitigated by the gate insulator post-oxidation (POA) or post-oxide deposition annealing (PDA) processes.
In this context, in this invited talk, some reliability concerns affecting the performances of 4H-SiC MOSFETs are discussed. In particular, the following aspects will be addressed: the SiO2/SiC interface chemistry and the impact of the device fabrication processes on the MOSFET threshold voltage (Vth) stability, and the impact of the semiconductor crystalline defect on the device lifetime.
4H-SiC MOSFETs were characterized by means of current voltage (ID-VG) transfer characteristics and capacitance–voltage (C-V) measurements. Furthermore, on selected failed devices, Scanning Transmission Electron Microscopy (STEM) analyses combined to electron energy loss spectroscopy (EELS), and electrical Scanning Probe Microscopy (SPM) analyses have been used to elucidate the physical mechanisms affecting their reliability. It will be shown that correlative macroscopic and microscopic (down to nanoscale) analyses are needed to fully comprehend the physical properties of the semiconductor/insulator interface and how these properties affect the real devices.
An important aspect is related the dielectric breakdown of 4H-SiC MOSFETs correlated to the presence of different crystalline defects in the 4H-SiC epitaxial layer. Of particular interest are the wafer level characterization of both the failed devices at t=0s, and of the devices showing an anomalous Fowler-Nordheim (FN) gate bias conduction. In fact, it is possible to correlate devices failing under high temperature gate bias (HTGB) stress with the presence of an anomalous FN behavior and the presence of a surface bump on the semiconductor. Moreover, the role of the threading dislocation (TD) in high temperature reverse bias (HTRB) failures was demonstrated employing high-resolution SPM techniques. These nanoscale methods elucidated the physical mechanism of the dielectric breakdown, revealing an increase of the minority carrier concentration close the insulator/semiconductor interface.
Furthermore, a method to monitor the Vth variation from single point drain current (ID) measurement using a single gate bias (Vread) value is presented. This method allowed to probe the interface states close to the 4H-SiC conduction and valence band edges and the amount of trapped charge at the interface close to 4H-SiC band edges (Nit) and inside the near interface oxide region (NIOTs).
These finding demonstrated that the threshold voltage instability of 4H-SiC MOSFETs, associated to different trapping mechanisms, is directly related to the SiO2/SiC interface chemistry and can be mitigated by an accurate control of the nitridation conditions of deposited oxides.

References

1. P Fiorenza, F. Giannazzo, S. Cascino, M. Saggio, F. Roccaforte. Appl. Phys. Lett. 117, 103502 (2020)
2. P. Fiorenza, C. Bongiorno, F. Giannazzo, M. S. Alessandrino, A. Messina, M. Saggio, F. Roccaforte; Appl. Surf. Sci. 557 149752 (2021)
3. P. Fiorenza, M S Alessandrino, B Carbone, C Di Martino, A Russo, M Saggio, C Venuto, E Zanetti, F Giannazzo, F Roccaforte Nanotechnology 31 (2020) 125203
4. P. Fiorenza, S. Adamo, M. S. Alessandrino, C. Bottari, B. Carbone, C. Di Martino, A. Russo, M. Saggio, C. Venuto, E. Vitanza, E. Zanetti, F. Giannazzo, F. Roccaforte, IEEE IRPS (2021)
5. P. Fiorenza, M. Zignale, M. Camalleri, L. Scalia, E. Zanetti, M. Saggio, F. Giannazzo, F. Roccaforte Mater. Sci. Semicon. Proc.169 (2024) 107866

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3D-stacking technologies: remaining challenges of co-integration of thin Ni(Pt)Si film and $TiSi_x$ contacts.

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In CMOS (Complementary Metal Oxide Semiconductor) devices, for technology nodes below 65 nm, Ni-based silicide has been widely used to provide an ohmic contact to the active Si regions (such as gate, source, and drain) [1]. Numerous advantages have been highlighted compared to previous Salicide integration (known as Self-Aligned Silicide), such as diffusion-controlled growth, which results in a smoother silicide/silicon interface, and easier formation in narrow active lines. Moreover, the formation of Ni(Pt)Si involves low silicon consumption, which enabled its introduction for Fully Depleted Silicon on Insulator (i.e., FDSOI) technology for the 28 nm node [2]. However, one of the major drawbacks of Ni(Pt)Si films is their low stability at high temperatures, i.e., morphological degradation due to the agglomeration phenomenon [3–5]. Particularly, for FDSOI technologies, the current thickness of Ni(Pt)Si films is reduced to 11 ± 1 nm, resulting in thin films prone to agglomeration. At device scale, solid-state agglomeration, or dewetting degradations, induce severe yield loss due to the obtained electrical discontinuity, as previously published [6]. Various published works have reported several key factors that promote Ni(Pt)Si layer agglomeration, such as film thickness, grain size, and texture [3–5]. More recently, we demonstrated a clear improvement in terms of agglomeration sensitivity of ultra-thin Ni(Pt)Si films for a specific annealing scheme, including Dynamic Surface Annealing (DSA) instead of the classical Rapid Thermal Annealing (RTA) [7].

Nowadays, new advanced 3D technologies such as FinFETs (Fin-type Field Effect Transistor), CMOS Image Sensors (CIS), or new smart power technologies are moving away from Ni(Pt)Si silicides to Ti-based silicide contacts [8]. In this context, Ti/TiN bilayers, usually used as diffusion barriers inside W contacts, have been employed as reactive metal layers to form TiSi-based ohmic contacts [9,10]. New 3D-stacking imaging technologies, among others, deal with a dual-layer device, where an image sensor is built on top of an up-to-date CMOS device ([11], Figure 1). This results in the co-integration of ultra-thin Ni(Pt)Si thin films and TiSi-based contacts in the same integrated circuit. Therefore, improving the Ni(Pt)Si layer sensitivity to agglomeration and forming TiSi-ohmic contacts at low temperatures appear to be critical for the integration of new 3D-stacking technologies.

In this paper, after a complete overview of different 3D-stacking integrations, we will discuss the advanced processes involved in the formation of ultra-thin Ni(Pt)Si films, including surface preparation, annealing schemes, and pre-amorphization by implantation (PAI). We will also cover the processes widely used for TiSi-based contacts optimization, such as Nano-seconds Laser Annealing (NLA). Finally, we will present the latest progress and the remaining challenges for such integrations.

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References

[1] C. Lavoie, et al. Microelectron. Eng. 70, 144 (2003).
[2] N. Planes et al., 2012 Symp. VLSI Technol. Dig. Tech. Pap. 133 (2012).
[3] C. V Thompson, Annu. Rev. Mater. Res. 42, 399 (2012).
[4] T. P. Nolan, , J. Appl. Phys. 71, 720 (1992).
[5] B. De Schutter, Appl. Phys. Rev. 3, 031302 (2016).
[6] C. Cavalcante et al., *2020 IEEE Symposium on VLSI Technology*, Vol. 1 (2020), pp. 3–4.
[7] F. Morris Anak, Materials Sci. Semicond. Process. 184, 108806 (2024).
[8] C. Lavoie, *ECS Transactions*, Vol. 77 (2017), pp. 59–79.
[9] G. T. Lai, IEEE Trans. Nanotechnol. 20, 761 (2021).
[10] M. Grégoire, , Micro Nano Eng. 2, 104 (2019).
[11] F. Guyader et al., , Tech. Dig. - Int. Electron Devices Meet. IEDM 2022-December, 3741 (2022).

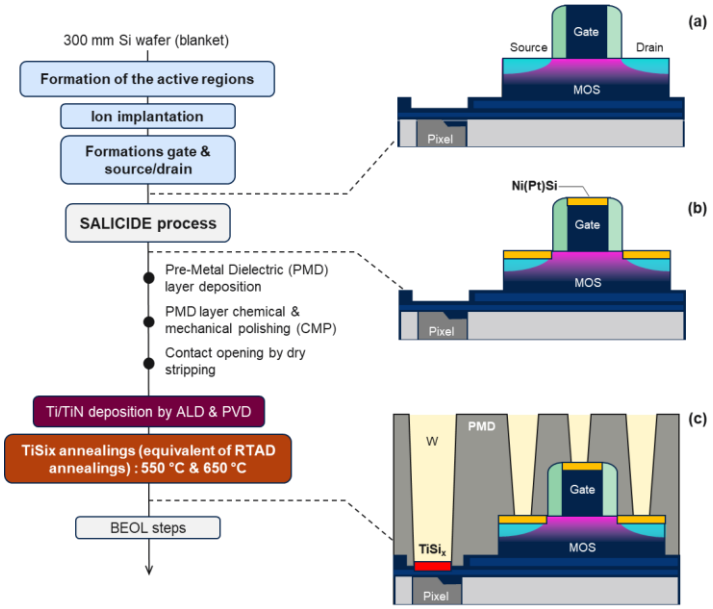

Figure 1. Description of a part of the process flow used to fabricate the integrated circuit involving the co-integration of Ni-silicide, Ni(Pt)Si and Ti-silicide, TiSiX presenting thermal budget incompatibility due to premature agglomeration of Ni(Pt)Si film during TiSix formation. Two type of annealings have been studied classical RTA (Rapid Thermal Annealing) and DSA (Direct Surface Annealing) to form Ni(Pt)Si thin films during SALICIDE process;

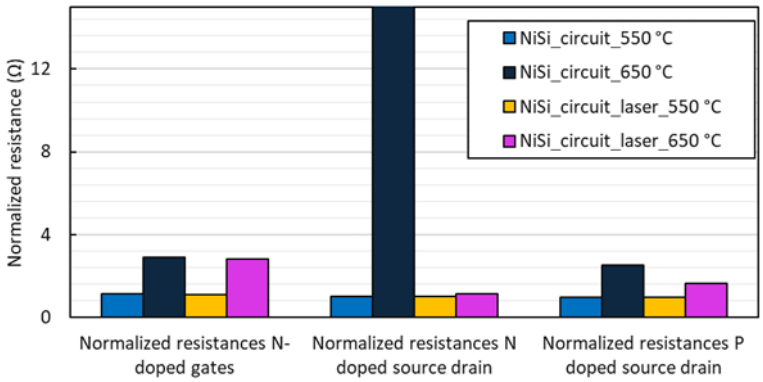

Figure 2. Normalized resistance, R (Ω), extracted from parametric tests on N-doped gates, source/drain, and P-doped source/drain for NiSi_circuit and NiSi_circuit_laser samples after $TiSi_x$ annealings at 550 and 650 °C.

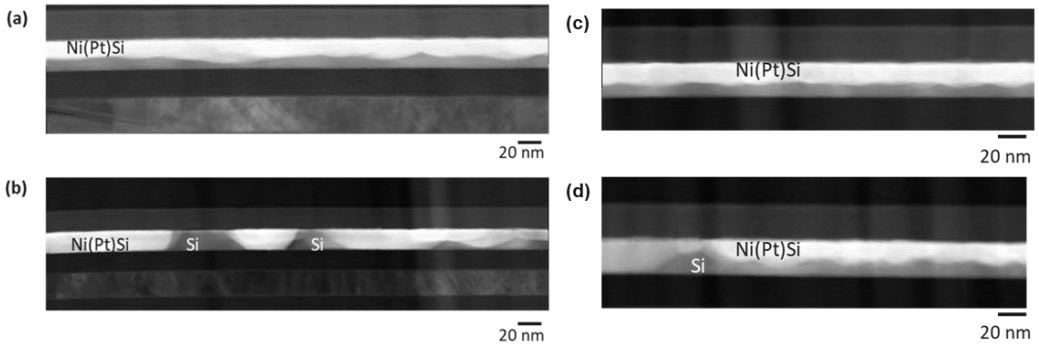

Figure 3 STEM cross-sections obtained for NiSi_circuit and for NiSi_circuit_laser samples for $TiSi_x$ annealings at (a,b) 550 and (c,d) 650 °C.

Electron and phonon thermal conductivity and scattering rates in metal and non-metal thin films and multilayers

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The progressive reduction in the characteristic length scales of logic technology nodes in very-large-scale integration (VLSI) has led to the need to find replacements for copper being used as interconnects. Both the thermochemical and thermomechanical stability of Cu at these length scales, along with the strong reduction in both electrical and thermal conductivity due to length scales reducing to those less than its electronic mean free path has led to underperformance, which in part can be ascribed to deleterious heating effects.[1] While Ru and W interconnects are currently being evaluated, a range of additional metals and metallic systems (alloys, eutectics and multilayers) are also of note due to their potential mechanical and thermal properties that are superior to Cu at the < 100 nm length scale. In this presentation, I will discuss our recent efforts in measurements of thermal conductivity and electron-phonon scattering rates of thin metal films for interest as next-generation metal interconnects, including Ru, W, Ir, Pt, Mo, Co and Ta. First, I will discuss the use of various thermoreflectance techniques – including time-domain thermoreflectance (TDTR), steady state thermoreflectance (SSTR),[2,3] and time resolved magneto-optical Kerr effect (TR-MOKE) – to measure the thermal properties of thin films, including the in-plane a cross plane thermal conductivity of thin films of metals, dielectrics, multilayer metals and multilayer chalcogenide phase change materials. I will then discuss how the measurement of in-plane thermal conductivity allows for direct comparison to k derived from electrical resistivity measurements and application of the Wiedemann-Franz (WF) Law. We find that in most cases, the application of the WF law with the low temperature value of the Lorenz number does not sufficiently predict the total thermal conductivity. To understand the mechanisms that drive the thermal transport of these metal films, we use infrared variable angle spectroscopic ellipsometry (IR-VASE) the measure the electron scattering rates, demonstrating the relatively thickness independent scattering processes in these films, providing strong promise in the scaling of these metals to technology node length scales.

References

1. Md.R. Islam, et al., Nat. Comm. **15**, 9167 (2024).
2. J.L. Braun, et al., Rev. Sci. Instrum. **90**, 024905 (2019).
3. D.H. Olson, J.L. Braun, P.E. Hopkins, J. Appl. Phys. **126**, 150901 (2019).

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Hybrid and Fusion Bonding to Enable Advanced Packaging

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Direct bonding is emerging as a critical technology for advanced 3D architectures. Fusion bonding plays a pivotal role in enabling CFET and BSPDN structures in logic devices, as well as advanced 3D memory structures [1]. Similarly, hybrid bonding has become indispensable for meeting the stringent requirements of HBM, CIS, and 3D NAND development [2,3]. Despite its growing importance, the mechanisms underlying wafer bonding remain inadequately understood. Achieving ultimate distortion control is critical for precise overlay corrections during lithography. Bond wave behavior, the primary contributor to wafer bonding distortion, remains insufficiently explored. Plasma activation and surface wetting are thought to strongly influence bond wave speed, yet their surface-level interactions are poorly understood [4] (Fig. (a)). Furthermore, the lack of standardized bond strength measurement methods introduces significant variability in results [5] (Fig. (b)). In this paper, we will share our latest findings on the comprehensive study of wafer/die bonding mechanisms. These insights aim to support the evolution of future node 3D architectures.

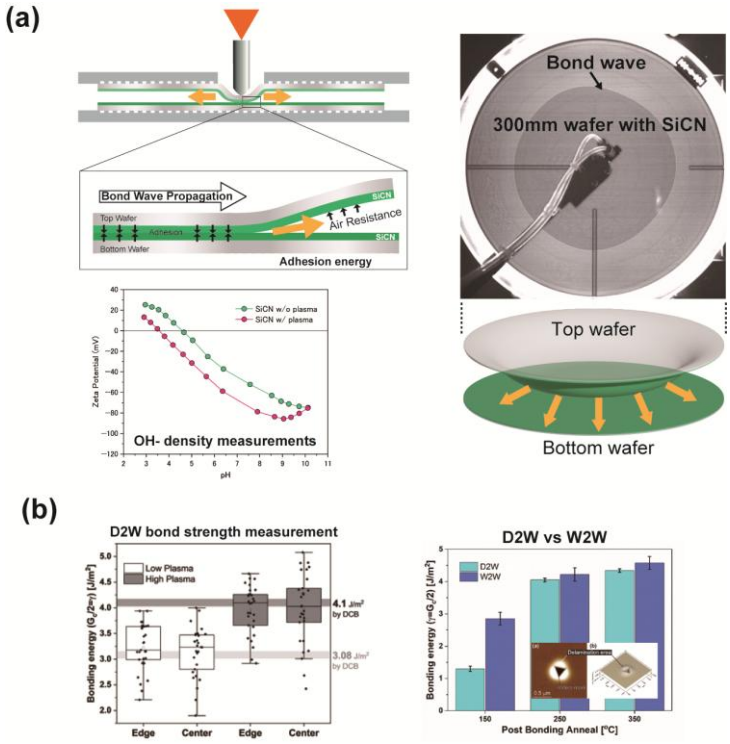

Figure (a) Bond wave analysis for ultimate distortion control in 300 mm wafer with SiCN (b) Bond strength measurements for die level hybrid bonding.

References

1. Yuh-Jier Mii, “Semiconductor Industry Outlook and New Technology Frontiers”, 2024 IEEE International Electron Devices Meeting (IEDM)
2. Y. Kagawa et al., "Novel stacked CMOS image sensor with advanced Cu2Cu hybrid bonding," 2016 IEEE International Electron Devices Meeting (IEDM),
3. M. Tagami, "CMOS Directly Bonded to Array (CBA) Technology for Future 3D Flash Memory," 2023 International Electron Devices Meeting (IEDM)
4. R. Sato et al., “Correlation between Pre-Bonding Surface and Bond Wave Speed” 2024 8th International Workshop on Low Temperature Bonding for 3D Integration (LTB-3D)
5. T. Iwata, et al., “Water stress corrosion at wafer bonding interface during bond strength evaluation.” Materials Science in Semiconductor Processing 184, 108820 (2024)

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Vertically Scaled Gate-All-Around Transistors: From Advanced Nano-Contact Engineering to Device Development

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The continuous scaling of semiconductor devices has pushed conventional architectures to their physical limits, necessitating the development of novel transistor structures. Vertically scaled Gate-All-Around (GAA) transistors have emerged as a promising solution, offering superior electrostatic control, enhanced current drive, and high device density [1][2][3]. However, achieving high-performance and reliable device integration requires advanced engineering of nano-contacts and source/drain (S/D) interfaces [4].

This work presents a comprehensive investigation into the fabrication and optimization of nano-contacts for vertical GAA transistors. We explore the impact of channel nanostructured materials [5][6], contact silicide selection [7][8], and doping strategies on device performance [9], leveraging advanced characterization techniques to analyze dopant segregation [10] and silicidation effects at the nanoscale. Furthermore, we discuss process innovations that enable precise control over vertical channel formation, ensuring optimal electrical properties and minimal parasitic resistance.

By integrating experimental results with simulation insights, we highlight the critical role of nano-contact engineering in the development of high-efficiency, scalable vertical GAA transistors [11][12]. These advancements provide a pathway toward the next generation of ultra-scaled logic devices, enabling further transistor miniaturization while maintaining energy efficiency and performance in modern semiconductor technologies.

References:
1- G. Larrieu et al., Nanoscale 5, 2437 (2013).
2- G. Larrieu et al., Solid-State Electron. 130, 9 (2017).
3- Y. Guerfi and G. Larrieu, Nanoscale Res. Lett. 11, 1 (2016).
4- C. Rossi et al., Solid-State Electron. 200, 108551 (2023).
5- J. Müller et al., Nanotechnology 34, 105303 (2023).
6- A. Lecestre et al., ACS Omega 7, 5836 (2022).
7- J. Müller et al., presented at the EMRS Spring Meeting, 2023.
8- N. Mallet, ACS Appl. Mater. Interfaces 16, 2449 (2024).
9- C. Rossi, Mater. Sci. Semicond. Process. 174, 108217 (2024).
10- P. Michałowski et al., Measurement 211, 112630 (2023).
11- A. Kumar, Nano Lett. 24, 7825 (2024).
12- G. Larrieu et al., proceeding of the 2023 Silicon Nanoelectronics Workshop (SNW), Kyoto, Japan, pp. 27.
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Secondary Ion Mass Spectrometry Measurements of Non-Planar Materials and Devices

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Recent advancements in materials science and device engineering have underscored the critical need for analytical techniques capable of high-resolution chemical characterization of complex, non-planar structures. In this context, the adaptation of secondary Ion Mass Spectrometry (SIMS), renowned for its exceptional sensitivity and elemental specificity, to non-planar materials is of paramount importance. Traditionally optimized for flat surfaces, SIMS is now being redefined to meet the demands of emerging materials such as MXenes, silicon nanowires (NWs), and vertical-cavity surface-emitting lasers (VCSELs) with their three-dimensional architectures.

MXenes, a versatile class of two-dimensional transition metal carbides and nitrides, exhibit intricate compositions with surface terminations that significantly influence their properties. The optimized SIMS measurement procedure, with its layer-by-layer characterization, has proven to be a reliable tool, identifying oxygen in the X-layers.[1] This precision has led to the discovery of the existence of oxycarbide, oxynitride, and oxycarbonitride subfamilies. By implementing advanced deconvolution protocols, SIMS has shown that it can achieve atomic depth resolution and precise quantification of elemental distributions within individual layers.[2]

Similarly, the analysis of NWs—key components in next-generation nanoelectronics—presents challenges due to their high aspect ratio and non-uniform doping. Conventional SIMS fails to resolve dopant distributions along nanowire heights due to a non-uniform sputtering process. However, a novel self-flattening approach, where nanowires are embedded in an organic matrix and analyzed at high incident angles, has revolutionized the field by allowing for accurate depth profiling of dopants, with detection limits as low as 5×10^{16} atoms/cm^3.[3] This approach has significantly improved our ability to understand and optimize the performance of nanowire-based devices.

The complexity of VCSEL structures, comprising hundreds of alternating semiconductor layers with nanoscale quantum wells, further necessitates refined SIMS methodologies. Standard SIMS suffers from matrix effects and depth-resolution degradation, making precise characterization difficult. Recent improvements, including impact energy modulation, optimized extraction parameters, and in-situ ion polishing, have led to artifact-free profiling, capturing the realistic distribution of elements within the device. This enhanced approach enables accurate quantification of dopants and contaminants combined with subnanometer depth resolution needed to analyze quantum wells. Interestingly, the measurements can be performed not only on epi-structures but also on fully processed devices.[4]

These advancements in SIMS methodologies are critical for accurately characterizing non-planar materials and devices. By addressing limitations inherent to conventional SIMS, these innovations pave the way for improved understanding, optimization, and application of complex nanostructured materials with non-planar geometries in electronics, such as advanced semiconductor devices, and photonics, including high-performance lasers and photodetectors, and beyond.

References

1. P.P. Michałowski et al. Nat. Nanotechnol. **17**, 1192 (2022)
2. P.P. Michałowski Nanoscale Horiz. **9**, 1493 (2024)
3. P.P. Michałowski et al. Measurement **211**, 112630 (2023)
4. P.P. Michałowski et al. Measurement **225**, 114003 (2024)

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Thin Films Characterization using Fast Data Acquisition at DiffAbs Beamline (Synchrotron SOLEIL)

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Characterizing the internal (micro)structure and the crystallinity of thin films of nanometric thickness and / or nanostructures is of major importance since a significant part of their properties are tightly related to them. Beyond the film thickness, parameters like the degree of crystallinity and the texture (information on the preferential orientation of crystallites) are meaningful to be addressed and to be quantified, since they (can) have a marked influence on the anisotropic physical properties of materials in general, or thin films (electrical, magnetic and/or mechanical).

Several experimental approaches will be detailed here, making use of the bright x-ray beams available at synchrotrons, the availability of high dynamics low noise fast area detectors, all these coupled with on-the-fly data acquisition. Collecting extended datasets for scattering angles in an angular domain of several 10° can be performed for nm-thick films in times as short as few minutes [1, 2]:

- Film thickness, roughness and density can be inferred from X-ray reflectivity measurements.
- Epitaxial thin films and structures can be characterized in detail by 3D mapping of reciprocal space volumes around Bragg diffraction peaks.
- Texture observation and quantification can be performed by measuring Bragg x-ray diffraction peak(s) intensity as a function of the sample orientation, *i.e.* the so-called pole figures.

The acquired data can also be rapidly converted for visualization and (pre-)analysis, and several 'filtering' procedures can be applied, in order to highlight (during the experimental campaign) the interesting situations for a more detailed investigation (for ex. new crystalline phases, modification or appearing of new / specific textures, …). This optimized experimental approach implemented on DiffAbs beamline (Synchrotron SOLEIL) will be detailed, together with some examples, to illustrate the wealth of information obtained.

Compared to the classical data acquisition schemes, a gain of at least 2 decades in the acquisition time is obtained. The rapidity of the method makes it adapted for systematic studies of a large number of samples, or to build trends by varying one or several characteristic parameters (composition, temperature, actuation, …). Moreover, accessing a broader scattering angle domain, a precise knowledge of the sample crystallinity is not a pre-requisite; studies of new crystalline phases or phase transformation, including the appearing of transitory phases, are thus also feasible. This approach opens thus the path for an in-depth materials characterization, including *in situ* or *operando* studies.

References

1. C. Mocuta *et al.*, J. Appl. Cryst. **46**, 1842 (2013).
2. E. Solano *et al.*, Thin Solid Films **638**, 105 (2017).

[*] *corresponding author e-mail:* mocuta@synchrotron-soleil.fr

Wide Bandgap Device Technology for Power Efficient and High Temperature Applications

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The rapid electrification of our society is in full swing. The need for better energy efficiency is urgent. The progress in the development of emerging new device technologies is very promising. Semiconductor materials with wide bandgap are maturing fast. Both gallium nitride (GaN) and silicon carbide (SiC) devices are today to be found in several commercial applications such as power supplies for computers and charging equipment for handheld units. High power applications are also rolling out for automotive industry and EV charging networks. Yet, much more development is needed and expected. The material quality is far from perfect, but promising. This talk will focus on the current status and projections on high voltage SiC and GaN device technology for the electrical infrastructure and promising high temperature applications. A brief presentation regarding the activities for the EU Chips JU Pilot Line 4 will be included.

Exploring properties and applications of amorphous 2D materials in interconnects using Artificial Intelligence

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Artificial Intelligence-based techniques have become critical to accelerate the innovation processes from material growth to characterization and properties prediction. Particularly challenging is the modelling of disordered (amorphous) materials, complex interfaces and random assemblies of (2D) materials which are mainly used today in applications.

In that perspective, complex forms of (reduced) graphene oxides and related composites as well as amorphous materials such as boron nitride (aBN) and “amorphous graphene” (aG) have recently become prominent materials for many different applications, notably due to their good properties such as thermal stability, mechanical properties, insulating behaviour, and ultralow dielectric constant in aBN (<2) which present appealing properties for developing next generation of interconnects. Moreover, amorphous films are more suitable to large area deposition compared to clean hBN or graphene since they can be grown at low temperatures (about 400 ºC) and on various substrates [1-3]. However, their properties strongly depend on the nature and degree of disorder, which needs a well-defined metrics for benchmarking different materials. Having such metrics in place will allow to tune the properties and performance of these films during the fabrication for desired applications. In this context, revealing the relationship between fabrication strategies and the material properties of the film is also crucial.

Capturing the key features of the amorphous nature of materials requires theoretical characterization to understand how material properties change with the microstructure. Since simulations of amorphous materials need large structural models, density functional theory (DFT) is not a suitable tool despite the high accuracy it offers. On the other hand, molecular dynamics (MD) simulations with empirical interatomic potentials require much less computational cost; however, they can turn out to be not accurate enough to correctly describe the local environment of amorphous materials. Machine learning-driven interatomic potentials (ML-IP) can describe the local environment with a similar accuracy to DFT and at a much lower cost [4,5]. Here, we introduce Gaussian approximation potentials (GAP) for atomistic simulations of aBN incorporating different contaminators and doping materials, which are trained on a large dataset of atomic structures generated by DFT calculations [6-8]. We will present a systematic analysis to screen out possible realistic morphologies as a function of growth parameters, such as temperature, quenching rate, and the presence of a dopant, and their corresponding material properties using GAP-driven MD simulations. The extensive simulations of a large quantity of possible structures presented here can guide experimental research and provide trends of scaling behaviour as a function of experimentally controllable parameters. The impact of amorphousness on dielectric properties will be also discussed for aBN and aG in the light of recent breakthroughs and claims [9,10].

We also present AI-driven computational workflows that could revolutionize advanced materials design and engineering, in which the automated building of structural and electronic models and their implementation into our in-house linear scaling computational algorithms (www.lsquant.org) enables the simulation of electronic, optical, transport properties in disordered models of materials containing up to the trillion atoms scale while keeping the accuracy of ab-initio approaches. These workflows will be designed to boost the innovation in a variety of technologies and applications in concertation and partnerships with industries.

References

1. Hong, S et al. Nature 582, 511–514 (2020).
2. Glavin, N. R., et al., Adv. Func. Mat. (2016).
3. Chen, C. Y., et al., arxiv: 2312.09136 (cond-mat).
4. Unruh D. et al. Physical Review Materials 6, 065603 (2022).
5. Deringer, VL. and Csányi, G. Physical Review B 95, 094203 (2017).

6. Kaya, O., et al. Nanoscale Horizons 8, 361–367 (2023).
7. Kaya, O. et al. J. Phys. Materials 7, 025010 (2024).
8. Kaya, O. et al. arXiv:2402.01251 (cond-mat).
9. Th. Galvani et al. Journal of Physics: Materials 7 (3), 035003 (2024); arXiv:2403.11924 (cond-mat).
10. Th. Galvani, O. Kaya, S. Roche, unpublished
* *corresponding author e-mail:* stephan.roche@icn2.cat

Enabling III-V and CMOS Synergy: Advances in Contact Technology

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III-V semiconductors have become central to the advancement of microelectronics, offering a unique combination of electronic and optical properties that enable a wide range of applications. In both microelectronics and optoelectronics, contacts play a critical role in III-V semiconductor devices, acting as the primary electrical interface between the device and external circuitry.

Traditionally based on noble metals, gold-free metallization schemes, which are critical for CMOS compatibility, have shown considerable promise, with materials such as titanium and nickel being explored for their potential to form ohmic contacts without introducing gold-related contamination risks into CMOS fabrication lines [1-7].

In this paper, we will review the last 10 years of efforts to develop Si CMOS compatible contact technology on III-V materials at CEA-Leti. After a brief overview of our group's contributions, we will focus on 2 examples of recent studies in 300 mm [8,9].

References

1. S. Jain et al., *Appl. Phys. Lett.* **100**, 201103 (2012)
2. H. Hahn et al., *J. Phys. D : Appl. Phys.* **50**, 235102 (2017)
3. E. Ghegin et al., *Microelectron. Eng.* **156**, 86 (2016)
4. S. Zhiou et al., *J. Appl. Phys.* **120**, 135304 (2016)
5. E. Ghegin et al., *J. Appl. Phys.* **121**, 245311 (2017)
6. S. Bensalem et al., *Mater. Sci. Semicond. Process.* **113**, 105038 (2020)
7. Ph. Rodriguez et al., *Jpn. J. Appl. Phys.* **59**, SL0801 (2020)
8. F. Boyer et al., *IEEE J. Electron Devices Soc.* **10**, 728-736 (2022)
9. E. Moulé et al., *Mater. Sci. Semicond. Process.* **189**, 109257 (2025)

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Assessment of environmental footprint of semiconductor manufacturing industry to promote more sustainable processes

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The European green deal aims to ensure net-zero emissions by 2050, making Europe the first climate-neutral continent in the world, as well as a target of 55% less emissions by 2030, in comparison to 1990 [1]. Global digital market is growing by 6% a year and semiconductor industry growth is forecast at 45% in 2030. The IC industry commits to a decarbonisation plan to reduce its greenhouse gases emissions, preserve energy, water and other resources. The Life Cycle Assessment (LCA) in this context plays a crucial role in helping to identify the main environmental impacts and known as "hotspots", allowing giving recommendations to mitigate the environmental footprint of chips manufacturing in clean rooms [2].

Building upon international ISO standards (e.g. ISO 14040/44), the Product Environmental Footprint (PEF) method, recommended by the European Commission [2], based on LCA provides the principles, framework and guidelines to quantify environmental impacts throughout the entire life cycle of products (Fig.1). For LCA studies, we use SimaPro® software, an ISO-compliant LCAs tool, coupled with the Ecoinvent v3.10 database.

We will present different LCA studies conducted at CEA-Leti on the chips manufacturing on Silicon wafers. The environmental impacts assessment includes both the infrastructure to maintain ultra-clean environments [3] (Fig.2), and the process steps required for manufacturing [4-6] of different technologies [7]. The major contributors in clean rooms are energy use (electricity, natural gas), resource consumption (e.g., water, chemicals, acids, metals…), emissions in air (e.g., CO_2, PFCs), and waste treatments of effluents.

Finally, we will illustrate eco-design solutions for both facilities and processes in clean rooms such as: Improving energy efficiency, reducing water consumption (reuse/recycling), replacing PFCs gas with lower global Warming Potential (GWP) gas, substituting materials containing harmful compounds (PFAS, CMR, etc.), promoting the circularity of critical materials and developing efficient waste treatment.

References

1. https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/european-green-deal_fr
2. https://green-business.ec.europa.eu/environmental-footprint-methods/pef-method_en
3. J. Lopes Barbosa J. *et al.*, J. Clean. Prod., accepted (2024)
4. I. Servin et al. "Chitosan as a water-based photoresist for DUV lithography" Proc. SPIE 12498, (2023)
5. M. Renaud et al. Proc. SPIE 12958 (2024)
6. I. Servin et al., "Life Cycle Assessment of semiconductor manufacturing: Focus on steps using chemicals" LCIC conference (2024)
7. L. Vauche L. et al., Sustainability, **15**, (2023)

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Fig. 1 Life cycle and 4 main phases of a PEF study

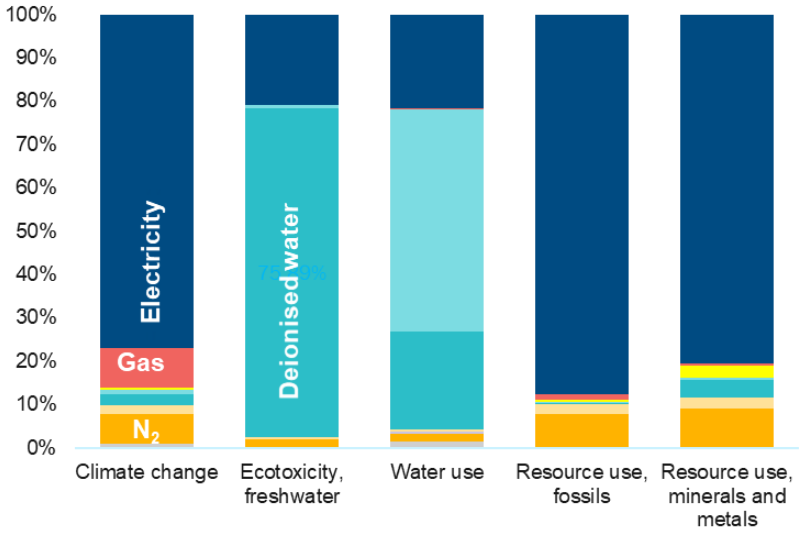

Fig. 2 LCA of infrastructure within CEA-Leti cleans rooms [3]

Enabling Ultra Low Temperature Hybrid Bonding for D2W Scaling

Veronica Strong et. al.

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Abstract:

Hybrid bonding is the next generation 3D integration technology that offers opportunities for extremely high interconnect densities (up to 1M IOs/mm^2 or more, [1]), significantly lower interconnect power [2] as well as improved thermal and power delivery performance [3, 4]. This can offer significant improvements in system performance and energy efficiency, especially for current and future AI and datacenter workloads. However, hybrid bonding offers several new challenges on cleanliness, dielectric and metal pad topography [5]. Additionally, several hybrid bonding schemes requires relatively high anneal temperatures to ensure good metal to metal bonding which can limit the capability of integrating temperature sensitive devices and potential mechanical impacts for complex die structures or larger chiplet sizes. To address these issues, we developed ultra-low temperature hybrid bonding (ULT-HB) technology targeting bonding temperatures <=200C. Several groups have been investigating copper grain engineering; as materials like nT-Cu and fine grain Cu has demonstrated higher expansion at lower temperatures (which can help reduce the CMP requirements), improved diffusivity, and are promising candidates for ultra-low temperature hybrid bonding [6-9]. Yet, engineered crystalline Cu is only part of the equation, for this technology to be fully viable within ultra-low temperature hybrid bonding all parts of the HB process need to be investigated, including surrounding dielectrics. In this talk, we will present on wafer-to-wafer and die-to-wafer compatible hybrid bonding using fine grain Cu. We will show wafer to wafer bonding results for 3 µm pitch at temperatures between 150 - 250 ^{o}C. Comparisons between types of Cu grain engineering vs. Std Cu, CMP slurry impact, pad recess impact, Cu grain stability, and discussion of current limitations and key drivers are shown.

Citations:

1. T. Talukdar *et al.*, "Process Development and Performance Benefits of 0.64-0.36 µm Pitch Hybrid Bonding on Intel Process," *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*, Denver, CO, USA, 2024, pp. 784-789, doi: 10.1109/ECTC51529.2024.0012

2. A. Elsherbini, S. Liff, J. Swan, K. Jun, S. Tiagaraj and G. Pasdast, "Hybrid Bonding Interconnect for Advanced Heterogeneously Integrated Processors," *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2021, pp. 1014-1019, doi: 10.1109/ECTC32696.2021.00166.

3. Oprins *et al.*, "Thermal characterization of the inter-die thermal resistance of hybrid Cu/dielectric wafer-to-wafer bonding," *2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, Las Vegas, NV, USA, 2016, pp. 1333-1339, doi: 10.1109/ITHERM.2016.7517703.

4. H. Oprins *et al.*, "3D Wafer-to-Wafer Bonding Thermal Resistance Comparison: Hybrid Cu/dielectric Bonding versus Dielectric via-last Bonding," *2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, Orlando, FL, USA, 2020, pp. 219-228, doi: 10.1109/ITherm45881.2020.9190392

5. A. Elsherbini *et al.*, "Enabling Hybrid Bonding on Intel Process," *2021 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp. 34.3.1-34.3.4, doi: 10.1109/IEDM19574.2021.9720586.

6. Gao, G.; Mirkarimi, L.; Workman, T.; Fountain, G.; Theil, J.; Guevara, G.; Liu, P.; Lee, B.; Mrozek, P.; Huynh, M. "Low temperature Cu Interconnect with Chip to Wafer Hybrid Bonding" *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019, pp. 628-635.

7. J.J. Ong, *et al.* Materials 2022, 1(5)5, 1888.

8. M. F. Chen *et al.*, "SoIC for Low-Temperature, Multi-Layer 3D Memory Integration," *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2020, pp. 855-860, doi: 10.1109/ECTC32862.2020.00139.

9. Qiushi Kang, Chenxi Wang, Shicheng Zhou, Ge Li, Tian Lu, Yanhong Tian, and Peng He *ACS Applied Materials & Interfaces* 2021 *13* (32), 38866-38876

Graphene Capping for Advanced Interconnects

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Graphene capping is attracting attention as a technology that can lead to lower resistance and higher reliability of copper, ruthenium, and other advanced nano-interconnects. I will review the history of graphene capping and discuss on the issues and recent trends. I will also introduce our study of graphene capping to advanced interconnect materials such as NiAl..

Multi-scale correlative investigations of failure mechanisms in two-dimensional crystalline polymers

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Two-dimensional (2D) polymer thin films hold great potential for advancing microelectronics and flexible electronics [1]. However, their integration into nanodevices remains challenging due to unresolved issues related to mechanical integrity, as the damage and failure mechanisms of 2D polymers are not yet well understood [2]. This study systematically investigates an interfacial-synthesized 2D crystalline polymer (2D polyimine) [3] to elucidate its failure mechanisms under different damage processes.

To evaluate patterning-induced failures, focused electron beam (FEB), focused ion beam (FIB), and mechanical patterning techniques were examined [4]. Based on this evaluation, a beam-free transfer and patterning method was developed, enabling *in-situ* tensile testing in a transmission electron microscope (TEM, Libra200, Carl Zeiss). The complete failure process of 2D polyimine films under in-plane mechanical stress was captured in real time, revealing unique fracture dynamics and crack propagation behaviors. Additionally, distinct fracture modes across different grain orientations underscore a crystallography-driven fracture mechanism, further supported by atomistic insights from Density-Functional Tight-Binding (DFTB) simulations [5].

These findings enhance the fundamental understanding of structure-property relationships in 2D polymers, providing valuable guidelines for designing novel 2D polymers with tailored mechanical reliability and optimizing patterning strategies for device integration.

References

1. J. I. Feldblyum *et al*., *Chem commun.* **51**, 13894 (2015)
2. H. Qi *et al*., *Sci. Adv.* **6**, eabb5976 (2020)
3. R. Dong *et al*., *Chem Rev*. **118**, 3189 (2018)
4. B. Zhang *et al*., *Nanotechnology*. **35**, 47530 (2024)
5. B. Zhang *et al*. *Adv. Sci.* **11**, 2407017 (2024)

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Selective and Self-Limited Process Technologies to Enable Ångstrom Scale Integrated Circuits

Speaker: Robert D. Clark

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Continued device density scaling according to Moore's Law has resulted in the adoption of 3D devices and architectures while driving critical dimensions down to atomic scales. This tutorial briefly reviews the trends in device scaling and outlines the forces driving 3D integration going forward as well as the new challenges these changes pose for future manufacturing process technologies. A look forward at the expected evolution of integrated circuit manufacturing through 3D monolithic and heterogeneous integration is presented to frame the opportunities and challenges for advanced process technologies. Selective, self-limited and atomic scale thin film process technologies that can enable 3 nm and beyond semiconductor manufacturing include plasma and thermal chemical vapor deposition (CVD), atomic layer deposition (ALD) and atomic layer etching (ALE) technologies. Selective processing including topographic and area selective deposition (ASD) is explained as an emerging technology enabling new device nodes, integration schemes and eventually the shift toward new patterning paradigms. The scope of the discussion includes examples of how these technologies enable self-aligned and sub-lithographic patterning and integration of new devices, interconnect structures and scaling boosters suitable for angstrom level process nodes. The major trends that will drive thin film innovation in semiconductor manufacturing over the next decade and beyond will also be summarized and explained.

The Metallization Routing to Two Trillion Dollars

Anand Murphy

[a] *LAM, USA*

Advancements in metallization and interconnect technology are crucial for enhancing performance, power efficiency, and scaling in modern semiconductor devices. This talk, from the perspective of a wafer processing equipment supplier, will delve into the evolution of materials and processes that enable next-generation interconnects. It will cover shifts to metals like cobalt, ruthenium, and molybdenum, as well as changes in integration and packaging with backside power and subtractive metallization. The discussion will also include advancements in metal deposition techniques such as area-selective deposition (ASD), new electrochemical processes, and pulsed laser deposition (PLD), addressing challenges in resistance-capacitance scaling, reliability, and specialty applications. Additionally, cost-effective pitch scaling through the transition from wet to dry resist processes will be described. By bridging material science and equipment engineering, this talk will highlight the importance of collaboration across the semiconductor ecosystem to achieve the performance, manufacturability, and sustainability required for future advanced nodes

Understanding and predicting interconnect metal deposition and morphology from atomic scale simulations

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Optimising the deposition process and morphology of interconnect metals is essential to successful metallisation processes. Atomic scale simulations provide a powerful tool to understand the underlying mechanisms of metal deposition and growth processes, as well as the dependence of their morphology on the substrate. We have developed a screening approach based on multiscale first principles simulations to predict the morphology of a metal on a given substrate. This way, promising material candidates can be pre-selected, thus reducing the time and cost of experimental development.

Growth of advanced metal interconnects is particularly impacted by the issue of metal morphology. At small scales, *ca* < 10 nm, copper preferentially forms non-conducting islands, leading to defects and poor quality of the deposited metal. To prevent this, a liner material that promotes 2D Cu morphology is deposited onto the diffusion barrier, which itself prevents migration of Cu into the surrounding dielectric. However, the lowest, and smallest, levels of interconnects have extremely high aspect ratios and the diffusion barrier and liner bilayer takes up too much volume to allow depositing sufficient Cu.

To tackle this significant technology bottleneck, we use density functional theory (DFT), ab initio molecular dynamics and kinetic Monte Carlo to investigate the morphology of copper and other possible interconnect metals on TaN, the state of the art diffusion barrier.

In particular, the competition between the metal-substrate and metal-metal interaction tends to be the key to controlling the final morphology [1], see Fig. 1. These interaction energies change based on the substrate and metal combination. By altering the properties of TaN through doping and defects we can optimize these interaction energies to drive 2D, horizontal growth of the interconnect metal.

With this methodology, we have developed promising TaN-based materials to promote deposition of high quality interconnects made from Cu for the higher metallization levels and Co and Ru for the lowest and smallest interconnect levels. Our kinetic Monte Carlo approach provides further insight into the metal deposition process for these materials, providing quantitative information on the depositedmetal, and highlighting the effect of substrate, deposition temperature and annealing on the film morphology and quality [2].

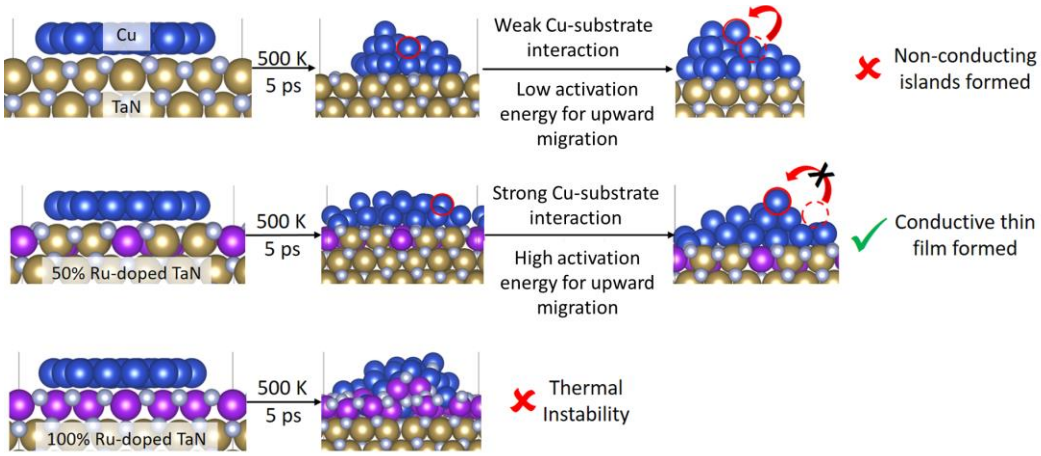

Figure 1: Examples of Cu morphologies on different TaN substrates. Cu = blue, Ru = purple, Ta = gold, N = silver

References:

1. C.-L. Nies, S. K. Natarajan and M. Nolan, Chem. Sci. **13**, 713-725 (2022).
2. S. D. Aldana, C.-L. Nies and M. Nolan, arXiv, (2024) https://doi.org/10.48550/arXiv.2410.06133

In situ study of the synthesis of lamellar metal chalcogenides by alternating deposition of organic & inorganic molecules

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Lamellar Metal Dichalcogenides have emerged as a class of exceptional materials which exhibits remarkable electronic and chemical properties on the scale of a few monolayers. In the quest for large-scale deposition methods for the fabrication of ultra-thin films of textured lamellar metal chalcogenides on amorphous substrate, we have adopted a synthesis strategy based on the alternating deposition of a metal precursor molecule with an organic precursor molecule followed by a specific annealing and applied it to the preparation of titanium disulfide (TiS2) [1-3]. The fine control of the whole synthesis process could be achieved by in situ synchrotron and ellipsometry studies during the 2-step process (Fig. 1a,b) using a custom-built portable reactor which mounts onto the 6-axis tower of the NewportTM diffractometer installed at the beamline SIRIUS (Fig. 1c), a thorough ex situ structural and chemical characterizations, and chemical experimental modeling on high surface area silica beads. Deeper understanding of the bonding mechanism at the early stage of growth could be obtained by quantitative analysis of x-ray absorption spectra recorded in situ during the growth at both the Ti and S K-edges, exploiting the results from density functional theory calculations [4].

This work was financed by the ANR project ANR-18-CE09-0031 and Labex MINOS

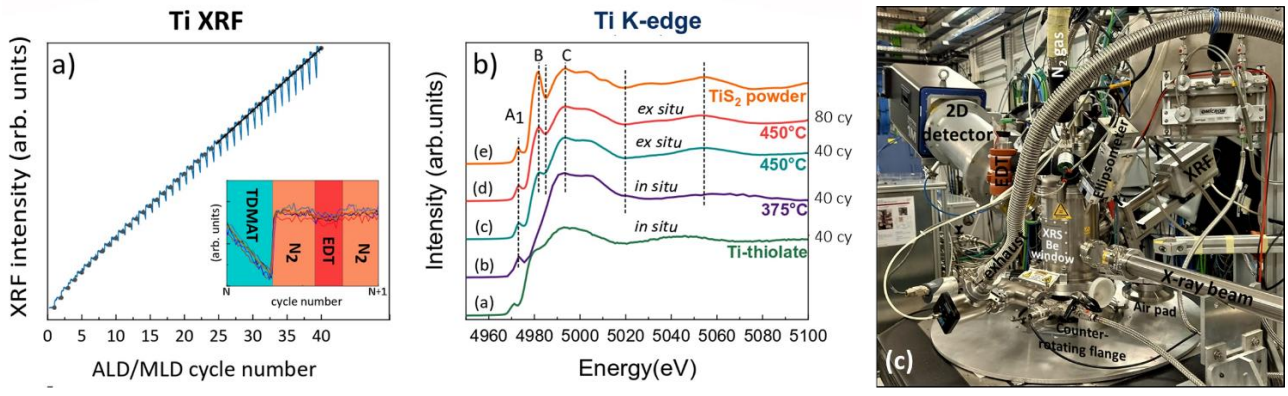

Fig. 1 (a) Chemical vapor deposition (hybrid Atomic Layer Deposition/Molecular Layer Deposition) reactor built for surface-sensitive in situ synchrotron studies, installed at synchrotron SOLEIL (Saint Aubin, France), (b) Ti x-ray fluorescence emission intensity and (c) Ti K-edge x-ray absorption spectra

References

1. 1. P. Abi Younes et al., Chem. Mater. 34, 10885c(2022).
2. 2. P. Abi Younes et al., J. Vac. Sci. Technol. A 41, 042403 (2023).
3. 3. In situ X-ray study of the synthesis of TiS2 prepared by an Atomic/Molecular Layer Deposition route. Sustainable energy, SOLEIL Highlights (2022), p98.
4. 4. A-K Yadav et al., Nanoscale 16, 1853 (2024).

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ALD and AS-ALD of Metallic Films with New Precursors and Approaches

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Metal ALD is a topic where high industrial importance and inspiring and challenging scientific questions meet. As always, the success of ALD builds on chemistry. There is constant need for new precursors to enable ALD of metals of interest with improved characteristics. Major challenge arises from the strong tendency of metals to agglomerate, hence making it difficult to achieve continuous films at the smallest thicknesses. Lowering of the deposition temperature is of utmost importance to tackle this issue. This requires highly volatile and reactive metal precursors and reducing agents. Overall, the lack of an efficient universal reducing agent is a major challenge for metal ALD. In this presentation examples will be shown from our recent work on both metal precursors and reducing agents, including also reaction mechanism studies on selected processes.

Sustainability is one more parameter to be taken into account when developing new ALD precursors. This is however challenging considering all the other requirements and limitations there are for the ALD precursors. Metal chlorides are controversary precursors that are often avoided because they and the resulting byproducts can be corrosive, yet metal chlorides are thermally stable, reactive, inexpensive and probably the greenest precursor compounds because of the small number of synthesis steps involved. Many metal chlorides are nonvolatile but here it will be shown that these can be converted volatile by adding proper neutral adduct ligands. One of the metal chloride adducts, $PdCl_2(PEt_3)_2$, was found to be fully recyclable: unused molecules can be condensed and collected from the exhaust tube of the reactor by dissolving into acetone, purified by recrystallization, and reused for ALD of Pd and Pd_2Ge [1].

Area-selective ALD (AS-ALD) of metals, and also other materials, is an important topic for self-aligned thin-film patterning. Ideally, the selectivity should be inherent with no need for passivation or activation of the surfaces. Here noble metal processes using metal β-diketonates and O_2 will be shown to have excellent inherent selectivity (Fig. 1) [2].

As an entirely new approach to self-aligned thin-film patterning area-selective etching of polymers will be presented (Fig. 1) [3, 4]. In these etching processes the selectivity arises from the materials underneath the polymer layer. Both O_2 and H_2 can be used as an etchant gas. The etching gas molecules diffuse through the polymer film, and upon reaching a catalytic surface underneath, they dissociate into the respective atoms which then react with the polymer etching it away. On noncatalytic surfaces the polymer film remains. When combined with AS-ALD, self-aligned etching of polymers opens new avenues for the fabrication of semiconductor devices. Fig. 2 shows an example where area-selective etching of polyimide from Pt is followed by area-selective ALD of iridium using the patterned polymer as a growth-inhibiting layer on SiO_2, eventually resulting in dual side-by-side self-aligned formation of metal-on-metal and insulator(polymer)-on-insulator.

References

1. A. Vihervaara, T. Hatanpää, M.-I. Selänne, K. Mizohata, M. Ritala, *Adv. Mater. Interfaces*, 2400579 (2024).
2. C. Zhang, E. Tois, M. Leskelä and M. Ritala, *Chem. Mater*. 34, 8379 (2022).
3. C. Zhang, M. Leskelä and M. Ritala, *Coatings* 11, 1124 (2021).
4. V. Lasonen, A. Vihervaara, G. Popov, E. Tois, L. Mester, M. Karimi, Y. Ilarionova, R. J. Jam, J. Sundqvist and M. Ritala, *Chem. Mater.* 35, 6097 (2023).

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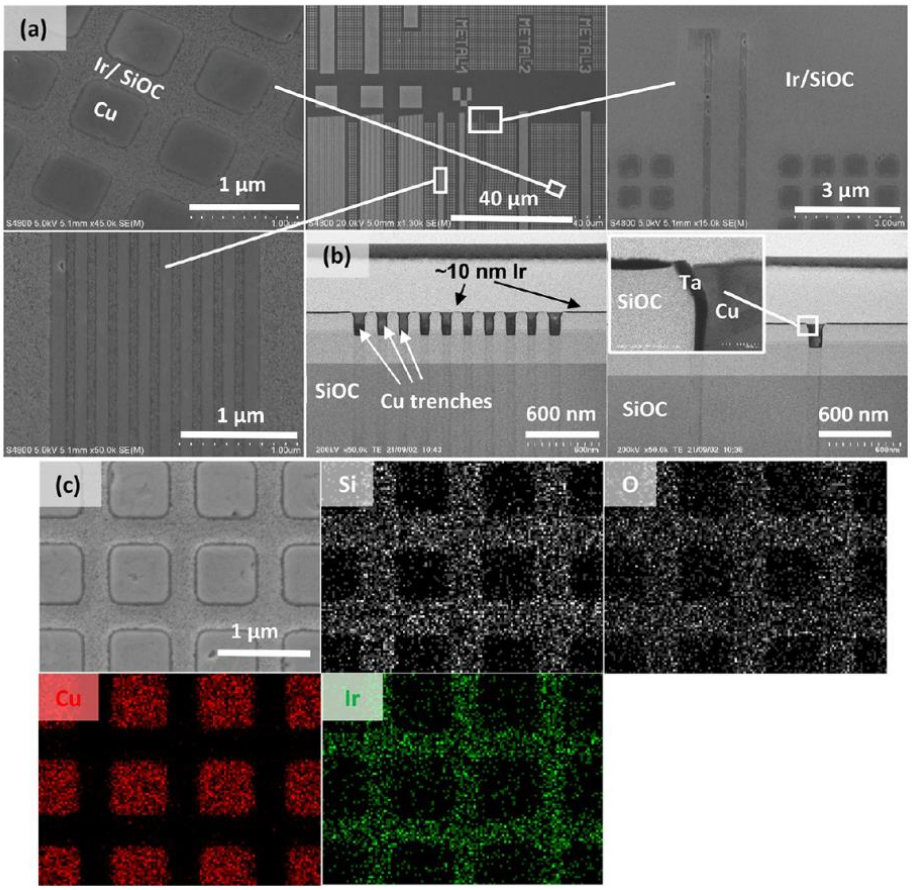

Figure 1. (a) SEM and (b) TEM images showing the selective growth of Ir on UV irradiated test chip at 225 °C for 1000 cycles. (c) EDS maps show the distributions of Si, O, Cu, and Ir elements [2].

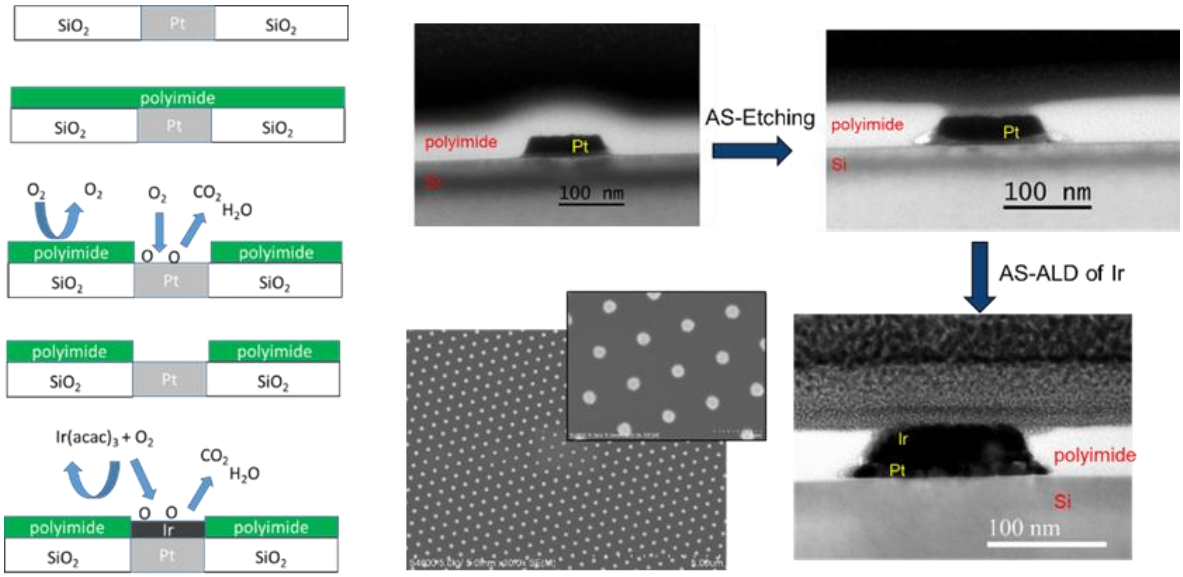

Figure 2. Principle of area-selective etching followed by AS-ALD (left), and cross-sectional SEM images before and after area-selective etching of polyimide from Pt and after AS-ALD of Ir (right).

Next Generation Microelectronics Devices Enabled by Atomic Layer Deposition

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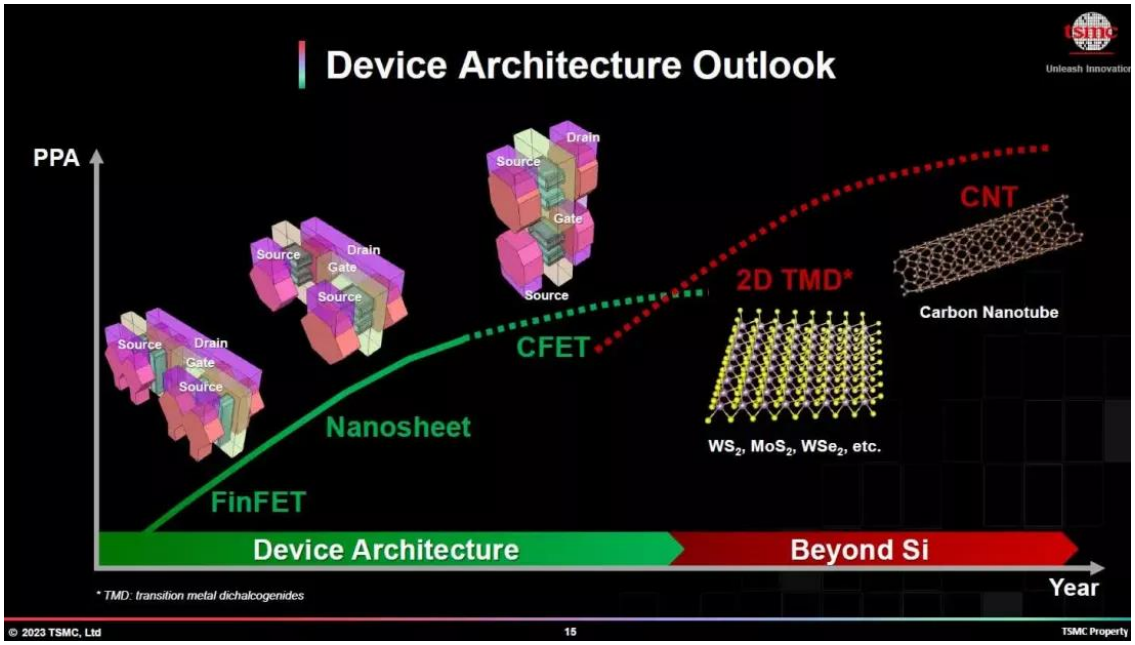
The semiconductor industry has enjoyed unprecedented growth over the last two decades fueled by the PC/internet era (2000s) and the Mobile/Social Media era (2010s). We are now entering the Artificial Intelligence/Big Data era which is predicted to reach $1T by the early 2030s. AI applications require huge amounts of computational power and power consumption. To keep up with computational demands and ensure that the industry does not surpass the global power supply, device makers are looking at ways to increase compute and while driving lower power consumption. Chip manufacturers are leveraging key device architecture inflections to secure leadership positions in the AI competition. Inflections such as those in high-performance logic (gate-all-around transistors, backside power delivery), compute memory (3D-DRAM, vertical transistor DRAM) and advanced packaging (high-bandwidth memory and heterogeneous integration) are blazing the trail. The image below shows TSMC's device roadmap (Source TSMC). After nanosheet (TSMC's flavor of gate-all-around transistors entering production today), TSMC will enter the 3D regime with transistor stacking. 3D integration of devices is a common theme across the industry from logic to memory. Stacking the devices is shown to increase performance, decrease area cost, and decrease power consumption. Realization of these complex architectures requires very stringent fabrication steps with various patterning techniques. Atomic Layer Deposition is a key enabler to fabricating next generation devices. Applications such as conformal deposition, gap fill, extreme thin film deposition (<10A), and area selective deposition are all in play as we move to next generation devices. Applied Materials is a key leader in materials innovation for the microelectronics industry, and as such are putting huge efforts into creating solutions for the device manufacturers. This talk will focus on how Applied Materials is leading the industry in solving these extremely difficult problems and give insight into what is still needed as we move forward



From stamp to wafer - How complex ALD processes become exponentially harder to control on fab-friendly scale

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Electronic devices utilizing different order parameters for new switching mechanisms is important in the transition to neuromorphics and the ultra-low power paradigm. Leveraging these order parameters very often require materials with tunable functionality, typically found in complex materials systems with at least two metal cations. Examples are ferroelectricity in $BaTiO_3$ and $(Hf,Zr)O_2$, ferromagnetism in $(Ca,La)MnO_{3-\delta}$ and $(Co,Ni)Fe_2O_4$ or multiferroicity in $BiFeO_3$.

While the possibilities offered by such materials are well-known on the lab scale due to facile preparation by *e.g.* molecular beam epitaxy or pulsed laser deposition, it is difficult to harness the possibilities at larger scale due to the limitations (area, temperature, pressure) of said techniques.

Integration of complex materials needs to take place utilizing fab-friendly techniques. One possibility is ALD, which is already in widespread use due to the low thermal budget, the large area conformality and the high repeatability. Unfortunately, not all of these advantages are (necessarily) carried over from simple binary systems (like HfO_2) over to the more complex materials.

In this talk, I will present some of the challenges going from simple binary processes over to the more complex materials with ALD. I will spend time on discussing how these challenges can be overcome, and how I propose that ALD is utilized beyond the classic binary oxides and nitrides as we move to completely new device types.

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Time for ALD Metals: Enabling the next generation of leading-edge devices

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ALD, a unique deposition technique, is attracting more and more interest in the industry. With the characteristics of precise thickness control, extremely high conformality, low temperature, ALD plays an important role in the current technology and will become more crucial for the next leading edge devices. Several ALD key innovations will be discussed. With these innovations, ALD metals could enable the future scaling of microchip technology.

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Ru epitaxy on differently oriented sapphire substrates for advanced interconnect applications

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Ruthenium is emerging as a promising alternative to Cu for advanced interconnects in future semiconductor technology. The traditional use of Cu in interconnects has faced significant challenges as device dimensions continue to shrink. These challenges include increased resistivity at smaller line widths due to surface and grain boundary scattering, and degraded electromigration performance, which collectively impact the reliability and performance of Cu-based metallization [1,2].

Ru offers several advantages over Cu, leading to lower line resistances. Ru can provide similar or lower resistivity at reduced dimensions, due to its shorter mean free path compared to Cu. Moreover, Ru's ability to maintain reliability without the need for diffusion barriers and adhesion liners allows for a larger metallization volume, further reducing line resistance [1,2].

Recent studies have shown that epitaxial single-crystal Ru films can exhibit low resistivity, close to the bulk resistivity, even at thin film thicknesses [3,4]. The measured resistivities indicate that single-crystal Ru can outperform polycrystalline films considerably, leading to increased interest in such films for future interconnect technologies. Moreover, Ru is an anisotropic conductor with low resistivity along the hexagonal [0001] axis. Aligning interconnect lines along this axis could lead to a significant further reduction in line resistance. Therefore, epitaxial growth is essential to harness these benefits and improve the performance of Ru interconnects in advanced semiconductor technologies.

Here, we study the epitaxy of Ru by physical vapor deposition on sapphire substrates with c-, a-, r, and m-plane orientations at a deposition temperature of 400°C. Epitaxy on c-plane sapphire leads to hexagon-on-hexagon orientation (Figs. 1 and 2) and ultralow resistivities, close to the Ru bulk resistivity perpendicular to the [0001] axis (7.4 μΩcm) or films thicker than about 30 nm (Fig. 3). X-ray diffraction indicates high crystal quality with a (002) rocking curve half width of 0.48°, consistent with a low Rutherford ion channeling yield of 5% (Fig. 4). The resistivity scaling is consistent with an *ab initio* model including surface scattering only (Fig. 3) [5], confirming that the impact of grain boundary scattering is minimized in epitaxial films.

By contrast, deposition on a-, r-, and m-plane sapphire leads to multiple epitaxial orientations, without clear signs for polycrystalline or minority phases. Ru on a-plane sapphire shows mainly (0001) our of plane orientation with some polycrystalline minority phase present (not shown). Epitaxy on m-plane sapphire leads to a both (0001) and (11-20) out of plane orientations (Fig. 5). Note that both orientations are epitaxial, as revealed by pole figures (not shown). By contrast, epitaxy on r-plane sapphire leads to a tilted twin structure with a {01-11} twinning plane, as revealed by TEM (Fig. 6). Surface faceting is also observed in this case. Due to the multiorientation microstructure and the resulting domain boundaries, the resistivities of epitaxial Ru on a-, m-, and r-plane sapphire is however higher than that of Ru on c-plane sapphire, reaching around 9 to 10 μΩcm for films above 30 nm. Future work is thus needed to understand the epitaxy on such substrates to enable Ru with the low-resistivity [0001] axis in-plane.

We finally comment on the prospects of integrating epitaxial Ru films in advanced interconnects of future CMOS technology nodes.

References:

1. D. Gall, J. Appl. Phys. **127**, 050901 (2020).
2. J.-P. Soulié *et al.*, J. Appl. Phys. **136**, 171101 (2024).
3. K. Barmak *et al.*, J. Vac. Sci. Technol. A **38**, 033406 (2020).
4. R. J. Mehta *et al.*, 2024 IEEE Intern. Interconnect Technol. Conf.(IITC), pp. 1-3 (2024).
5. B. Van Troeye *et al.*, Phys. Rev. B **108**, 125117 (2023)

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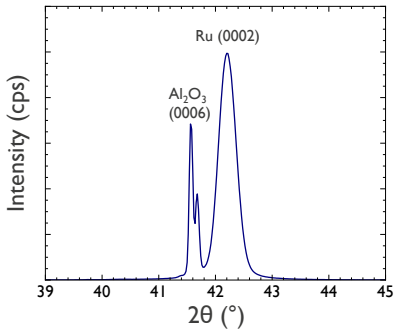

Figure 1: 2θ-ω XRD pattern of a 50 nm thick Ru film deposited on c-plane sapphire

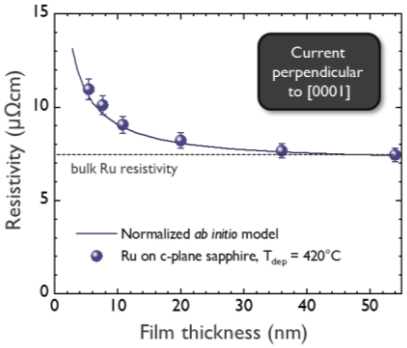

Figure 3: Resistivity vs. thickness of epitaxial Ru on c-plane sapphire.

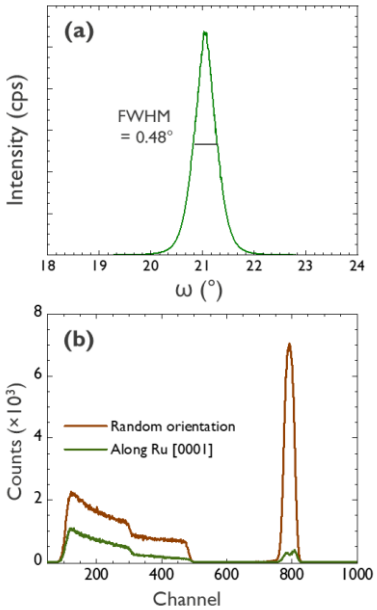

Figure 4: (a) XRD rocking curve and (b) Rutherford ion channeling of a 50 nm thick Ru film deposited on c-plane sapphire.

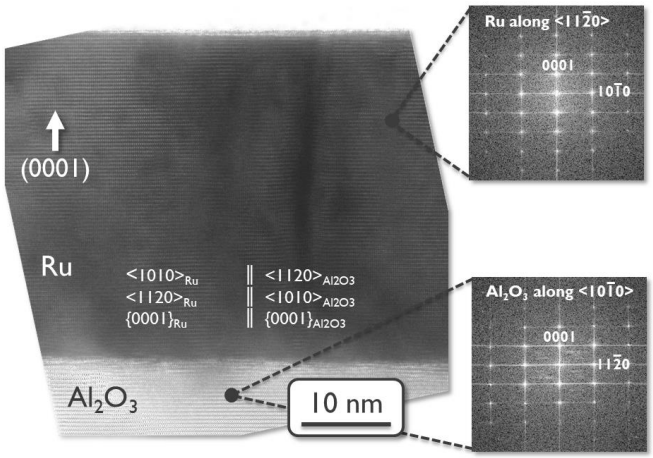

Figure 2: TEM image and corresponding Fourier transforms of a Ru film deposited on c-plane sapphire.

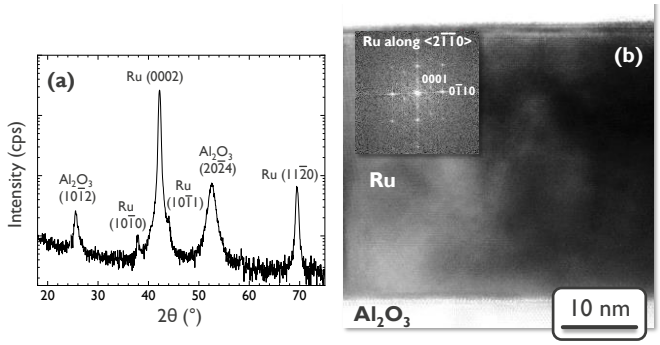

Figure 5: (a) 2θ-ω XRD pattern as well as (b) TEM image and corresponding Fourier transforms of a Ru film deposited on m-plane sapphire.

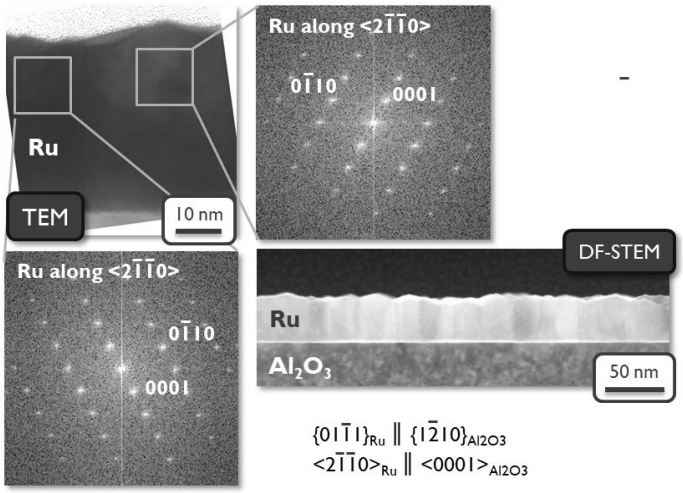

Figure 6: TEM images and corresponding Fourier transforms of a Ru film deposited on r-plane sapphire.

Inherent Area-Selective Deposition of Low-resistivity Molybdenum Carbide Films by Thermal Atomic Layer Deposition

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With the ongoing downscaling of logic and memory devices, one of the main challenges has emerged such as edge placement error issues resulting from top-down patterning. To overcome the limitations of lithography, a recent focus in bottom-up patterning is based on area-selective atomic layer deposition (AS-ALD) [1,2]. Numerous studies have investigated AS-ALD that employed precursor inhibitors such as SAMs or SMIs to prevent precursor adsorption in non-growth areas. However, there is an increasing need for research into inherent AS-ALD strategies, which exploit the intrinsic properties of substrates with the chemical adsorption of the precursor to enable selective adsorption at targeted surface sites. Molybdenum carbide (MoC_x) has attracted as promising materials for metallization [3,4], particularly as bottomless diffusion barriers, liners, capping layers, and interconnects, due to their high melting points, low resistivity, excellent thermal stability, and low reactivity with Cu and its area selective deposition methods have been requiring.

In this work, we developed conductive MoC_x films via thermal ALD without the use of halogen-based precursors, at the deposition temperatures of 200−300 ℃. This process enabled area-selective growth of MoC_x films on metallic substrates (TiN, Ru, Cu) over oxide substrates (SiO_2, Al_2O_3) by utilizing the intrinsic chemical adsorption of the precursor. We investigated the crystallinity, chemical bonding states, impurity, and resistivity of the MoC_x films (Fig. 1), and evaluated the selectivity between substrates through analysis of Mo areal density and film thickness. Moreover, the selective growth of MoC_x films on metallic substrates was demonstrated on metal/dielectric patterns using auger electron spectroscopy (AES) mapping and energy-dispersive X-ray spectroscopy (EDS) analysis, indicating the feasibility of implementing this process in practical device applications (Fig. 2). To elucidate substrate-dependent surface chemistry in MoC_x AS-ALD, density functional theory (DFT) calculations were conducted, revealing the relative adsorption energies of Mo precursor between metal and dielectric substrates (Fig. 3). In conclusion, a newly developed inherent AS-ALD of MoC_x films presents a promising alternative to top-down processes, offering a simplified workflow and potential conducting materials for advanced metallization.

References

1. Gregory N. Parsons et al., Chem. Mater., 32, 12, 4920–4953 (2020)
2. Adriaan J. M. Mackus et al., Chem. Mater., 31, 1, 2–12 (2019)
3. Min-Ji Ha et al., Chem. Mater., 34, 6, 2576–2584 (2022)
4. Paloma Ruiz Kärkkäinen et al., Adv. Mater. Interfaces, 2400270 (2024)

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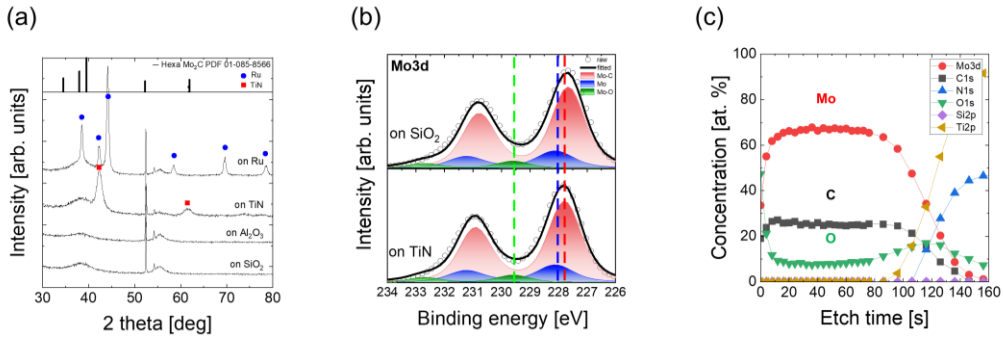

Figure 1 (a) GIXRD patterns of MoC_x films depending on metal and dielectric substrate, (b) XP spectra of Mo 3d for MoC_x films on SiO_2 and TiN substrate, (c) The XPS depth profiling for atomic concentration of MoC_x films

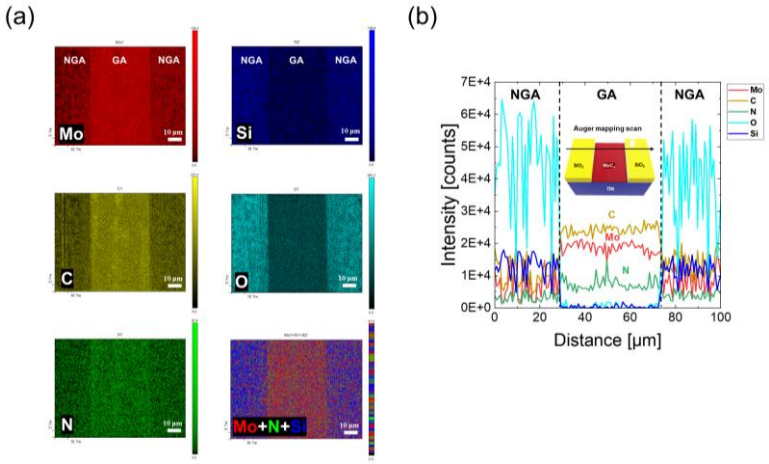

Figure 2 (a) Auger elemental mapping images and (b) auger line scan in a lateral direction of MoC_x films on SiO_2/TiN patterned substrates

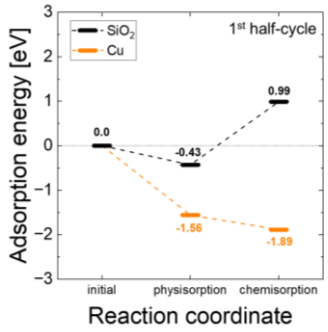

Figure 3 The adsorption energy of Mo precursor depending on the substrates for 1st half-cycle

Epitaxial $SrTiO_3$ thin films on silicon for electro-optical quantum devices

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Electro-optical (EO) quantum transducers will be key to quantum information processing as they are the gateway to transfer information between electronics (RF qubits) used for computation and photonics (optical qubits) used for communication. However, quantum applications require EO transducers that offer unity efficiency which is difficult to achieve with current materials. Perovskite oxides are an auspicious category, featuring high dielectric permittivity values at radio frequencies, strong nonlinearities and some materials such as $BaTiO_3$ can be integrated into standard silicon photonics. An overlooked material in the EO transducer community is strontium titanate ($SrTiO_3$, STO). Its intrinsic parameters allow a direct growth on silicon, it shows nonlinear optical behaviour and importantly, its dielectric permittivity of several hundred at room temperature is very high and increases further to ~10^4 at cryogenic temperatures thanks to its quantum paraelectric behaviour [1] making it an ideal transparent electrode material.

Molecular beam epitaxy (MBE) is one of the few techniques which allows epitaxial growth of STO directly on industry-relevant Si substrates. However, maintaining precise stoichiometry and high crystalline quality in this process remains a significant challenge. Establishing this is essential to obtain STO with bulk-like dielectric properties and to minimize leakage current and optical absorbance. In this study, the importance of cationic stoichiometry and the effect of thickness are investigated for STO thin films epitaxially grown on (001)-oriented silicon substrates.

High-temperature post-growth annealing treatments in O_2 were investigated to promote layer relaxation and reduce oxygen vacancy concentration, thereby improving the physical, electrical, and optical properties of stoichiometric STO. As a result, high-quality STO thin films exceeding 100 nm were successfully fabricated featuring a bulk-like out-of-plane lattice parameter and refractive index, as well as rocking curve full width at half maximum (FWHM) below 0.2°, smooth surface (R_q < 0.2 nm) and a leakage current density below 1E-7 A/cm^2 [2].

This epitaxy process for MBE growth of high-quality thick STO layers on silicon (001)-oriented substrates is essential for optimizing dielectric properties, such as the dielectric permittivity. By establishing a correlation between cationic stoichiometry, crystallinity, and STO thickness, we achieve significant enhancement of the effective permittivity at cryogenic temperatures, reaching values of over 2,500 for our stoichiometric 105 nm STO film. To our knowledge, this is the highest reported permittivity for STO thin films on silicon. This study paves the way for using STO thin films as active materials in advanced devices for various applications, including energy storage and quantum information technology.

References:

[1] Müller, K., Burkard, H., "$SrTiO_3$: An intrinsic quantum paraelectric below 4K," *Phys. Rev. B*, (1979), 19, 3593–3602.

[2] A. Boelen, M. Baryshnikova, A. Ulrich, K. Brahim, J. Van de Vondel, C. Haffner, and C. Merckling, "Stoichiometry and Thickness of Epitaxial $SrTiO_3$ on Silicon (001): An Investigation of Physical, Optical, and Electrical Properties," *APL Materials*, manuscript submitted for publication, 2025.

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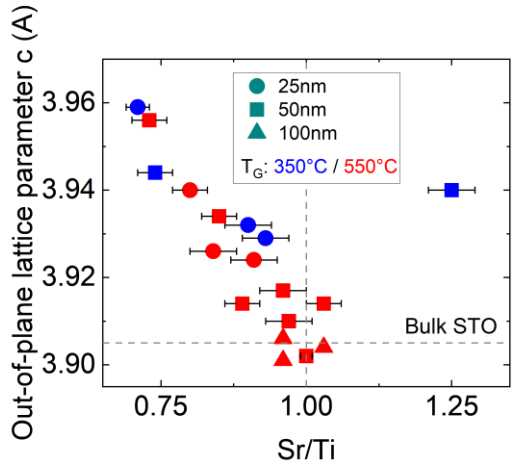

Figure 1: Out-of-plane lattice parameter (c) as a function of Sr/Ti ratio for STO films with varying thickness and growth temperature T_G. For obtaining a bulk-like lattice parameter, perfect cationic stoichiometry, high growth temperatures and layers > 50 nm need to be fulfilled.

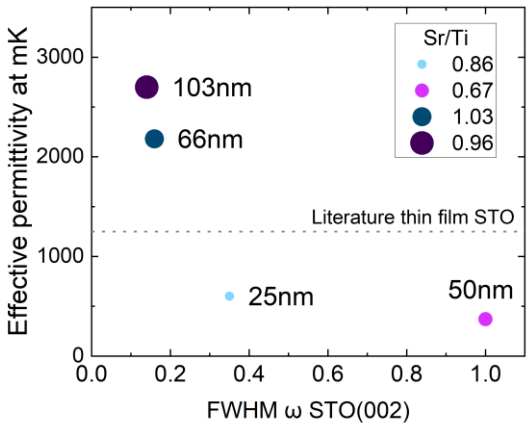

Figure 2: Effective permittivity ε_{eff} near 0 K as a function of the STO (002) rocking curve FWHM. Cationic stoichiometry (Sr/Ti = 1) and increasing STO thickness result in lower FWHM and higher effective permittivity.

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Nickel silicide phase change transformation upon nanosecond laser annealing

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In recent devices, nickel silicide is widely used due to its low resistivity and silicon consumption [1]. A classical process flow used for nickel silicide fabrication consists in a first anneal to form the Ni_2Si phase, a selective etch to remove unreacted metal, and a second anneal to obtain the low resistivity NiSi phase [1]. However, the high diffusivity and the low temperature stability of the phase of interest is a problem [2]. Research has been performed on the second anneal to overcome these problems. "Plateau" anneal [3], spike anneal [4] and then millisecond anneal have been investigated with significant gains in agglomeration robustness [5–7]. Nanosecond anneal is a logical alternative but still largely unexplored when the energy is kept below the melting threshold [8].
Sample preparation is described in **Figure 1.** On a p-doped bulk silicon substrate, a partial silicidation followed by a selective etch is performed. Then, nanosecond (ns) anneals at different energy densities are applied. The sheet resistance (Rs) value as a function of nanosecond laser energy density is shown, for 10 laser shots in ***Figure 2***. The curve shows four distinct regimes. R_S exhibits a high resistance plateau, followed by an intermediate one, then a low resistance plateau. The last regime starts with an abrupt R_S increase due to the onset of silicide melting.
To better understand this phase transformation curve, in-plane and out-of-plane X-ray diffraction (XRD) measurements were performed (***Figure 3***). In the diagrams corresponding to the initial plateau and the melt region at around 1 J/cm², small peaks of Ni_3Si_2 (identified by circles in the figure) are detected. In the intermediate plateau, the main phase observed is Ni_3Si_2. In the low resistivity plateau, the NiSi phase is identified (triangles) with residual peaks of Ni_3Si_2 but with a different preferential orientation compared to that in the intermediate plateau. In melt region at high ED no other peaks than the one due to the substrate is obtained. The formed silicide(s) may be amorphous or made of too small nanocrystallites to be detected.

The possibility of obtaining a low resistivity NiSi phase by nanosecond laser anneal was thus demonstrated. The phase sequence obtained with ns anneal was atypical. In fact, the expected Ni_2Si phase was not seen in XRD for the initial plateau. Furthermore, an intermediate phase between the first Ni silicide phase and the NiSi phase was shown to be Ni_3Si_2. Finally, the melt regime showed a huge variation in resistivity, which was not correlated with the evolution of the diffraction peaks, since no peaks other than those due to the substrate were detected in XRD diagrams at high energy density.

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1. J. Foggiato et al., Mat. Sci. and Eng.: B **114–115**, 56 (2004).
2. N. Breil et al., Microelec. Eng. **137**, 79 (2015).
3. B. Imbert et al., Microelec. Eng. **87**, 245 (2010).
4. T. Futase et al., IEEE Transac. on Semi. Manuf. **22**, 475 (2009).
5. C. Ortolland et al., in *2009 IEEE International Electron Devices Meeting (IEDM)* (2009), pp. 1–4.
6. M. Gregoire et al., in *2011 IEEE International Interconnect Technology Conference* (2011), pp. 1–3.
7. J. Kim et al., IEEE Trans. on Elec. Dev. **66**, 389 (2019).
8. J. Kim et al., Journal of Alloys and Compounds **788**, 1013 (2019).

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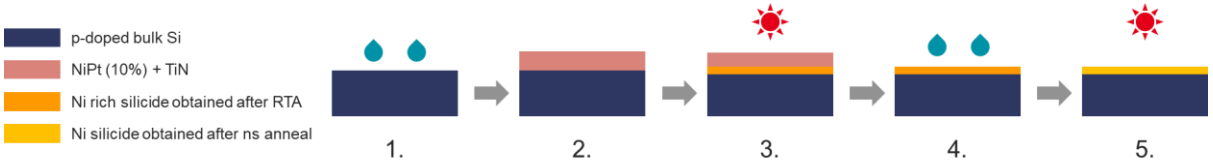

Figure 1: Details of the sample preparation flow. 1. Wet surface preparation. 2. 16 nm NiPt (10%) deposition. 3. Rapid thermal annealing (RTA) for partial silicidation. 4. Selective etch to remove unreacted metal. 5. Nanosecond laser anneal to complete phase transformation.

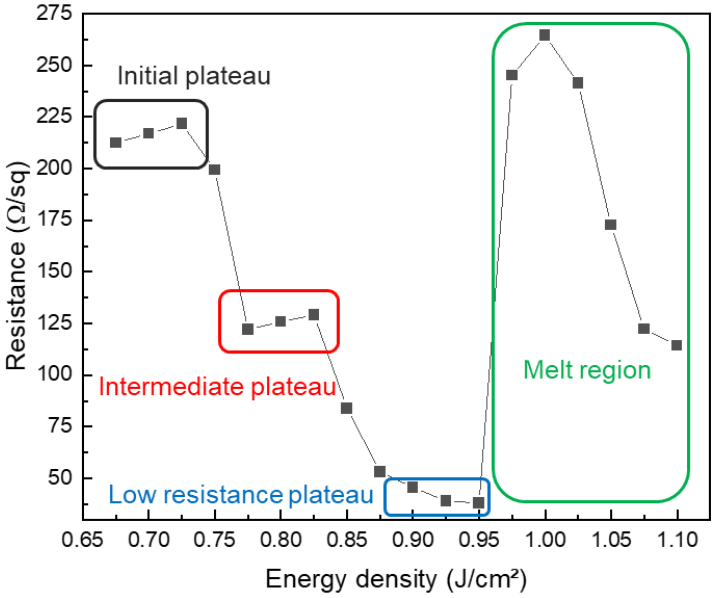

Figure 2: Sheet resistance (Rs) as a function of nanosecond laser energy density for 10 laser shots.

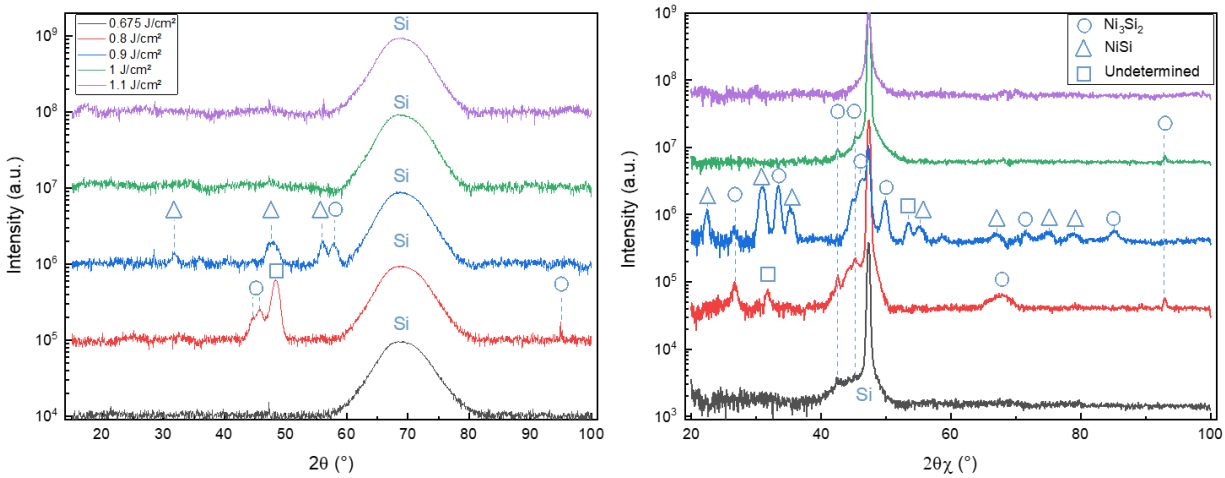

Figure 3: Out-of-plane (left) an in-plane (right) X-ray diffraction diagrams for different nanosecond laser energy densities.

Contribution of varying accelerating voltage for S/TEM EELS and EDS analysis of AlGaN/GaN based semiconductors

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The integration of Scanning Transmission Electron Microscopy (STEM) with electron energy-loss spectroscopy (EELS) and Electron-Loss Near-Edge Structure (ELNES) has gained significant attention within the microelectronics sector. ELNES, in particular, offers enhanced insights into the local atomic and electronic structures of materials, surpassing the traditional X-ray Energy Dispersive Spectroscopy (XEDS) used for chemical analysis in that regard. This study aims to explore the properties of High-Electron Mobility Transistor (HEMT) devices constructed from $Al_xGa_{1-x}N$ semiconductors, which are designed for high-power and high-frequency applications [1], utilizing EELS. STEM analyses are conducted using a probe Cs-corrected JEOL Neo-ARM 200F, featuring a Cold-FEG and a GIF Continuum spectrometer.

The HEMT device under examination consists of a GaN channel and an AlGaN barrier structure, separated by a few-nanometre AlN spacer to enhance the performance of the 2-Dimensional Electron Gas (2DEG) formed at the interface [2]. Given the substantial lattice mismatch between GaN and Si, an AlN nucleation layer is initially grown on 300 mm Si wafers. Subsequently, $Al_xGa_{1-x}N$ buffer layers with progressively decreasing aluminum content are employed to manage the stress within the structure (Fig. 2 (a)). This buffer configuration facilitates the growth of a crack-free GaN channel, ensuring optimal electron mobility within the device.

In this study, the first objective will be to present the contribution of varying S/TEM accelerating voltage on the limitation of electron-beam damage at the active region interface. In fact, electron-beam irradiation is susceptible to induce sputtering and knock-on damage which are amplified by higher accelerating voltages and low sample thickness with aggravated surface contamination. As illustrated by Fig.1, a conventional high tension (HT) of 200 kV will favour carbon surface contamination as well as leading to the sample deterioration, in that case with the formation of nitrogen dimer at the periphery of a previously scanned area. In that regard, it was shown that the use of lower HT (i.e. 80 and 60 kV) greatly reduces damage and contamination, even at sensible areas as observed by experiments with intensive static-beam irradiations in AlN spacer.

Additionally, the probability of an incoming electron to interact with and ionize an atom is linked to the ionization cross-section of an atom inner shells. Thus, a larger ionization cross-section provided by lower HT [3] will lead to a greater probability of scattering events meaning an increased production of x-rays and increased EELS detections in theory. This phenomenon has been verified in this work on EDS signals of GaN, AlN and Si bulks for various thickness samples, t, (with $t \approx [30, 200]$ nm). Fig.2 shows that for each EDS peak (Al, Ga and N K peaks), we observe a significant increase of peak intensities for lower HT. It is also observed that the profile intensity of the heavier atoms (i.e) Al and Ga K peaks tends to follow the thickness profile where the N K peak intensity profiles in both materials seems to be constant or even slightly decrease for $t > 100$ nm. Furthermore, the contribution of the lower HT to the production of N K x-rays seems to be significantly less important in GaN compared to AlN most probably due to a higher material density of the GaN. This will eventually be confirmed by simulations of the interactions of electron in both AlN and GaN.

Finally, the contribution of lower HT to ELNES analysis of the N K edge (Fig. 3) will also be discussed in order to provide insight on the benefits of each HT in terms of signal intensities, energetical resolution and comparison of the fine structure to simulation, which are key factor for advanced EELS analysis.

References

[1] T. D. H. Nguyen, phdthesis, Université Paris Sud - Paris XI, 2013.
[2] R. Ramesh et al, Materials Chemistry and Physics **259**, 124003 (2021).
[3] X. Llovet,et al., Journal of Physical and Chemical Reference Data **43**, 013102 (2014).

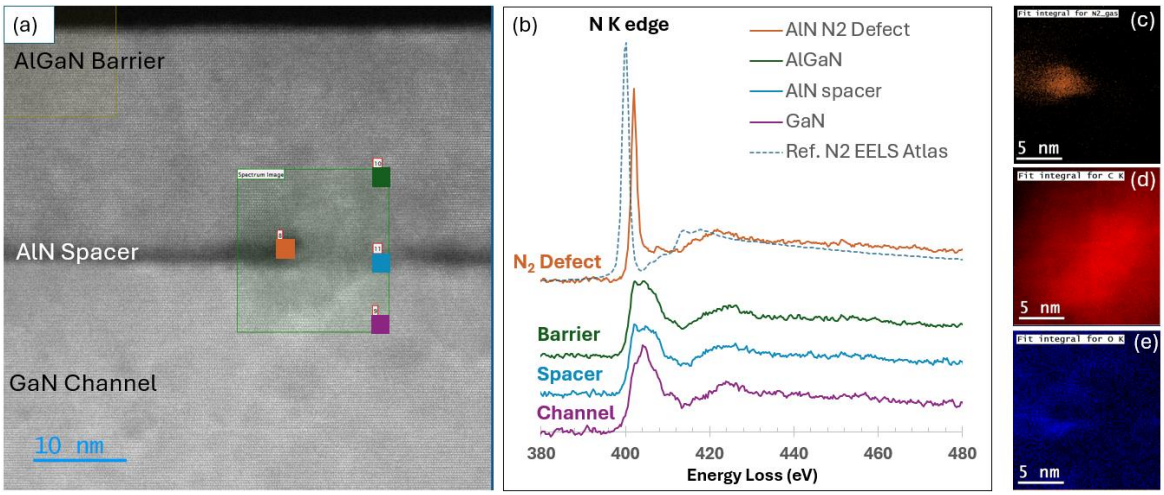

Figure 1. (a) HR-STEM micrograph with spectrum image in active region. (b) N K edges EELS spectrum in barrier, spacer and channel region with N_2 defect formation on AlN spacer at the periphery of the degraded spacer area shown by the loss of contrast observed in (a). (c, d, e) respectively the Mean Least-Squares (MLS) fitting maps of the characteristic N_2 defect observed, as well as the C and O K EELS edges illustrating surface contaminations.

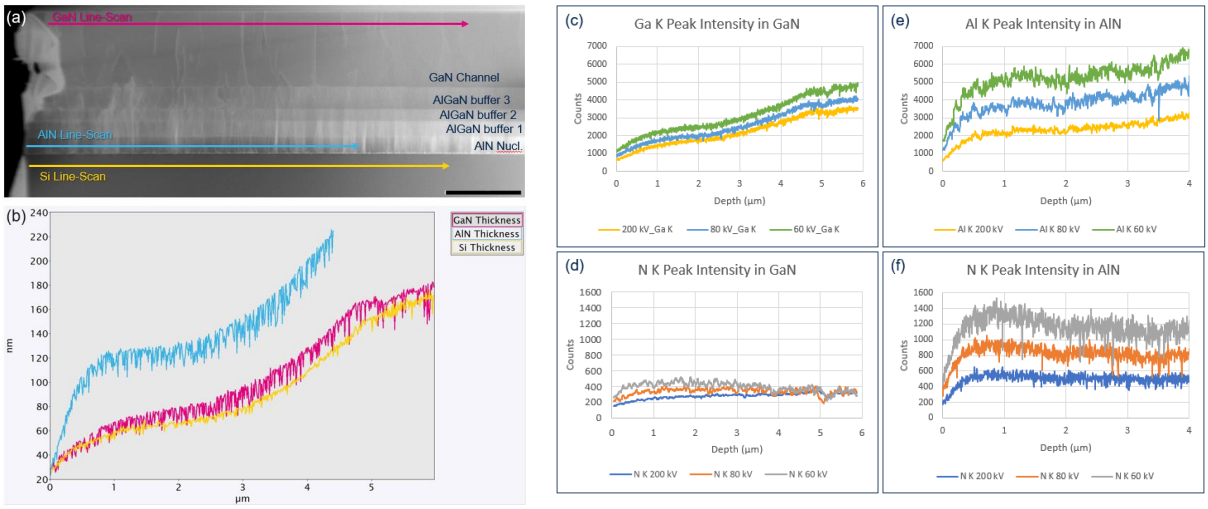

Figure 2. (a) HA-ADF micrograph of the stacking-fault with line scan location for bulk GaN, AlN and Si with their respective thickness profiles calculated from EELS Low-Loss (LL) spectra (b). (c, d) Ga and N K in GaN and (e, f) Al and N K in AlN EDS peak intensities respectively at 200, 80 and 60 kV.

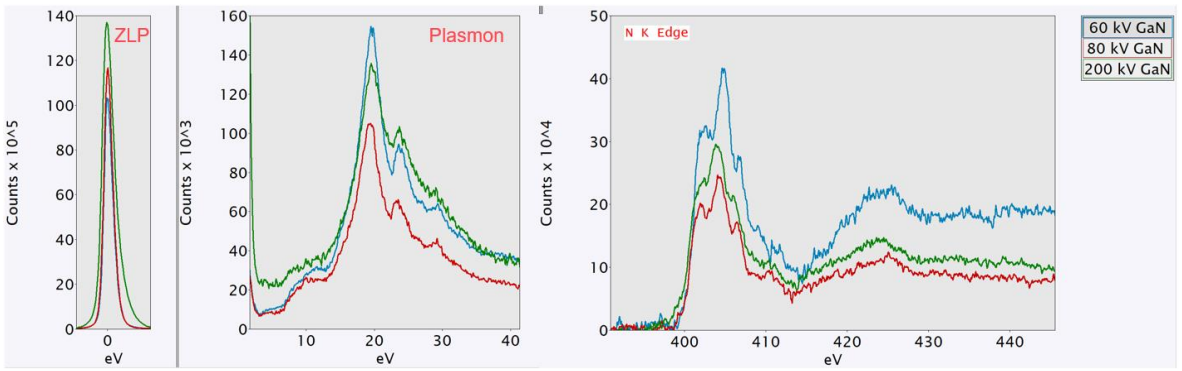

Figure 3. Contribution of lower HT for ELNES analysis in GaN with Zero-Loss Peak (ZLP), plasmon peaks and N K edge ELNES signal at 200, 80 and 60 kV. Slight differences of fine structures of the N K edge can be observed depending on HT with slight shifts in energy and intensities.

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Ultrahigh-density '*electrolithic'* storage memory proof-of-principle with high-aspect-ratio nanometer-sized holes

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It is estimated that more than 1 billion Tbit will be stored in the cloud in 2024 [1]. This amount has been growing at a compound annual growth rate of roughly 35% over the previous years [1]. At the same time, bit-density scaling of 3D NAND flash and hard disk drives (HDD) is becoming increasingly more difficult [2]. Therefore, it is unlikely that these two main storage technologies will remain cost-effective in the future.

To address this issue, we previously introduced 'Electrolithic Memory' [3], which has the potential to provide bit densities up to 1 Tbit/mm^2. This bit density significantly goes beyond the ~20 Gbit/mm^2 that 3D NAND flash reaches today [4], or even its predicted end-of-roadmap (~100 Gbit/mm^2) [2]. The 'Electrolithic Memory' concept relies on electrodeposition and -dissolution of multilayered metal stacks from a tight-pitched array of nanometer-sized high aspect ratio holes (Fig. 1). Provided an extremely precise control of the individual metal layer thicknesses can be achieved, these layered stacks can be used to encode information and achieve very high bit densities.

The proof-of-principle presented in [3] was limited to large area electrodes, which only allowed a few bits to be read successfully. To further understand the dissolution process that leads to a poor read-out signal, we deposited alternating Cu (10 nm) and Ni (5 nm) layers on a blanket wafer using physical vapor deposition (PVD). The resulting dense, well-defined, and uniform metal layers served as a model system for a perfectly deposited stack. As such, we can interpret the read-out signal without the uncertainties introduced by a granular or non-uniformly electrodeposited stack. By inspecting the metal stack with STEM-EDS at intermediate stages of the electro-dissolution process, it was observed that dissolution of multiple Ni|Cu bilayer occurs in three steps (Fig. 2): i) passivation of the Ni layer, ii) pinhole formation and breakthrough of that Ni layer, and iii) selective dissolution of the underlying Cu layer. This process repeats for the subsequent layers of the stack. Consequently, the dissolution leaves behind Ni residues, which obstruct read-out of layers located deeper in the stack.

Ultimately, the problem with using blanket wafers to evaluate the memory concept, is that the layers are typically thin (<100 nm) compared to the exposed coupon area (1 cm^2). Then, random pinhole formation, residue formation, and other coupon scale non-uniformities severely impact the overall read-out signal. To resolve this problem and bring the proof-of-principle closer to the final application, we fabricated patterned coupons consisting of a large array (>10^6) of holes (80 nm diameter), etched in 1 µm thick SiO_2 (Fig. 3). All the holes land on a common, blanketed Ru bottom electrode. The holes were spaced sufficiently far apart (4 µm) so that hole-to-hole diffusional crosstalk could be ignored. Using a citrate-based CuNi plating bath [5], we were now able to read out more layers, as the dissolution process occurred layer-by-layer in the nanoholes, resulting in a more pronounced read-out signal (Fig. 4).

To reach bit densities approaching 1 Tbit/mm^2, the layer thickness must be further reduced, ultimately down to 2 nm. To achieve this, the plating bath needs improvement so that dense and smooth multilayers can be obtained. In addition, despite being practical for bench-top experiments, the large array of holes must be scaled down to a single hole to provide a convincing demonstrator. Due to the small currents and charges involved for individual holes, active CMOS circuitry is necessary to amplify and control the memory hole and work is ongoing to realize such a demonstrator.

References

1. A. Smith *et al.*, IDC, US47565321 (2021).
2. T. Coughlin *et al.*, IEEE IRDS 2023 (2023).
3. S. Fransen *et al.*, IEEE Trans. Electron Devices **66**, 4504 (2019).
4. Khakifirooz et al., IEEE Solid-State Circuits **6**, 161 (2023).
5. X. Cui and W. Chen, J. Electrochem. Soc. **155**, K133 (2008).

* *corresponding author e-mail: Senne.Fransen@imec.be*

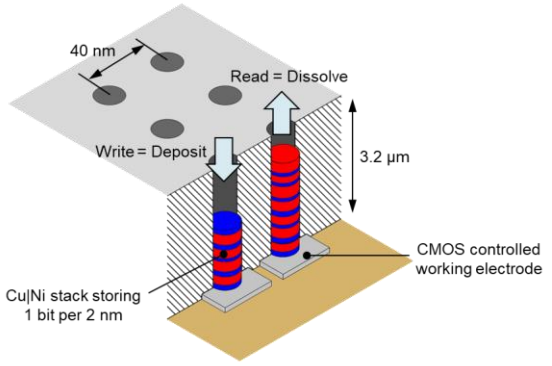

Fig. 1: Schematic of the 'Electrolithic Memory' concept, with envisioned dimensions that would lead to a bit density of 1 Tbit/mm^2.

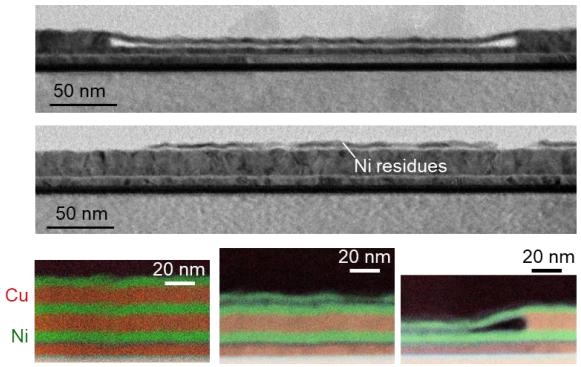

Fig. 2: STEM micrographs and EDS maps of PVD Cu|Ni stacks that have been partially dissolved electrochemically at 21 mA/cm^2 in 0.5 M H_2SO_4 (200 rpm sample holder rotation).

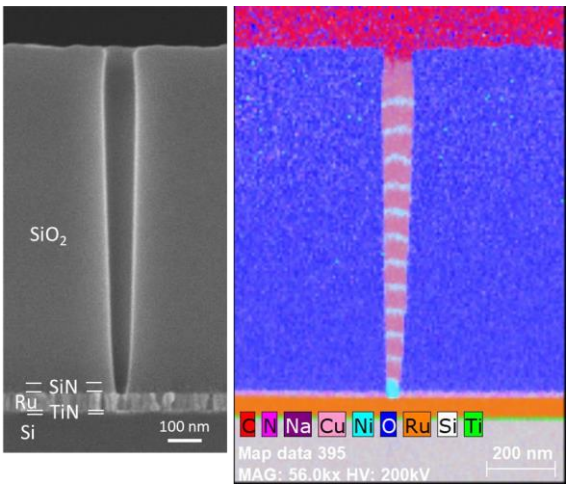

Fig. 3: (left) XSEM of a high aspect ratio hole with 80 nm diameter and 1 µm depth. (right) Electrochemically deposited $(Cu|Ni)_{12}$ multi-layered stack using a single citrate-based plating bath.

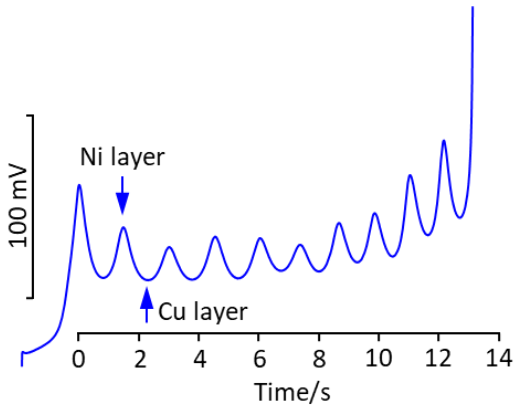

Fig. 4: Electrochemical dissolution of a $(Cu|Ni)_{11}$ multilayered stack from an array with 6×10^6 holes at 5.3 pA/hole, in the same plating bath that was used for deposition.

Electrical analysis of damascene patterned metal lines to evaluate patterning yield of EUV 0.33NA lithography

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A set of electrical test structures (serpentines and combs) are demonstrated to detect defects, line breaks and pinches, formed during lithography patterning. These structures were patterning using 0.33 NA EUV (NXE 3400) down as far as pitch 26nm and transferred using single damascene W metal fill. This method can demonstrate a combo yield (opens + shorts) of 99.7% for 1m long structures corresponding to a defect density of 12 defects/cm2. This method can be used as a platform to screen and test different aspects of lithography and patterning processes.

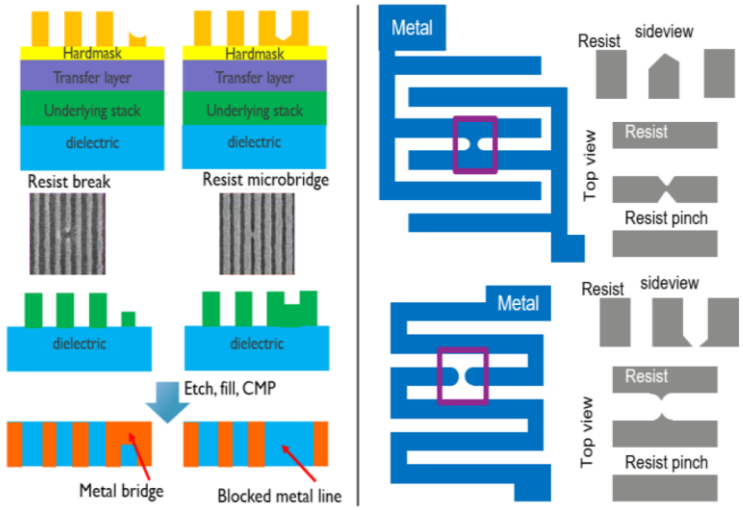

Fig. 1 Schematic representation of the different type or resist defects and its process transfer through full damascene process.

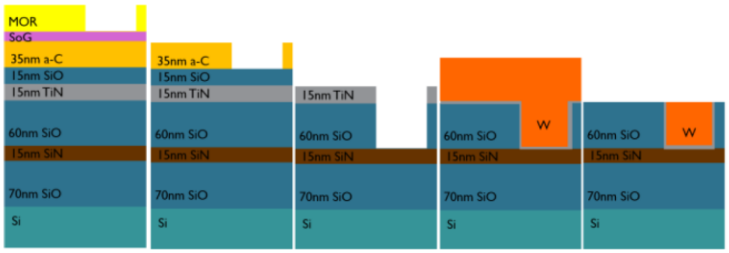

Fig. 2 Schematic representation of the fabrication process flow. From left to right: MOR resist exposure, pattern transfer into a-C hard mask, pattern transfer into final oxide layer, TiN hard mask wet strip and TiN liner and W CVD deposition, W CMP.

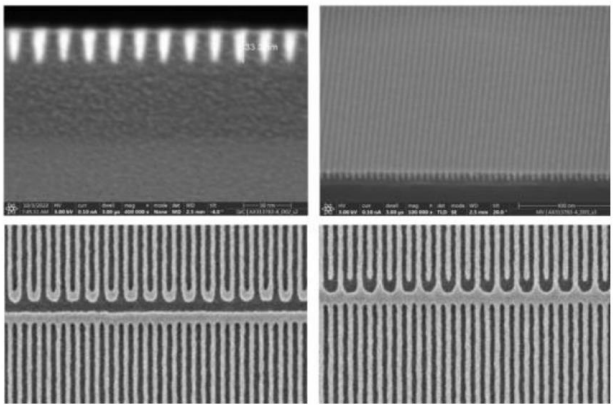

Fig. 3 Example cross-SEM pictures of fabricated devices after metallization and CMP (top) and top view CD-SEM inspection after etch inspection into TiN hard maks of meander and for structures.

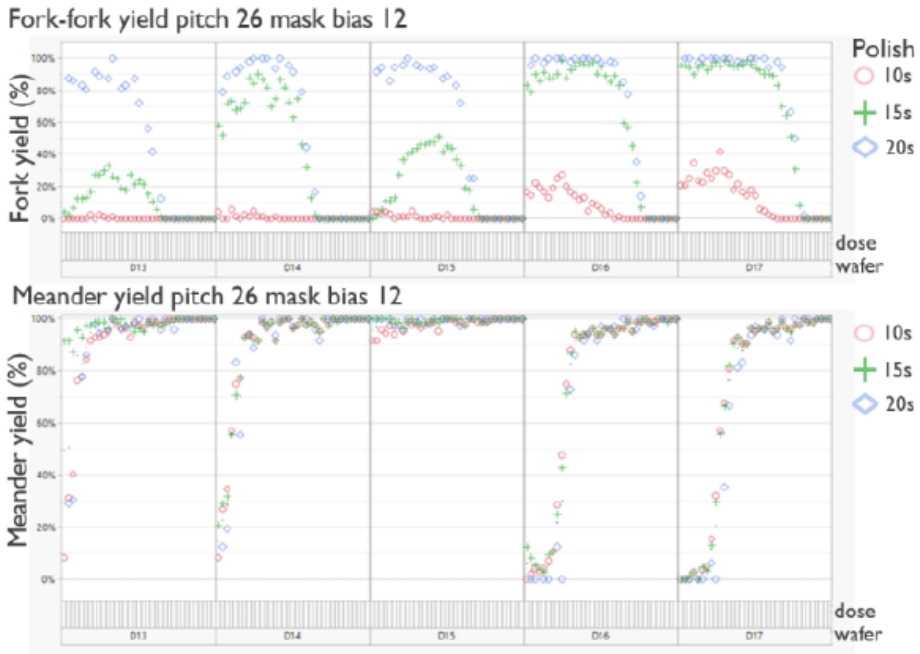

Fig. 4 Fork-fork (top) meander (bottom) yield for five different dose stripe wafers with various process conditions as function of CMP time for mask bias 12nm and one point per field electrical test measurements.

References

1. L. Tan, W. Gillijns, J. Lee, D. Xu, J. Kerkhove, V. Philipsen, R. Ki, " EUV low-n attenuated phase-shift mask on random logic Via single patterning at pitch 36nm", Proc. SPIE 12051, Optical and EUV Nanolithography 2022, 120510P (2022) https://doi.org/10.1117/12.2614000
2. Carballo, V.M. & Wachter, K. & Nafus, Kathleen & Feurprier, Y. & Thiam, Arame & Hsu, A. & Tabery, C. & Doise, J. & Schepper, P.. (2024). Patterning process and electrical yield optimization at the limits of single exposure EUV 0.33 NA: a pitch 26nm damascene process. 1-3. 10.1109/IITC61274.2024.10732293.

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Optimizing ultrathin HfO_2-ZrO_2 structures by ALD for BEOL-compatible ferroelectric non-volatile memories

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Ferroelectric HfO_2-based materials are promising for advanced memory applications due to their CMOS compatibility, scalability, and low processing temperatures, such as 400 °C, suitable for back-end-of-line (BEOL) integration. Among these, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) stands out for its strong ferroelectric properties, reaching a remanent polarization of 40 µC/cm² [1]. However, reducing the thickness of HZO to ultrathin values (<10 nm) to lower the operating voltage and meet the demands of low-power memory applications introduces critical challenges, including increased crystallization temperature, higher leakage currents, and instability that affect device endurance and reliability [2,3].

To further optimize the properties of ferroelectric films, the multilayer approach has demonstrated significant potential in addressing the challenges of ultrathin HZO films. By stacking alternating HfO_2 and ZrO_2 layers, this method can reduce leakage currents by blocking electron injection from the electrodes, thereby enhancing endurance and stability [4]. Additionally, multilayers can also provide an additional degree of control over ferroelectric performance through the careful design of the stacking sequence and layer thicknesses.

The aim of this work is to develop ultrathin ferroelectric layers by ALD for MFM (Metal Ferroelectric Metal) capacitors for non-volatile memories. Within this work, two different types of structures were investigated: HZO solid solution, made through supercycles, and HfO_2/ZrO_2 nanolaminates consisting of stacked HfO_2 and ZrO_2. To explore ferroelectric performance at reduced thicknesses, the film was scaled down to 4 nm, with the nanolaminate achieved by stacking 1 nm of HfO_2 and 0.5 nm of ZrO_2.

The experimental results demonstrate the influence of structural configuration, composition, and annealing conditions on ferroelectric performance in ultrathin HZO films. For the 10 and 6 nm HZO samples, annealed at a BEOL-compatible temperature of 400°C, ferroelectric properties were achieved, validating its potential for integration in non-volatile memories. However, reducing the thickness to 5 and 4 nm introduced challenges that required increasing the crystallization temperature to 500 °C and modifying the structure to nanolaminates with higher Hf content. The Zr composition in the multilayer structure was deliberately lowered to prevent excessive stabilization of the tetragonal phase, which is known to negatively impact ferroelectric properties in ultrathin films. Despite these adjustments, further optimization of the annealing temperature for 5 and 4 nm samples is necessary to ensure compatibility with BEOL processing, potentially through approaches such as laser or rapid thermal annealing. XRD analyses (Fig. 1) confirm the existence of a peak near $2\theta \approx 30.5°$ in the samples, indicating the presence of orthorhombic or tetragonal phases. While the HZO 1:1 at 4 nm lacked a well-defined peak due to incomplete crystallization, nanolaminates of the same thickness exhibited distinct peaks, reflecting improved crystallization.

The P-E hysteresis loops (Fig. 2) further highlight the benefits of these modifications. The 5 nm HZO, annealed at 500 °C, demonstrated superior polarization, surpassing the 6 nm sample annealed at 400 °C. In contrast, the HZO 1:1 at 4 nm displayed antiferroelectric behavior, consistent with incomplete phase stabilization. The 4 nm nanolaminates, however, achieved promising ferroelectric performance, with a remanent polarization of approximately 10 µC/cm² and low coercive voltage, favorable for low-energy applications. The Ec-Vc plot (Fig. 3) revealed a clear trend of decreasing coercive voltage with reduced thickness, further emphasizing the potential of nanolaminates to maintain ferroelectric properties at ultrathin dimensions. However, HZO films remain BEOL-compatible only down to 6 nm. Further progress requires optimizing crystallization while meeting BEOL thermal limits for advanced memory technologies.

References

1. M. H. Park, Y. H. Lee, T. Mikolajick, et al., MRS Commun. 8, 795 (2018).
2. K. Toprasertpong, K. Tahara, Y. Hikosaka, K. Nakamura, H. Saito, M. Takenaka, and S. Takagi, ACS Appl. Mater. Interfaces 14, 51137 (2022).

3. C. I. Wang, H. Y. Chen, C. Y. Wang, T. J. Chang, Y. S. Jiang, C. S. Chang, and M. J. Chen, J. Mater. Chem. C 9, 12759 (2021).
4. Y. Chen, L. Wang, L. Liu, et al., J. Mater. Sci. 56, 6064 (2021).
*corresponding author e-mail: amanda.mallmanntonelli@cea.fr

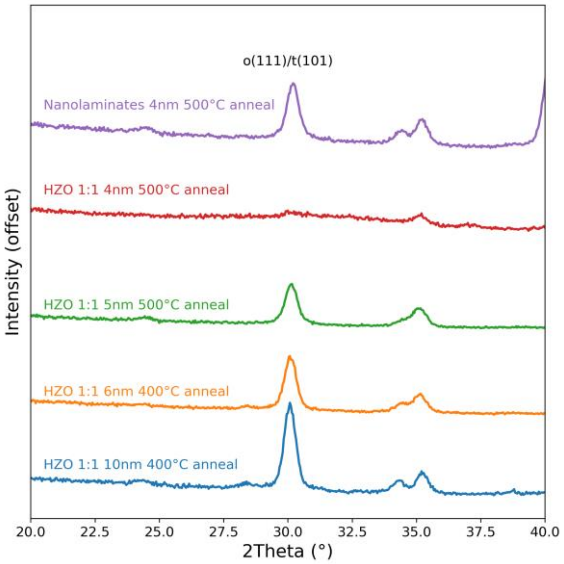

Fig. 1. In-plane XRD patterns of HZO films with varying thicknesses (10 nm, 6 nm, 5 nm, and 4 nm) and annealing conditions (400 and 500 °C), measured after the etching of the top electrode.

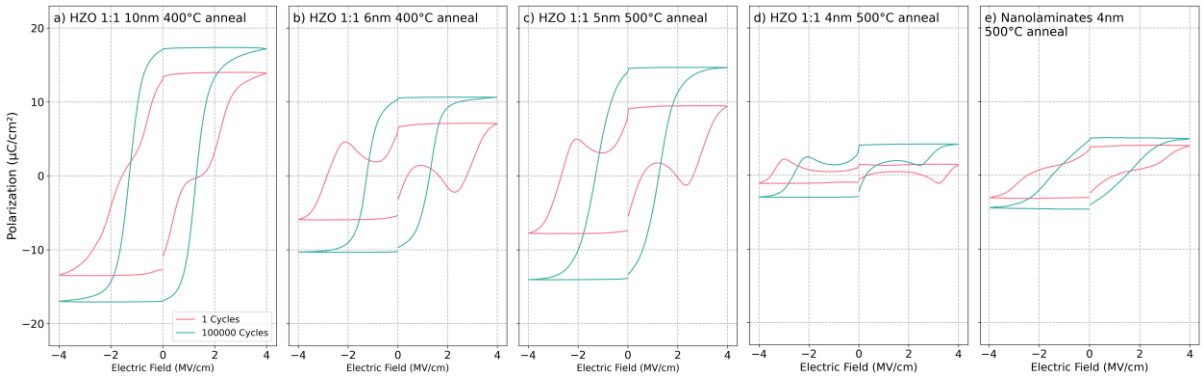

Fig. 2. P-E hysteresis loops of (a) HZO 1:1, 10 nm and (b) 6 nm, both annealed at 400 °C; (c) HZO 1:1, 5 nm, (d) 4 nm and (e) nanolaminates 4 nm, annealed at 500 °C. The nanolaminates at 4 nm show promising ferroelectric performance with a remanent polarization of approximately 10 μC/cm².

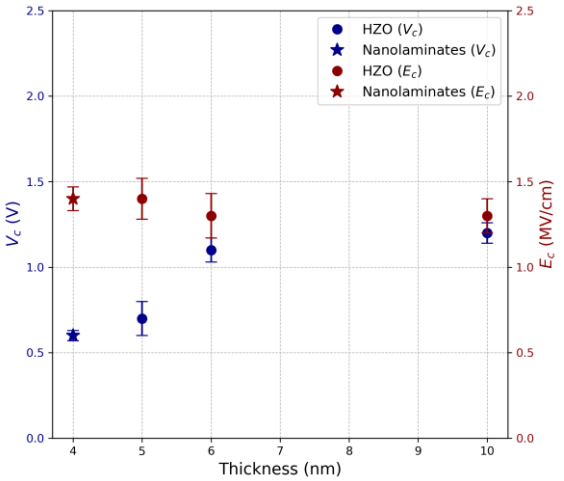

Fig. 3. Coercive voltage (Vc, blue, left axis) and coercive electric field (Ec, dark red points) as a function of film thickness after 10^5 cycles. The plotted samples include HZO 1:1 at 10 and 6 nm, both annealed at 400 °C, as well as HZO 1:1 at 5 nm and nanolaminates at 4 nm, annealed at 500 °C. Vc decreases with reduced thickness, which is favorable for low-energy applications

A model for the redistribution of Pt during the agglomeration of Ni(Pt)Si thin films

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Silicides, particularly thin films of Ni-Pt monosilicide (Ni(Pt)Si), are widely employed as contact materials in microelectronic devices, especially in complementary metal-oxide-semiconductor (CMOS) technologies. Their popularity is due to several advantages, including low resistivity and high thermal stability. However, as device dimensions shrink, contact thickness requirements can be as low as 10 nm, presenting significant challenges.
At such small scales, Ni(Pt)Si films become highly susceptible to agglomeration during high-temperature processing [1,2]. This agglomeration, driven by the reduction of interfacial energies and controlled by diffusion, can lead to morphological discontinuities and significantly reduce device yield. In polycrystalline thin films, agglomeration typically begins with grain boundary grooving, and usually results in isolated islands. For NiSi films, these islands form within the silicon substrate rather than on its surface, a phenomenon known as inverse agglomeration [1]. Luo et al. have shown that the slow diffusion of Si at the silicide/substrate interface plays a crucial role in NiSi agglomeration [1].
The addition of Pt to NiSi has been found to delay agglomeration, shifting it to higher temperatures [3,4], and is thus used industrially to stabilize the low-resistivity NiSi phase during high-temperature processing. However, the precise role of Pt in the agglomeration process is not yet fully understood and warrants further investigation.

In this study, the redistribution of Pt during the agglomeration of Ni(Pt)Si films is investigated using scanning transmission electron microscopy with energy-dispersive X-ray spectroscopy (STEM-EDX) measurements (Fig. 1). Results indicate that agglomeration follows the classical steps, beginning with the formation of holes by grain boundary grooving, and finally the expansion of holes, resulting in isolated islands of Ni(Pt)Si. The surface of the sample remains flat, corroborating the particularity of inverse agglomeration in Ni(Pt)Si thin films (Fig. 1.a). Moreover, the complex redistribution of Pt is characterized by the existence of three different regions: a Pt-rich surface region, a Pt-depleted region within the grain, and a moderately Pt-rich region near the silicide/Si interface that corresponds to the displaced Ni(Pt)Si (Fig. 1.d). A model is developed to describe the redistribution of Pt during grooving and agglomeration. A model based on spherical cap geometry is developed to describe the redistribution of Pt during grooving and agglomeration (Fig. 3). It is based on similar assumptions to our previous model [1], with additional assumptions for the Pt redistribution including diffusion at the silicide/Si interface (Fig. 4). The model allows reproducing the Ni(Pt)Si island shape and Pt redistribution within these islands after grooving and agglomeration (Fig. 5) but underestimates the concentration of Pt in the displaced Ni(Pt)Si. The difference can be explained by diffusion from the Pt-rich sub-surface region to the region near the silicide/Si interface, involving volume diffusion in addition to diffusion at the surface, grain boundaries (GB), and interface, which are fast diffusion paths (Fig. 2). These findings have implications for understanding the complex nature of Ni(Pt)Si agglomeration and, especially, the role of Pt in the agglomeration phenomenon.

References

1. T. Luo, C. Girardeaux, H. Bracht, D. Mangelinck, Acta Materialia 165 (2019) 192
2. F. Morris Anak, A. Campos, M. Grégoire, A. Estellon, M. Lombard, T. Guyot, S. Guillemin, D. Mangelinck, Materials Science in Semiconductor Processing 184 (2024) 108806.
3. D. Mangelinck, J.Y. Dai, J.S. Pan, S.K. Lahiri, Applied Physics Letters 75 (1999) 1736
4. D. Mangelinck, J.Y. Dai, S.K. Lahiri, C.S. Ho, T. Osipowicz, MRS Proceedings 564 (1999)

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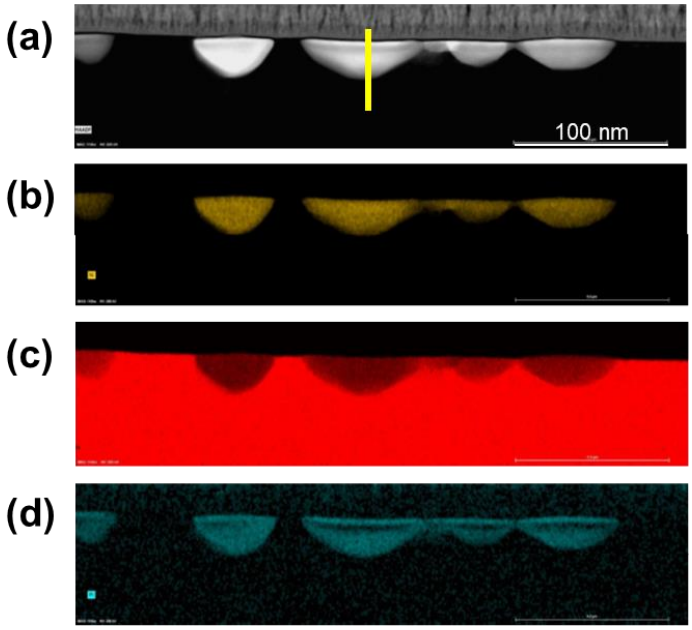

Figure 1: STEM-EDX cross-sections of the sample after the salicide heat treatment and RTAD at 700 °C: (a) STEM image, (b) Ni EDX map, (c) Si EDX map, and (d) Pt EDX map.

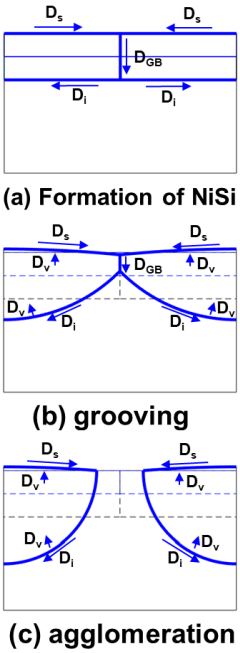

Figure 2: Schematics illustrating diffusion paths during different processing steps: (a) Formation (b) Grooving (c) Agglomeration

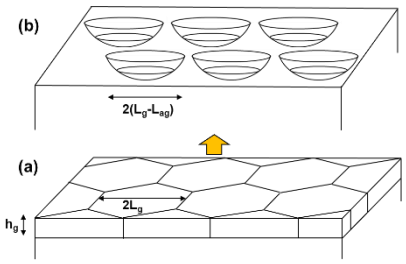

Figure 3: Schematics of the geometry used for the redistribution model: (a) initial columnar grains with a hexagonal base, (b) islands with a spherical cap shape after agglomeration

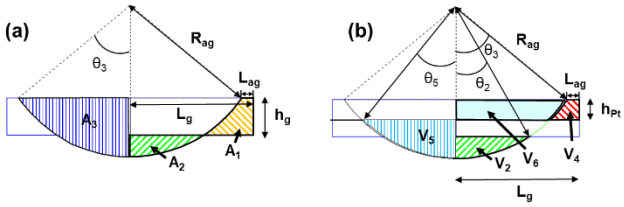

Figure 4: Schematic of the model used to simulate the agglomeration (a) change in the grain shape (b) redistribution of Pt. Only half of the annotated volumes is shown for clarity

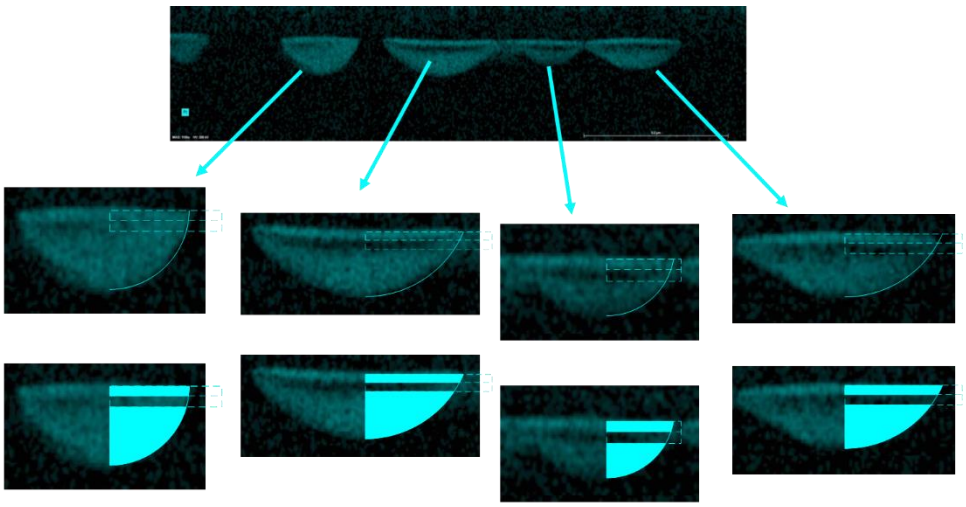

Figure 5: Fit of the EDX map for Pt for four grains after agglomeration (RTAD 700°C) using the present model: (a) whole EDX map for Pt, (b) EDX map for Pt with the fitted shape and Pt-rich region superimposed, (c) same as (b) with the Pt-rich regions highlighted in blue

Nearly-ideal Molybdenum Schottky contacts on AlGaN/GaN heterostructures

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Gallium Nitride (GaN) stands out as a promising material for next-generation high-power electronic devices due to its wide bandgap of 3.4 eV and high critical breakdown electric field of 3.3 MV/cm [1]. Additionally, the development of AlGaN/GaN hetero-epitaxial structures benefits from the coexistence of spontaneous and piezoelectric polarization [2], which leads to the formation of a quantum-confined two-dimensional electron gas (2DEG) with high sheet carrier density and electron mobility [3]. These properties make high electron mobility transistors (HEMTs) based on such heterostructures highly attractive for advanced high-power and high-frequency applications.

In HEMTs, Schottky contacts are critical for modulating the amount of charge of the 2DEG underneath the gate contact. The electrical behavior of Schottky contacts is ideally explained by the Thermionic Emission (TE) model, exhibiting temperature-independent parameters like the Schottky barrier height (Φ_B) and a unitary ideality factor (n) [4]. However, in AlGaN/GaN heterostructures, deviations from ideality are particularly significant, often with ideality factors exceeding 2 [5], [6]. Furthermore multiple mechanisms are often employed to rationalize the overall conduction mechanism [5], [6]. Such strong deviations from ideality indicate the complexity of conduction mechanisms in these systems and highlight the need for detailed studies to understand these behaviors.

Commonly used Schottky contacts for AlGaN/GaN heterostructures employ Ni/Au bilayers. On the other hand, also other unconventional metallization, such as W, TiN, WC, Cu, Fe, or Al have been explored [7]. Molybdenum (Mo), as a refractory metal with a high melting point (2600 °C), exhibits favorable properties such as thermal stability, mechanical strength, good adhesion to AlGaN/GaN surfaces, and low oxidation tendency below 500 °C. Despite its potential as a cost-effective "Au-free" alternative, the application of Mo Schottky contacts in GaN-based electronics deserve further investigation.

This study investigated Mo Schottky contacts on AlGaN/GaN heterostructures using current-voltage-temperature (I-V-T) measurements (see Fig. 1). The results, displayed in Fig.2, indicate near-ideal TE behavior, with an ideality factor of ~1.26 at 25 °C and minimal changes over the temperature range of 25–150 °C. The barrier height increased slightly from 0.85 eV to 0.89 eV, while the ideality factor decreased from 1.26 to 1.20. These findings suggest a minimal contribution from tunneling mechanisms. To address deviations from ideal TE behavior, the inhomogeneity of the Schottky barrier was analyzed using Tung's model [8]. This model provides insights into the observed temperature dependence of the Schottky barrier and ideality factor, attributing the deviations to localized low-barrier regions embedded within the overall barrier [9],[10]. Furthermore, introducing the inhomogeneities contribution to the Richardsons' equation, it was possible to extract a value of the Richardsons' constant that is close to the one commonly used for AlGaN/GaN heterostructures (32 A cm^{-2} K^{-2}). Moreover, according to the Tung's model it was possible to model the I-V curves acquired at the different temperature by considering 10 different patches (see Fig.4).
These results expand the understanding of conduction mechanisms in AlGaN/GaN heterostructures and highlight Mo as a promising material for GaN-based electronics.

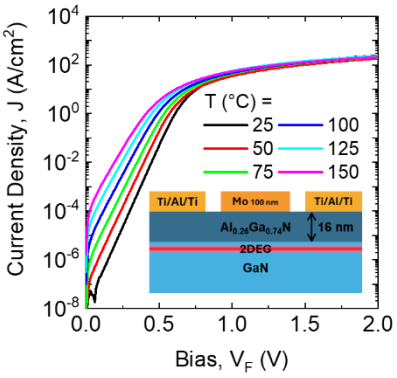

Figure 1 Experimental J-V curves of the Mo/AlGaN/GaN diodes

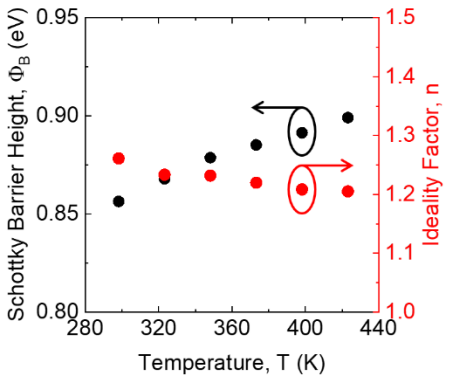

Figure 2 Thermal dependence of the barrier height and ideality factor

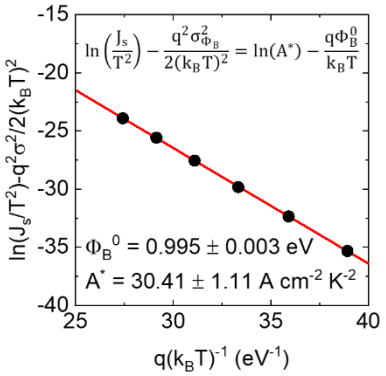

Figure 3 Richardsons' plot including the inhomogeneities contribution, extraction of a constant A* = 30.41 A cm^{-2} K^{-2}

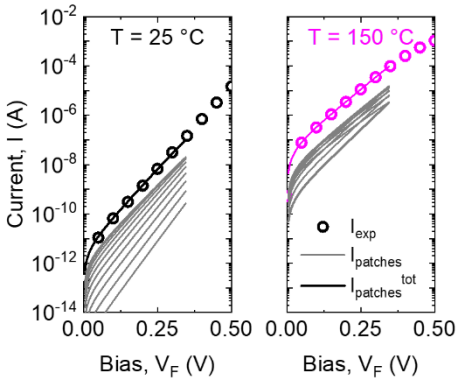

Figure 4 Rationalization of the conduction mechanism considering 10 different patches according to Tung's model

References

[1] F. Roccaforte, P. Fiorenza, R. Lo Nigro, F. Giannazzo, and G. Greco, “Physics and technology of gallium nitride materials for power electronics,” *La Rivista del Nuovo Cimento*, vol. 41, no. 12, pp. 625–681, Dec. 2018, doi: 10.1393/ncr/i2018-10154-x.

[2] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, “Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors,” 2000.

[3] O. Ambacher *et al.*, “Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures,” *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999, doi: 10.1063/1.369664.

[4] P. M. Gammon *et al.*, “Modelling the inhomogeneous SiC Schottky interface,” *Journal of Applied Physics*, vol. 114, no. 22, p. 223704, Dec. 2013, doi: 10.1063/1.4842096.

[5] E. Arslan *et al.*, “Electrical characterization of MS and MIS structures on AlGaN/AlN/GaN heterostructures,” *Microelectronics Reliability*, vol. 51, no. 2, pp. 370–375, Feb. 2011, doi: 10.1016/j.microrel.2010.08.022.

[6] D. Yan, J. Jiao, J. Ren, G. Yang, and X. Gu, “Forward current transport mechanisms in Ni/Au-AlGaN/GaN Schottky diodes,” *Journal of Applied Physics*, vol. 114, no. 14, p. 144511, Oct. 2013, doi: 10.1063/1.4824296.

[7] F. Roccaforte, M. Vivona, G. Greco, L. A. M. Lyle, B. Sarkar, and L. M. Porter, “Contacts to wide band gap (WBG) and ultra-wide band gap (UWBG) semiconductors for power electronics devices,” in *Comprehensive Semiconductor Science and Technology*, Elsevier, 2025, pp. 605–665. doi: 10.1016/B978-0-323-96027-4.00033-4.

[8] R. T. Tung, “Electron transport at metal-semiconductor interfaces: General theory,” *Phys. Rev. B*, vol. 45, no. 23, pp. 13509–13523, Jun. 1992, doi: 10.1103/PhysRevB.45.13509.

[9] F. Roccaforte, F. La Via, V. Raineri, R. Pierobon, and E. Zanoni, “Richardson’s constant in inhomogeneous silicon carbide Schottky contacts,” *Journal of Applied Physics*, vol. 93, no. 11, pp. 9137–9144, Jun. 2003, doi: 10.1063/1.1573750.

[10] F. Roccaforte *et al.*, “Barrier inhomogeneity in vertical Schottky diodes on free standing gallium nitride,” *Materials Science in Semiconductor Processing*, vol. 94, pp. 164–170, May 2019, doi: 10.1016/j.mssp.2019.01.036.

Study ZnSb Phase Change Material Alloys for Nonvolatile Embedded-Memory Applications

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Phase-change materials (PCMs) play a key role in emerging memory technologies, particularly in resistive phase-change memories (PCRAM). Among well-studied PCMs, GeSbTe (GST) [1], GaSb [2], and SbTe [3] stand out. Our study focuses on ZnSb alloy, a promising intermetallic semiconductor, exhibiting a crystallization temperature of 257°C, an activation energy of 5.63 eV, thermal stability of 10 years at 201 °C, and a resistivity contrast of approximately 10^{-4} Ω/sq between its amorphous and crystalline states [4]. The objective is to explore the atomic redistribution mechanisms, physico-chemical phenomena and crystallization process during the thermal annealing of ZnSb alloys and Zn-Sb bilayers. To this end, various samples were deposited using magnetron sputtering: deposition from an alloyed ZnSb (50:50) target, co-deposition of Zn and Sb targets with composition variations, and bilayer deposition to study reactive diffusion. *In situ* X-ray diffraction (XRD) was used to monitor phase sequences and determine crystallization temperatures as shown in Fig 1, while X-ray reflectivity (XRR) provided insights into thickness and density changes in the layers before and after thermal treatment. Additionally, atom probe tomography provided detailed insights into atomic compositions, further enriching the understanding of phase formation processes. A notable result was the consistency of the phase sequence (formation of Zn_4Sb_3 followed by ZnSb) regardless of the deposition method, although the ZnSb phase formation temperature varied depending on the method employed.

Index terms: phase change memory (PCM), ZnSb compound, phase sequence, reactive diffusion, crystallization temperatures, density changes.

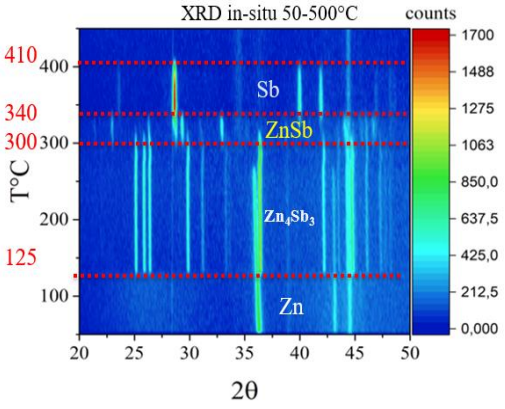

Fig 1 : *in situ* XRD recorded during ramp annealing (5°C/min) on a Zn/Sb Bi-layer. The horizontal dotte dred lines deliminate the temperature domain of each phases.

References

1. GOMIERO, E., SAMANNI, G., JASSE, J., et al. Crystallization speed in Ge-rich PCM cells as a function of process and programming conditions. IEEE Journal of the Electron Devices Society, 2019, vol. 7, p. 517-521.
2. UME, Rubab, GONG, Haibo, TOKRANOV, Vadim, et al. Electrical and structural properties of binary Ga–Sb phase change memory alloys. Journal of Applied Physics, 2022, vol. 132, no 3.
3. ZHU, Min, WU, Liangcai, RAO, Feng, et al. Uniform Ti-doped Sb2Te3 materials for high-speed phase change memory applications. Applied Physics Letters, 2014, vol. 104, no 5
4. CHEN, Yimin, WANG, Guoxiang, SHEN, Xiang, et al. Crystallization behaviors of Zn x Sb 100− x thin films for ultralong data retention phase change memory applications. CrystEngComm, 2014, vol. 16, no 5, p. 757-762.

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Crystallographic defects in orthorhombic ScSi / Si(001) contacts

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1. Introduction

Orthorhombic ScSi (COD card no. 00-000-9969, mp-9969, [1]) has been identified in the top part of lowly resistive TiN / ScSi / ScSiP / Si:P / Si(001) contact stacks showing great potential for NMOS devices [2-3]. However, little is known about its precise formation mechanism and contribution within the stack. In a previous publication [4], the analysis of X-ray diffraction (XRD) pole figures revealed that orthorhombic ScSi / Si(001), formed via solid state reaction, has an epitaxial texture with two different components having a (010) and (130) out-of-plane orientation (referred to as 'epi 1' and 'epi 2' in the following). Both components have a ScSi(002) // Si(220) in-plane alignment. Additionally, the epi 1 grains are aligned in-plane along a second independent direction: ScSi(200) // Si(220). Despite having identified these two orientations, the nanostructure and interface properties of the corresponding grains are not known. This work aims at bridging this gap by correlating the macro scale structural properties with local nano-structural inspections by cross section transmission electron microscopy (XTEM).

2. Methods

The sample consists of 10 nm TiN / 17 nm ScSi / Si(001) obtained by solid state reaction between a nominally 15 nm thick Sc thin film and a Si(001) substrate. Physical vapour deposition (PVD) is used to deposit the Sc and TiN layers. These layers are deposited without vacuum break. Prior to deposition, a wet etch in diluted HF is performed to remove the native oxide. TiN acts as a capping layer to prevent oxidation of the underlying ScSi. Following deposition, the sample is annealed in forming gas (10% H_2 in N_2) at 420°C for 20 min, resulting in the formation of orthorhombic ScSi [3]. Nano-structural inspections are carried out using XTEM. All XTEM images are taken along the Si<110> zone axis. Complementary energy dispersive X-ray spectroscopy (EDS) analysis confirms the formation of ScSi monosilicide (not shown).

3. Nano-structural analysis of orthorhombic ScSi / Si(001)

Figure 1(a) shows a large-scale bright-field transmission electron microscopy (BF-TEM) cross-section image of the stack. The Si substrate, ScSi layer and TiN layer can be clearly distinguished and are labelled for clarity. The ScSi layer is polycrystalline. Two distinct regions can be observed: region 1, containing small ($\lesssim$ 5 nm) nano-twinned grains and region 2, containing large ($\gtrsim$ 20 nm) grains that are horizontally and vertically aligned with the substrate. The orientation of the ScSi grains in these two regions is further investigated in Fig. 1 (b) – (d). Figure 1(b) shows multiple nano-twinned grains. As a result of the small size of the individual grains, a strong streaking effect can be observed in the fast Fourier transform (FFT). In between the nano-twinned regions, some larger grains can be observed (Fig. 1(c)). These grains correspond to the epi 1 texture component. Comparing Fig. 1(b) and Fig. 1(c) evidences that the nano-twinned grains correspond to epi 1 ScSi and epi 2 ScSi with their twin boundary along the (110) plane of the epi 1 grain. Indeed, the mirror image of epi 1 ScSi across the (110) plane (equivalent to a rotation of 42° about its c-axis) results in the epi 2 orientation as found in [4]. The ScSi grain shown in Fig. 1(d) also corresponds to epi 1. However, its in-plane component is rotated 90° about the b-axis compared to Fig. 1(c).

4. Crystalline defects in orthorhombic ScSi / Si(001)

The analysis outlined in the previous section reveals that the growth of ScSi along its a-axis (region 1) is associated with the formation of {110} twin defects that propagate through the full ScSi layer, resulting in a small grain size ($\lesssim$ 5 nm). The epi 2 ScSi grains are only present in this region and are twinned versions of the epi 1 ScSi. This agrees with the low peak intensity observed in XRD for the epi 2 orientation [4]. The small grain size and large defect density (roughly 1 twin defect every 1 – 5 nm) may be detrimental to the contact performance.

Finally, the growth of ScSi along its c-axis is further investigated. Figure 1(e) shows a HRTEM of the ScSi / Si interface for a ScSi grain oriented in the same way as in Fig. 1(d). The corresponding FFT image shown in Fig. 1(f) reveals the lattice mismatch between ScSi{002} and Si{220}. The alignment between these planes is visualized in the ScSi{002} / Si{220}-filtered inverse FFT shown in Fig. 1(g). The planes are epitaxially aligned across the contact interface. However, there is a misfit dislocation at the ScSi / Si interface every ~ 23rd plane. This domain-matching epitaxy [5] is expected given the large mismatch between the ScSi{002} and Si{220} interplanar spacings (Δd = 0.086 Å). Additional FFT analyses reveal that the remainder of the ScSi in this region is nearly defect free (not shown).

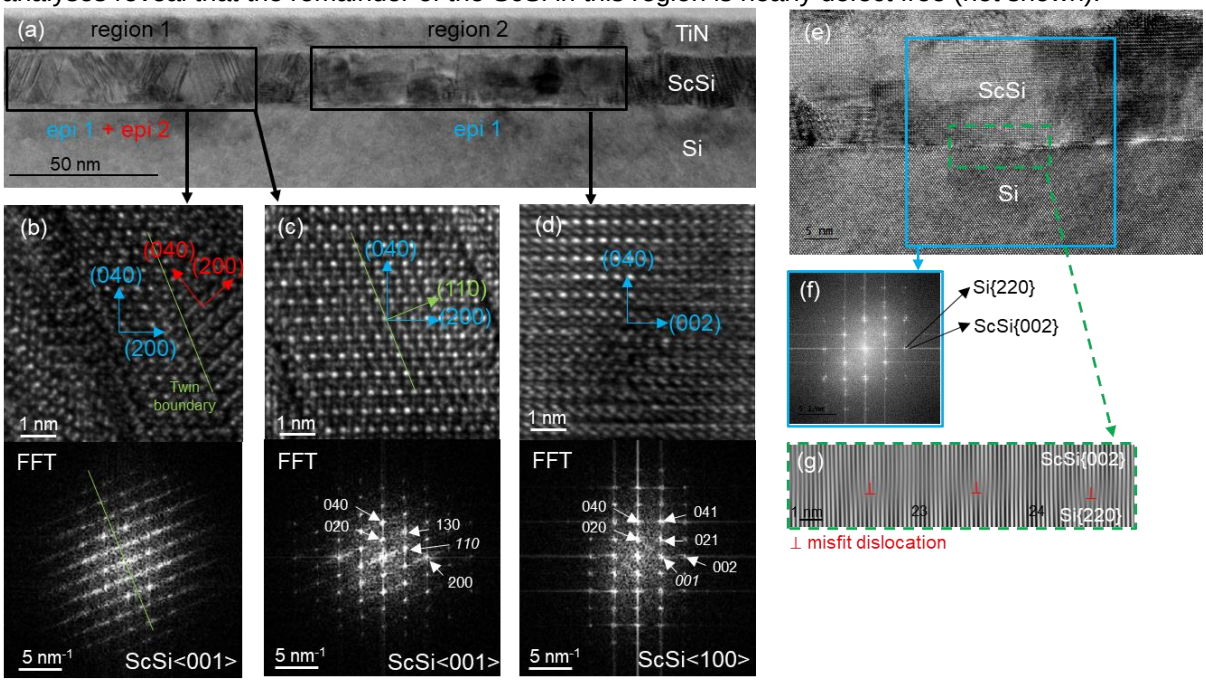

Fig. 1: (a) Large-scale BF-TEM image of a 10 nm TiN / 17 nm ScSi / Si(001) contact stack. HR-TEM images and corresponding FFTs taken in region 1 ((b) – (c)) and in region 2 (d). The FFT patterns are indexed using orthorhombic ScSi oriented along the indicated zone axis. The FFT spots indexed in italic correspond to kinematical forbidden diffraction spots. (e) HRTEM image of ScSi / Si(001), oriented according to Fig. 1(d). (f) FFT image extracted from the ScSi / Si(001) interface. (g) Corresponding ScSi{002} / Si{220} FFT filtered image.

5. Conclusions

The nanostructure and defectivity of orthorhombic ScSi / Si(001) contacts are investigated by XTEM. The analysis reveals that the growth and resulting nanostructure of ScSi is strongly anisotropic. The growth along ScSi<001> // Si<110> results in domain matched epitaxy, having a minimal defectivity limited to 1 misfit dislocation located at the contact interface every ~ 4.4 nm. The growth along ScSi<100> // Si<110> on the other hand, results in a higher density (up to ~ 1 defect / nm) of ScSi{110} twin defects, which propagate through the full ScSi layer. The former growth mechanism is expected to be preferred for optimal contact performance. Hence, it is hypothesized that a further improvement in contact resistivity could be achieved by controlling these growth mechanisms, and hence extend epi 1 grains along ScSi<100>, during the formation of orthorhombic ScSi. The origin of the growth anisotropy will be investigated as a first step to enable this.

Acknowledgements

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References

1. O. Thomas, C. S. Petersson, and F. M. D'Heurle, Appl. Surf. Sci., 53, 138 (1991).
2. C. Porret *et al.*, IEEE Int. Electron Devices Meeting, 34.1.1 (2022).
3. B. Pollefliet *et al.*, Jpn. J. Appl. Phys., 63, 02SP97 (2024).
4. B. Pollefliet *et al.*, Int. Conf. on Solid State Devices and Materials (SSDM) 2024, p. 607, PS-01-13 (2024).
5. J. Deng *et al.*, Phys. Rev. Appl. 9, 034023 (2018).

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Source/drain and silicides for nanosheet device applications

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1. Introduction

The advent of nanosheet (NS) devices generates many challenges. Source/drain (SD) epitaxy e.g. no longer proceeds from Si(001) substrates, which requires optimizing the properties of layers grown on non-{001} oriented surfaces surrounded by dielectrics (Fig. 1). Process complexities and loading effects linked to unprecedentedly high aspect ratios and device densities [1] must also be accounted for [2]. Silicide reactions and resulting phases can also be affected by varied starting surfaces and pattern dimensions [3]. These questions require systematic assessments to maintain acceptably low access resistances in scaled devices. In this regard, this contribution aims at investigating the dependency of SiGe:B SD epilayers and Ti, Mo and Sc silicide properties on substrate orientation. Sc and Mo are considered due to their excellent contact properties for N- and PMOS applications, respectively [4]. Ti is used as reference.

2. Methods

The blanket $Si_{1-x}Ge_x$:B layers discussed in this work are grown using *conventional* conditions (SiH_2Cl_2, GeH_4, and B_2H_6 at 500°C) on n-type 300 mm Si wafers. The B_2H_6 flow and deposition time are adjusted to obtain 20 nm thick $Si_{1-x}Ge_x$:B layers with nominally 60% Ge and covering the 0.1-5x10^{21} cm^{-3} chemical B concentration range. Other growth parameters remain unchanged. Silicides are formed on p-type Si wafers with relatively high resistivities (> 1 Ω.cm). After Si native oxide removal, 30 nm thick Ti, Sc and Mo films are deposited using physical vapour deposition. The layers are left uncapped to enable electrical measurements, which leads to overestimated resistivities and enlarged error bars. Some samples are annealed in different conditions including (i) forming gas (10% H_2 in N_2) sintering for 20 min at 420°C and (ii) rapid thermal annealing (RTA) for 1 min at 525 or 650°C in N_2. All layers are deposited on Si(001), Si(110) and Si(111) substrates.

3. $Si_{1-x}Ge_x$:B epitaxy on Si(001), Si(110) and Si(111) substrates

Transferring the initial $Si_{1-x}Ge_x$ process from Si(001) to alternative substrates highlights differences in surface reactions and resulting layer properties. Growth rates (not shown here) and Ge contents (x) extracted by secondary ion mass spectrometry (SIMS) (Fig. 2(a)) are indeed lower on Si(110) and Si(111) compared to Si(001), which matches trends observed in [5]. Introducing and increasing the B_2H_6 flow during growth leads to a significant increase in x on Si(110). In addition, X-ray diffraction (XRD) data shown in Fig. 2(b) indicates larger reductions in apparent Ge concentration, $[Ge]_{app}$. These reductions exceed 10% on Si(001) and Si(111) due to the incorporation of high B levels. On Si(110), the observed decrease is more limited, partly compensated by the increase in x. Fig. 3(a) eventually compares $Si_{1-x}Ge_x$:B resistivities as a function of the B_2H_6 flow used during growth. Resistivity minima are obtained for different B_2H_6 flows. Notably, resistivities are the lowest for $Si_{1-x}Ge_x$:B / Si(111), down to 1.2x10^{-4} ohm.cm. This minimum corresponds to the largest active B concentration recorded in this study. Doping activation therefore seems to be enhanced in $Si_{1-x}Ge_x$:B grown on {111} surfaces, which suggests opting for contact formation prior to SD merging.

4. Ti, Sc and Mo silicide formation on Si(001), Si(110) and Si(111) surfaces

The impact of substrate orientation on silicidation and resulting physical properties as a function of post metal deposition thermal budget is also investigated. Ti and Sc silicides are found to thicken with increasing the thermal budget on all surfaces, while Mo does not show any reaction up to 525°C (not shown here). Fig. 3(b) compares Ti, Sc and Mo silicide resistivities as a function of post metal deposition thermal budget. Annealing Ti- and Mo-based stacks generally induces an increase in material resistivity, while low temperature Sc silicidation benefits the contact electrical properties. Interestingly, the evaluated silicides do not exhibit any clear dependence on surface orientation.

5. Conclusions

The study proposes a systematic assessment of SiGe:B SD and Ti, Mo and Sc silicides deposited on Si surfaces relevant to nanosheet device applications. SiGe:B epitaxy using conventional growth conditions is affected by non Si{001} substrate orientations, which turns out being beneficial to enhance active doping in $Si_{1-x}Ge_x$:B / Si(111). On the other hand, the resistivity of silicides evaluated in this work is not affected by the starting surface. Contacting {111}-oriented $Si_{1-x}Ge_x$:B may therefore allow to improve contact performance in nanosheet devices.

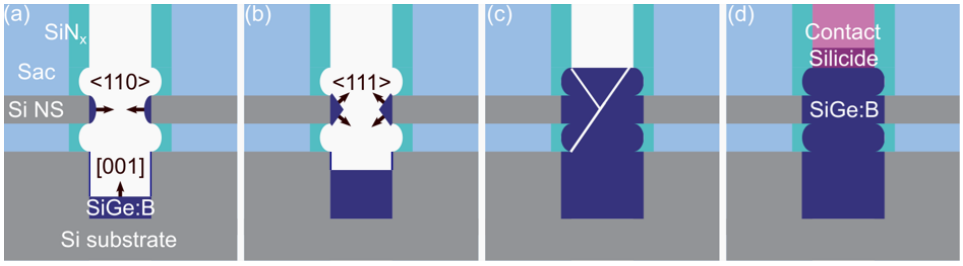

Fig. 1: Schematic representation of $Si_{1-x}Ge_x$:B source/drain-contact formation in simplified nanosheet device structures. (a) $Si_{1-x}Ge_x$:B nucleation from different surfaces, (b) formation of {111} facets, (c) merging of opposing SD possibly resulting in twin defects (white lines) and (d) contact processing and (germano)silicidation. 'Sac' stands for sacrificial layers later replaced by gates and dielectrics.

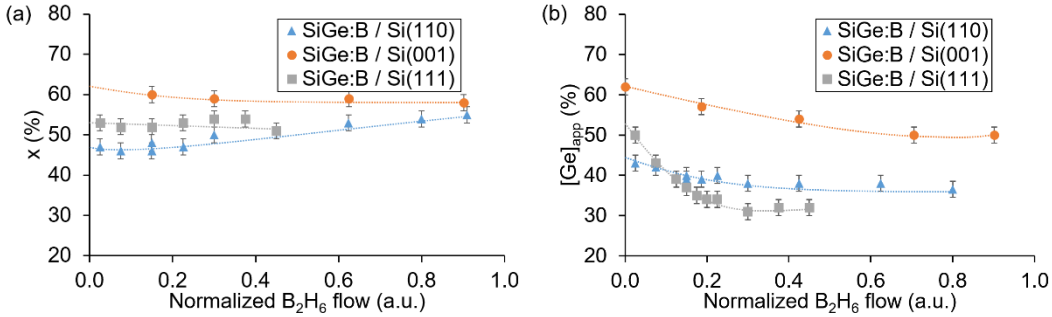

Fig. 2: Ge (a) chemical and (b) apparent concentrations in $Si_{1-x}Ge_x$:B grown on Si(001), Si(110) and Si(111) substrates, as extracted from SIMS and XRD, respectively. Apparent Ge contents obtained with XRD are lower due to B incorporation in substitutional lattice sites. Lines are guides for the eye. All B_2H_6 flows are normalized with respect to the highest flow used in this study, which is common to all curves.

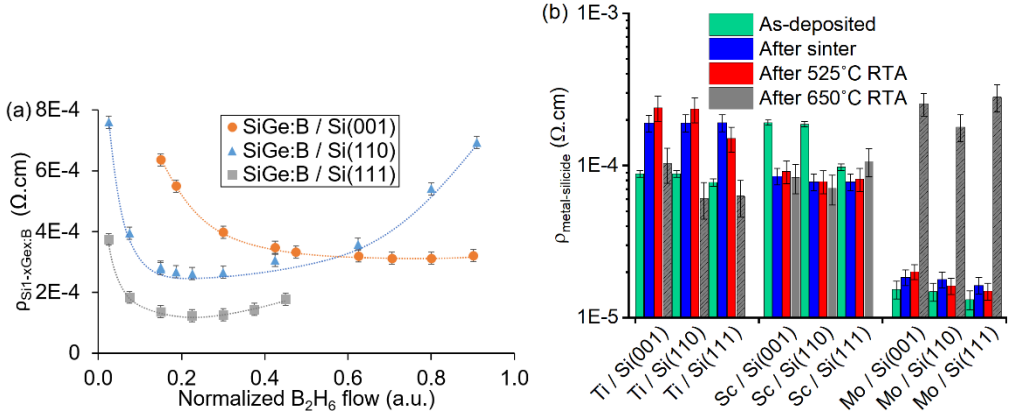

Fig. 3: (a) $Si_{1-x}Ge_x$:B resistivity curves as a function of the normalized B_2H_6 flow used during growth on Si(001), Si(110) and Si(111) substrates. Resistivity minima are obtained for different B_2H_6 flows. Lines are guides for the eye. (b) Ti, Sc and Mo silicides resistivities as a function of post metal deposition thermal budget. Data corresponding to Ti and Mo silicides after 650°C RTA (with patterned fill) assume the same thicknesses as measured after 525°C RTA, due to surface roughening preventing accurate thickness measurements, which reflects in larger error bars.

References

1. H. Mertens *et al.*, 2023 IEEE Symposium on VLSI Technology and Circuits, 1-2 (2023).
2. J. Hållstedt *et al.*, Journal of Applied Physics, 103(5), 054907 (2008).
3. H. Jeon et al., Thin Solid Films, 299, 178-182 (1997).
4. C. Porret *et al.*, 2022 International Electron Devices Meeting (IEDM), 34.1.1 (2022).
5. J.M. Hartmann *et al.*, Journal of Crystal Growth, 294(2), 288-295 (2006).

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$PtCoO_2$ delafossite oxide thin films for advanced interconnects

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The ongoing miniaturization of device densities in both logic and memory circuits necessitates a commensurate reduction in the dimensions of interconnect lines. In state-of-the-art microelectronic chips, the characteristic dimensions of interconnects are now approaching 10 nm, with future projections indicating even smaller scales. While elemental metals were initially explored as potential replacements for Cu in interconnect line metallization to enhance resistance and reliability, recent research has shifted toward binary [1] [2] [3] and ternary intermetallic compounds due to their advantageous material properties and superior performance potential.

Among the ternary candidates under investigation, delafossite oxides have emerged as promising materials for advanced interconnects. Notably, the delafossite oxide $PtCoO_2$ exhibits a bulk resistivity of just 2.1 μΩcm, lower than aluminium [4]. The structure of $PtCoO_2$ comprises alternating layers of Pt and Co cations, separated by O atoms. The Pt layers form a triangular lattice, while the Co layers reside in octahedral coordination with oxygen. This highly anisotropic material demonstrates excellent in-plane conductivity, albeit with reduced out-of-plane conductivity.

Our work has focused on the epitaxial growth of $PtCoO_2$ thin films on c-plane sapphire substrates to mitigate grain boundary scattering. As deposited films are amorphous and oxygen deficient, requiring a post-deposition annealing process at 700-800°C in an oxygen atmosphere. 2D reciprocal space mapping, conducted using a Rigaku SmartLab diffractometer, confirms the epitaxial growth of delafossite $PtCoO_2$ following annealing, with the characteristic (006) diffraction peak observed (Fig. 1a). The resultant films exhibit a (001) oriented delafossite phase. The epitaxial relationship between $PtCoO_2$ and the c-sapphire substrate is further validated by the six-fold symmetry observed in the pole figure for the (214) reflection (Fig. 1b). Platinum, a secondary phase, is also detected post annealing, consistent with a previous study [5]. Rocking curve analysis of the sample yields a full width at half maximum of 0.96°, indicative of good crystalline quality (Fig. 1c).
Transmission electron microscopy (TEM) analysis has been employed to investigate the microstructure of the delafossite oxide. As shown in Fig. 2, the layered structure of $PtCoO_2$ is clearly observed, epitaxially grown on the sapphire substrate. Fast Fourier transform (FFT) analysis reveals the crystallographic orientation relationship: $(0001)_{PtCoO2}$ // $(0001)_{Al2O3}$. However, defects and instabilities are evident in the $PtCoO_2$ layer post-annealing (Fig. 3). Observed issues include void formation (Fig. 3a), internal delamination across various film thicknesses (Fig. 3c), and Pt loss/move during annealing (Fig. 3b), even in an oxygen-rich atmosphere. These phenomena suggest a competition between crystallization and decomposition processes. Additionally, the rough interface between Al_2O_3 and $PtCoO_2$ highlights further challenges. These defects require careful analysis and optimization in future process iterations, as they indicate a narrow process window for achieving phase stability and uniform nucleation.
Despite these challenges, $PtCoO_2$ films exhibit low resistivity values ranging from 11 and 17 μΩcm at thickness of 5 to 27 nm after annealing at 800°C in oxygen atmosphere. These values position delafossite $PtCoO_2$ as a promising candidate for advanced interconnects metallization.

References

1. D. Gall, 2020 IEEE International Symposium on VLSI Technology, Systems and Applications, 112 (2020).
2. L. Chen *et al.*, J. Appl. Phys. **129**, 035301 (2021).
3. J-Ph. Soulié *et al.*, J. Appl. Phys. **136**, 171101 (2024).
4. A.P. Mackenzie, Rep. Prog. Phys. **80,** 032501 (2017).
5. D.J. Hagen *et al.*, Adv. Mater. Interfaces **9**, 2200013 (2022).

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Figure 1: XRD measurements of delafossite $PtCoO_2$ thin films

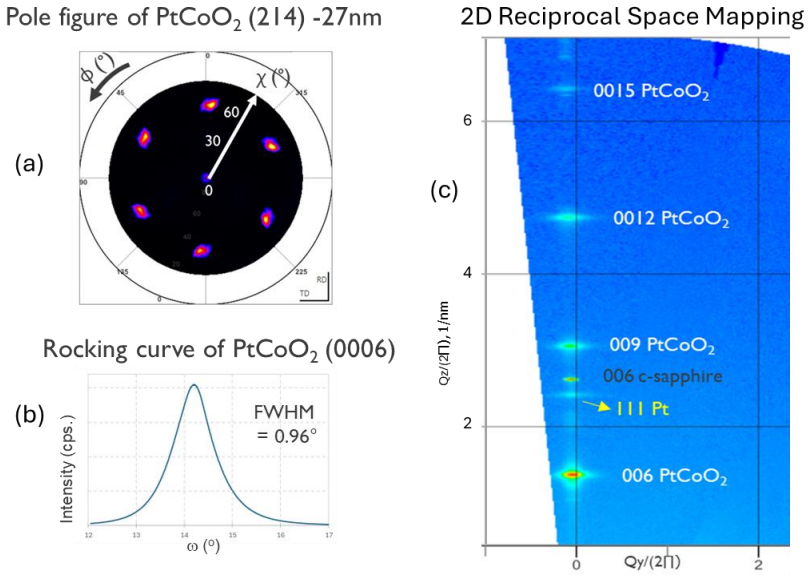


Figure 2: Cross-TEM image and Fast Fourier Transform of $PtCoO_2$ thin film

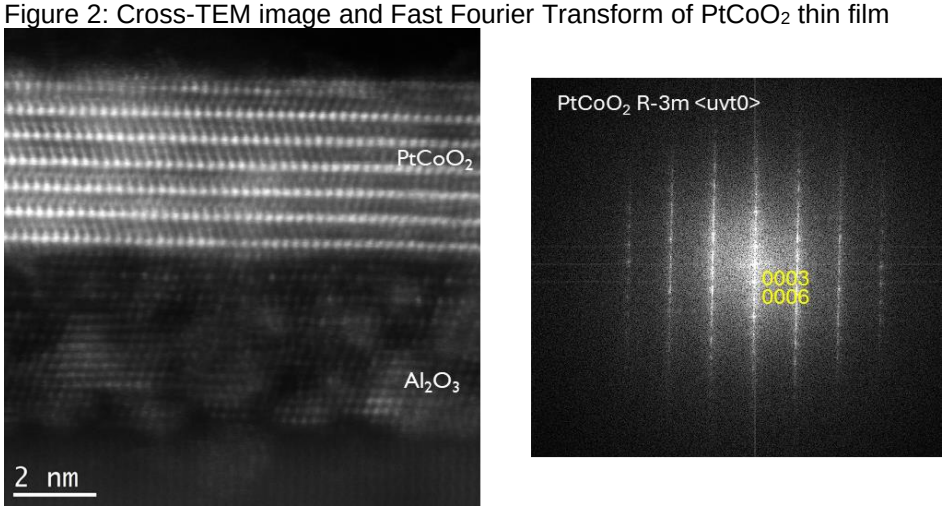
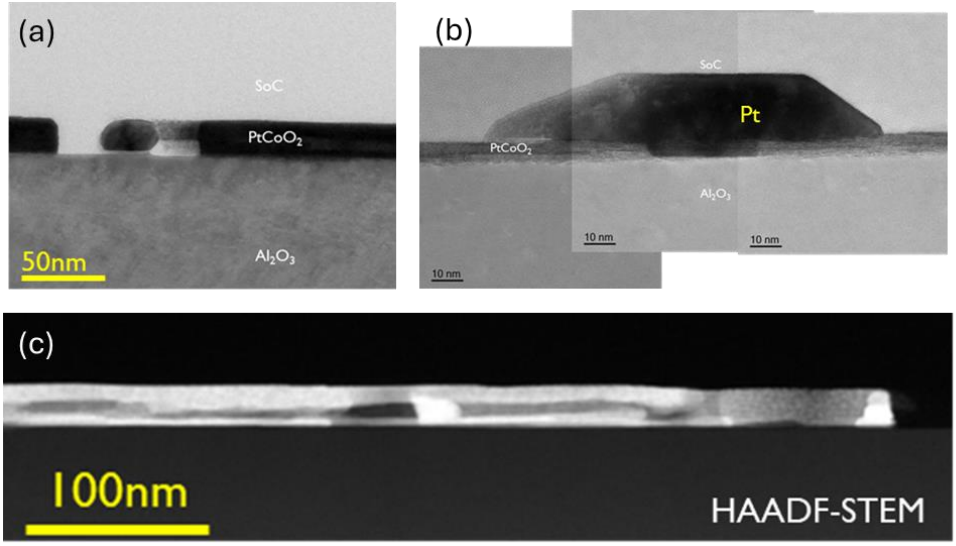


Figure 3: Defectivities seen by Cross-TEM for the $PtCoO_2$ thin films



Picking the Right TMD is the Key to Controlling Heat In a Phase Change Superlattice

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Introduction

Although phase change materials, such as GST, generally boast a low thermal conductivity in the amorphous phase, this often changes drastically upon crystallization. This is problematic as a loss of energy, due to heat diffusion into the surroundings, contributes to the high energy consumption of this novel type of memory. One promising way of tackling this high contrast in thermal conductivity, is by incorporating the phase change material into a superlattice. For example, interlacing Sb_2Te_3 with thin layers of $TiTe_2$ has proven to reduce the thermal conductivity, even in the crystalline phase. This in turn contributes to the superb performance, demonstrated by these structures [1]. TiTe2 has, by itself, a relatively high thermal conductivity, which begs the question if TiTe2 is the best choice for this application. In the search for new materials to be used in these superlattices, three alternative transition-metal ditellurides are presented: WTe_2, VTe_2 and $ZrTe_2$.

Methods

To create the different metal-ditelluride films and superlattices, magnetron sputtering is applied from elementary pure targets. Magnetrons are energized in a planetary geometry, while the substrate passes underneath. Through this way, the stoichiometry of the deposited layer can be controlled and highly crystalline materials can be achieved after anneal [2]. An automated shutter system is used to create the superlattice of Sb_2Te_3 and the different MTe_2 candidates. Thermal conductivity is measured using time-domain thermoreflectance (TDTR), a laser-based pump probe technique that can directly probes the thermal response of a system of thin-films. Samples are covered with a 80nm Ru transducer. The transducer turns the power of the laser into heat (pump), while its reflectivity acts as an indicator of the surface temperature (probe) [3].

Structural Characterization

The three materials show little to no crystallinity right after deposition. While both VTe_2 and $ZrTe_2$ crystallize upon anneal, we were not able to crystallize WTe_2. For this reason, we focus solely on the first two materials. After an anneal to 300°C, both materials crystallize into a highly textured CdI_2 structure with 00L planes parallel to the Si substrate. This can be seen in the rocking curve and XRD data shown in Fig. 1. A sample containing 80nm VTe_2 is shown on the left, the right side shows a 5nm Sb_2Te_3 / 3nm $ZrTe_2$ superlattice. Peaks of both materials are present in the superlattice, next to satellite peaks that are a result of the superlattice structure.

Thermal Conductivity Results

A room-temperature study of all three candidate materials is first performed. Creating a thickness series allows us to extrapolate-out interface resistances and reveal the intrinsic thermal conductivity of the materials. An example of this analysis for $ZrTe_2$ is shown on the left of Fig. 2. On the right, a comparison is made between the three candidate materials, $TiTe_2$ and Sb_2Te_3. All three candidates have very little contrast between the two states, with $ZrTe_2$ displaying the lowest thermal conductivity. To characterize $ZrTe_2$ even further, an in situ study is performed, results can be seen in Fig. 3. After crystallization, the thermal conductivity for $ZrTe_2$ stays under that of Sb_2Te_3, which is exactly what is wanted for a good superlattice. A 5nm Sb_2Te_3 / 3nm $ZrTe_2$ superlattice displays a consistently low thermal conductivity all the way up to 450°C..

Conclusions

Both VTe_2 and $ZrTe_2$ make promising candidates for use in PCM superlattices due to their high crystalline quality, thermal stability and consistently low thermal conductivity contrast. On top of this, $ZrTe_2$ and its superlattice demonstrate a low thermal conductivity, even at high temperatures, making it a prime candidate for further investigations.

References

1. K. Ding et al., Science **366**, 210 (2019)
2. M. Noh et al., Science **270**, 1181 (1995)
3. D. G. Cahill, Rev. Sci. Instrum. **75**, 12 (2004)

[*] *corresponding author e-mail:* Seppe.VanDyck@UGent.be

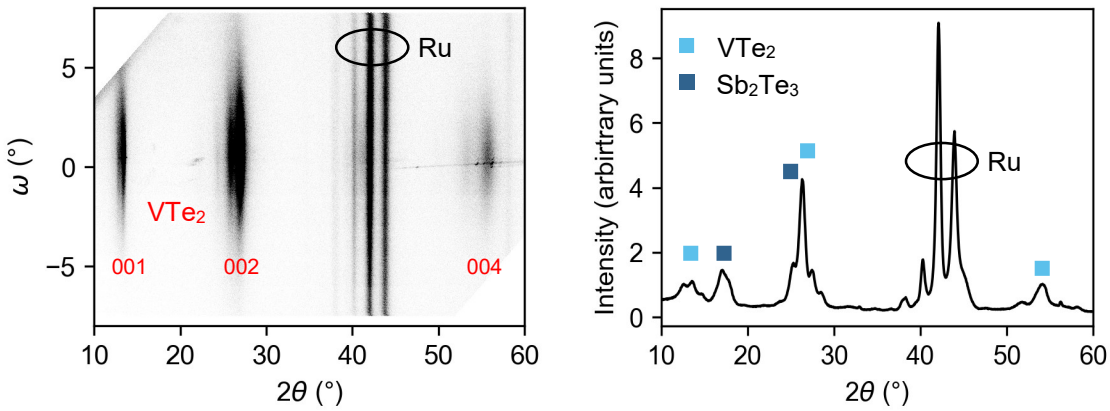

Figure 1. (left) XRD and rocking curve data show the high quality and structure of sputtered VTe_2 after an anneal to 450°C. The 80nm ruthenium transducer layer is also visible. **(right)** XRD data for the VTe_2 /Sb_2Te_3 superlattice shows that both phases are present in the superlattice. The visible satellite peaks indicate an ordered superlattice structure.

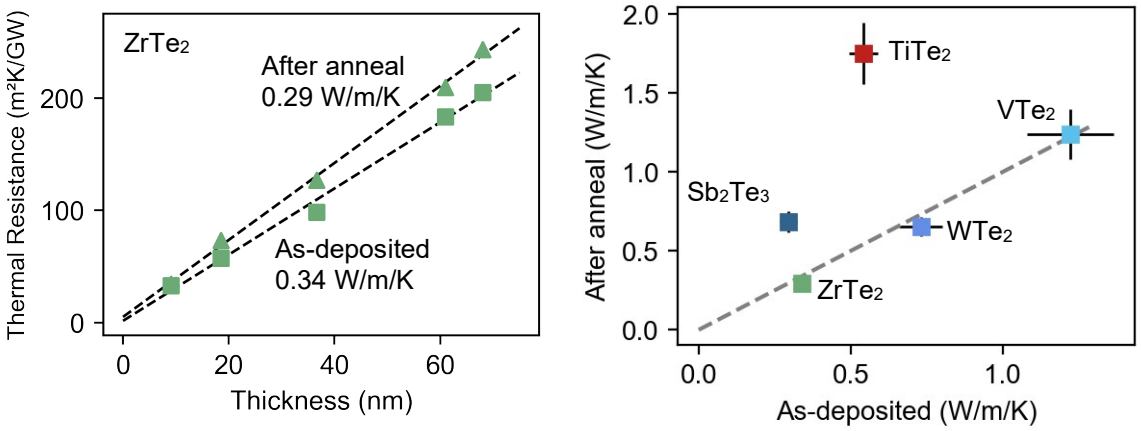

Figure 2. (left) Creating a thickness series of the same material, allows us to calculate the intrinsic thermal conductivity of the materials. Shown is the data for $ZrTe_2$ between 10 and 80 nm. **(right)** All three materials show a very low contrast in thermal conductivity. They lie close to dashed line, which signifies zero contrast.

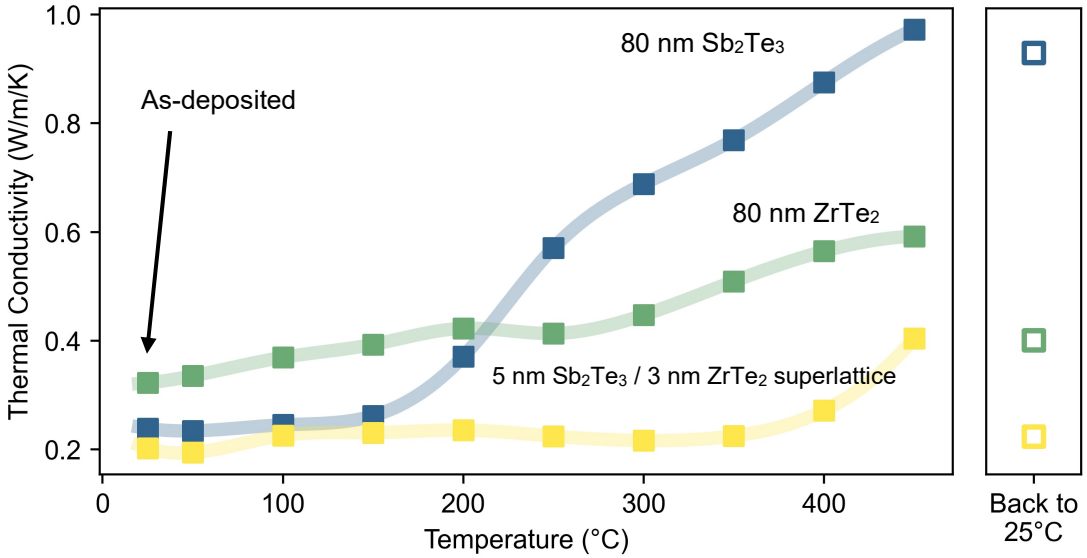

Figure 5 At high temperatures the thermal conductivity of $ZrTe_2$ only increases slightly, while that of Sb_2Te_3 increases drastically. The superlattice with 16 periods of these materials performs very well in the studied temperature range.

Surface Analysis of SiO_2 for Die-to-Wafer Hybrid Bonding

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Advanced packaging and chiplet integration are being explored as an alternative integration scheme for achieving higher yield, density and energy efficiency[1]. A key technology required for advanced node chiplet is die-to-wafer (D2W) hybrid bonding. The bonding quality, i.e. bond strength, is a critical factor in ensuring the robustness of subsequent processes. In wafer level hybrid bonding, the bonding dynamics and bonding surface are well-controlled since the cluster system of wafer bonding equipments are available in mass-production[2,3]. However, the understanding of "D2W" bonding dynamics and the surface state after plasma activation is insufficient since the die bonder for D2W hybrid bonding is still not fully commercialized. Furthermore, the lack of the quantitative and robust bond strength measurement method for D2W bonding makes characterization of surface more challenging. In this study, the investigation of bonding surface is executed for die level hybrid bonding. In particular, the surface state before and after plasma activation was deeply analyzed. In addition, the bond strength measurements by nanoindentation (NI) were used to measure bonding energy[4].

A 300 mm silicon wafer is used for the origin of the substrates. A Si dioxide (SiO_2) layer with 100 nm thickness was used as the bonding interface. Fig. 1 provides an image of the sample structure used in this study. The D2W bonding process was executed using an optimized top bonding head and non-contact die transfer system. NI test, typically used for measuring Young's modulus and hardness of the materials, was employed to measure bonding energy. As shown in Fig. 2(a), a sample was prepared by completely removing the upper silicon substrate to expose the bonding film. Indentation was then performed vertically on this exposed bonding layer, introducing delamination around the indentation (Fig. 2(b)). The size of the delaminated region was used to calculate the bonding energy.

Fig. 3 shows the relationship between bonding energy and PBA temperature. The measured bonding energy on D2W samples showed equivalent value range for the W2W samples. Therefore, the NI method is applicable for D2W bonding interface. It is observed that as the PBA temperature increases, the bonding energy also increases linearly. The amount of water desorbed from surface of SiO_2 with increasing temperature was evaluated by TDS (see Fig.4). The results revealed that higher temperatures led to greater surface water release. These results suggest that higher PBA temperatures increase water supply to the bonding interface. Furthermore, we propose a model shown in Fig. 5 by integrating the results from Fig. 3 and Fig. 4. This model indicates the state of the bonding interface at various PBA temperatures and suggests that higher annealing temperatures result in more water release from the film, leading to an increased supply of water to the bonding interface. The water fills the minute gaps at the bonding interface, thereby increasing the contact area between the upper and lower films. As a result, this process enhances the bond strength[5]. This suggests that the amount of water present at the bonding interface plays a critical role in the bond strength of hybrid bonding. it will be necessary to develop D2W bonding processes that take this factor into account.

From these results, the relationship between PBA, water content at the bonding interface, and bond strength in hybrid bonding has been clarified. These findings are expected to accelerate the research and development of hybrid bonding for future chiplet integration.

References

1. Debendra Das Sharma "Universal Chiplet Express (UCIe)® : Building an open chiplet ecosystem" 2022.
2. J. H. Lau, "Recent Advances and Trends in Advanced Packaging," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 2, pp. 228–252, 2022.
3. Fumihiro Inoue et al., "Area-Selective Electroless Deposition of Cu for Hybrid Bonding", IEEE Electron Device Letters, Volume 42, Isuue 12, P1826-1829, 2021.
4. Y. Yoshihara et al., "In-Depth Analysis of Bonding Interface at Die Level Hybrid Bonding," 2024 International Conference on Electronics Packaging (ICEP), Toyama, Japan, pp. 3-4, 2024.
5. F. Fournel et al., "Water Stress Corrosion in Bonded Structures," 2015 ECS J. Solid State Sci. Technol. 4 P124, 2015.

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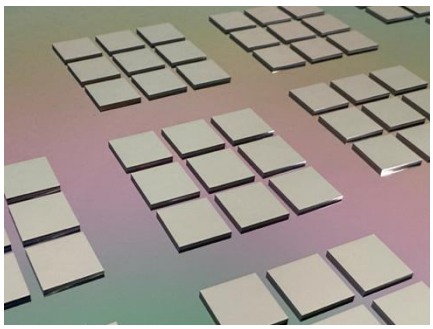

Fig. 1. Image of D2W sample.

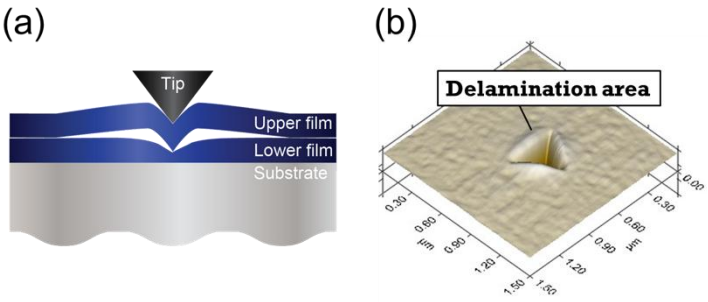

Fig. 2. Delamination behavior with Nanoindentation test (a) schematic illustration, and (b) 3D image.

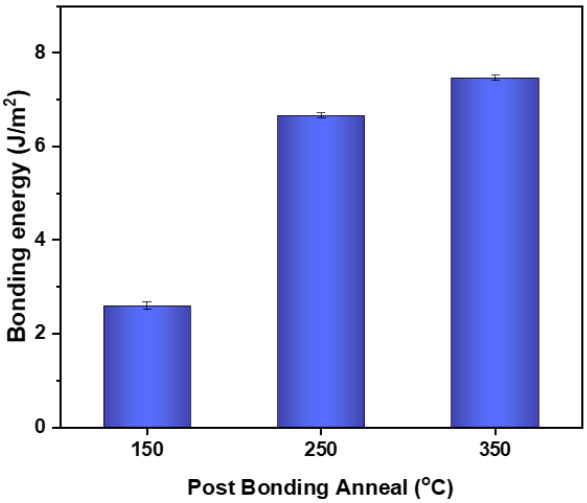

Fig. 3. Transition of bonding energy with post bonding anneal temperature.

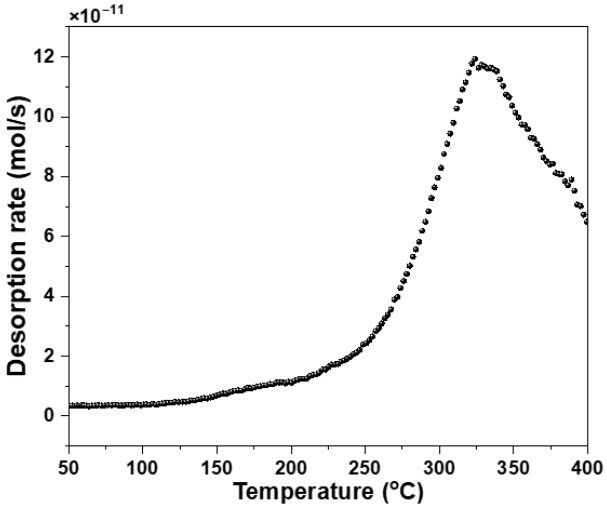

Fig. 4. TDS spectra of mass number of 18 M/e (water) for SiO_2.

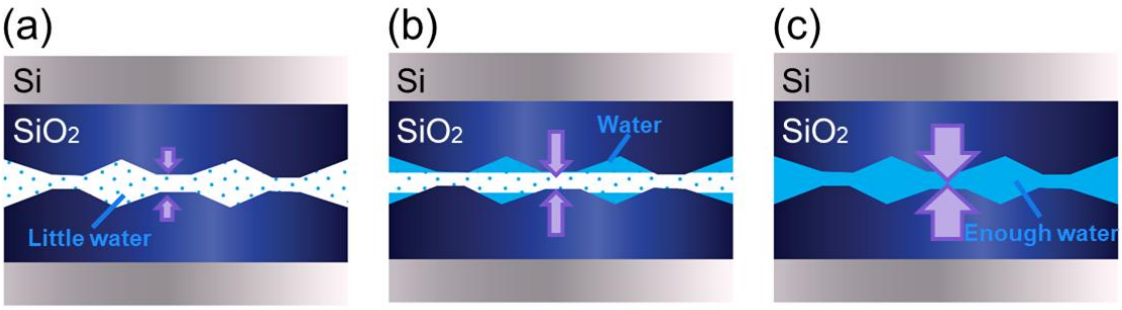

Fig. 5. Water content at the bonding interface during annealing at (a) 150 degrees, (b) 250 degrees, and (c) 350 degrees.

Analytical evaluation of the interface states on SiO_2/4H-SiC n-type MOS Capacitor

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The increasing adoption of silicon carbide (SiC) in power devices is justified by its superior properties compared to the already established and widely used silicon (Si). The ability to operate at high temperatures and its high breakdown voltage make it a key material in the transition to systems requiring high efficiency and high power [1]. Although several generations of SiC devices are commercially available today, this technology is far from mature.

Indeed, the metal-oxide-semiconductor (MOS) interface of SiC, a critical component in MOSFET devices, still demands extensive investigation compared to Si. The interface traps (D_{it}) formed during device manufacturing are significantly higher in SiC-MOSFETs than in their silicon counterparts [2]. These traps affect the channel mobility, threshold voltage, and reliability, ultimately impacting the electrical properties of the device [3]. Understanding the influence of oxide/semiconductor interface traps on channel activation is therefore essential for advancing SiC-based MOSFETs. The high D_{it} in SiC remains a key challenge, as it leads to variations in channel mobility and compromises the device's final electrical performance.

To determine the impact of those traps on the activation of the device and, consequently, on the capacitance-voltage (C-V) characteristic curve of the MOS region in the gate of a MOSFET, the analysis was limited to the MOS interface, using a MOS capacitor as an approximation. An analytical approach was employed without the use of TCAD simulators, taking as reference a nitrogen doped n-type MOS capacitor with a semiconductor doping concentration of $7.8 \cdot 10^{15}\,cm^{-3}$, a silicon oxide layer with a thickness of 45 nm and a metal with a work function of 4.05 eV relative to the vacuum energy level. This value corresponds to the typical poly-Si work function used in MOSFETs. The advantage of using a metallic contact with a specific work function is that it eliminates potential depletion effects of poly-Si, which can appear in the C-V curve of the device in the inversion region, allowing the focus of the study to remain solely on the effects of interface traps.

A detailed analytical model that include distributed and discrete interface levels will be presented in order to fit the experimental data collected on MOS capacitors.

Figure 1 shows the ideal curve of the MOS capacitor mentioned above, where a significant discrepancy is observed, particularly in the shift of the two curves caused by the presence of fixed charges in the oxide near the oxide/semiconductor interface. Figure 2, in fact, depicts a C-V curve that includes the component related to the fixed charges we calculated, approximately $1 \cdot 10^{12}\,cm^{-2}$, which shifts the curve towards negative voltage values. Finally, the introduction of interface traps, whose profile is shown in Figure 3, causes a change in the slope of the C-V curve in Figure 4. To generate the trap profile, two distinct trap distributions were used and summed, taking into account the trends of the D_{it} tabulated in the literature [4,5]: an acceptor trap profile with an exponential distribution, a maximum concentration of $3 \cdot 10^{12}\,cm{-}2\,eV^{-1}$, starting from the conduction band energy level and decreasing exponentially with a sigma of 0.18; and a Gaussian profile centred 0.45 eV below the conduction band, with a maximum concentration of $1.5 \cdot 10^{11}\,cm^{-2}\,eV^{-1}$ and a sigma of 0.2.

Although this is a preliminary study on the calculation of interface traps, the development of a mathematical model capable of accurately predicting the final shape of the C-V curve of a MOSCap represents a fundamental step toward its application as a model for the channel region in a MOSFET. This approach will enable the separation of the contributions of individual capacitive components and a more in-depth investigation into the role these traps play in altering channel mobility.

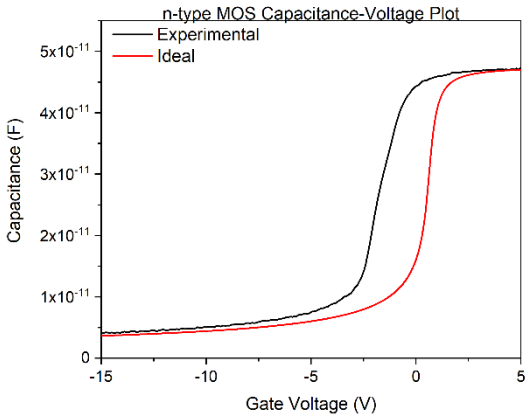

Figure 2: Capacitance-Voltage Plot of experimental n-type MOS compared with simulated curve

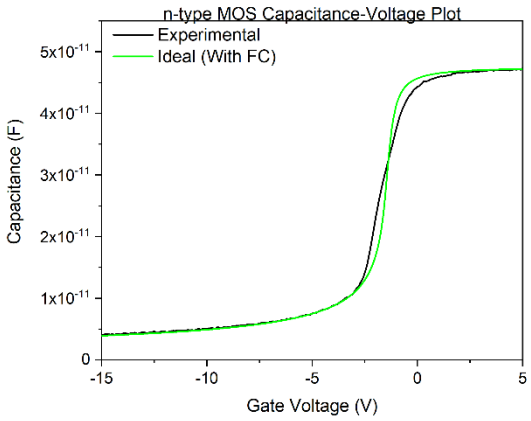

Figure 1: Capacitance-Voltage Plot of experimental n-type MOS compared with simulated curve (FixedCharge were added)

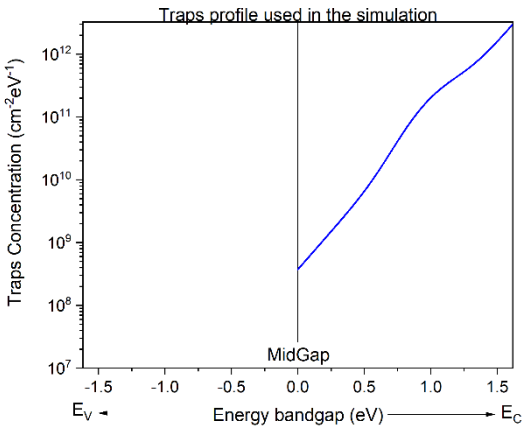

Figure 3: Interface traps used for the simulation of the final curve plotted in figure 4

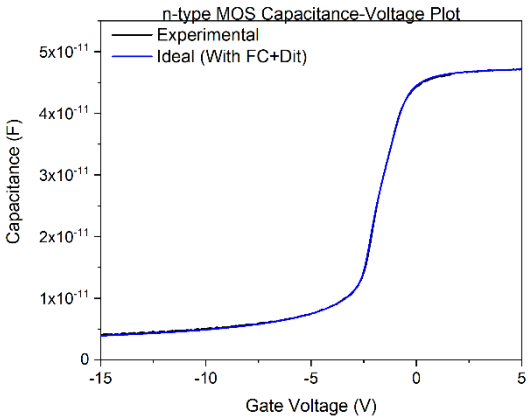

Figure 4: Capacitance-Voltage Plot of experimental n-type MOS compared with simulated curve (FixedCharge and Dit were added)

References

[1] Tsunenobu Kimoto, 2016, "Bulk and epitaxial growth of silicon carbide", Progress in Crystal Growth and Characterization of Materials, Volume 62, Issue 2.

[2] Pantelides, S.T., Wang, S., Franceschetti, A., Buczko, R., Di Ventra, M., Rashkeev, S.N., Tsetseris, L., Evans, M.H., Batyrev, I.G., Feldman, L.C., Dhar, S., McDonald, K., Weller, R.A., Schrimpf, R.D., Fleetwood, D.M., Zhou, X.J., Williams, J.R., Tin, C.C., Chung, G.Y., Isaacs-Smith, T., Wang, S.R., Pennycook, S.J., Duscher, G., Van Benthem, K., Porter, L.M., 2006, "Si/SiO2 and SiC/SiO2 Interfaces for MOSFETs – Challenges and Advances", MSF.

[3] Fiorenza, P., Giannazzo, F., & Roccaforte, F., 2019, "Characterization of SiO2/4H-SiC interfaces in 4H-SiC MOSFETs: a review", Energies, 12(12), 2310.

[4] Potbhare, S., Goldsman, N., Pennington, G., Lelis, A., & McGarrity, J. M., 2006, "Numerical and experimental characterization of 4H-silicon carbide lateral metal-oxide-semiconductor field-effect transistor", *Journal of Applied Physics*, *100*(4).

[5] Maresca, L., Matacena, I., Riccio, M., Irace, A., Breglio, G., Daliento, S., 2020, "TCAD model calibration for the SiC/SiO 2 interface trap distribution of a planar SiC MOSFET", In *2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)* (pp. 1-5), IEEE.

Atomic layer etching of nickel aluminide binary intermetallic using a super-cycle sequence based on Hhfac and $Al(CH_3)_3$

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Nickel aluminide (NiAl, Ni_3Al) binary intermetallics have garnered significant interest as potential materials for next-generation barrier-less interconnects and extreme ultraviolet (EUV) mask absorbers, owing to their lower resistivity compared to conventional metals[1] and superior optical properties[2]. However, their high chemical stability and low gas-phase volatility present substantial challenges in developing a precise and controllable etching process. In this work, we introduce a super-cycle atomic layer etching (ALE) approach tailored for the selective and compositionally stable etching of NiAl-based intermetallics. The ALE process consists of two alternating sub-cycles: (1) a nitrogen/hydrogen (N_2/H_2) plasma exposure step, which modifies the Ni surface, followed by hexafluoroacetylacetone (Hhfac) vapor exposure to facilitate the removal of Ni, and (2) an SF_6 plasma activation step coupled with trimethyl-aluminum (TMA) exposure to selectively etch Al. By optimizing the exposure duration for each sub-cycle, we achieve precise control over the etching of different nickel aluminide phases, including NiAl and Ni_3Al.

A comprehensive characterization of the ALE process was performed using in-situ spectroscopic ellipsometry to monitor thickness variations and self-limiting behavior. X-ray reflectivity measurements confirmed tunable etch rates ranging from 0.5 ± 0.10 Å/super-cycle at 250°C to 3.3 ± 0.23 Å/super-cycle at 350°C. Additionally, atomic force microscopy (AFM) analysis demonstrated that the surface remains smooth throughout the etching process, with only minor roughness observed after extended cycles. X-ray photoelectron spectroscopy (XPS) further confirmed that the elemental composition of the Ni aluminide alloys is preserved after etching.

This work presents a novel ALE strategy for Ni aluminides, offering a promising pathway for the precise patterning of these intermetallics in advanced semiconductor fabrication. The ability to maintain composition control and surface smoothness makes this process a strong candidate for future applications in high-performance interconnects and EUV lithography mask technology.

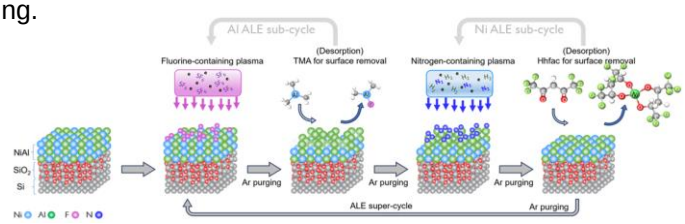

Figure 1. General reaction scheme of one complete super-cycle isotropic plasma atomic layer etching of nickel aluminide binary intermetallic.

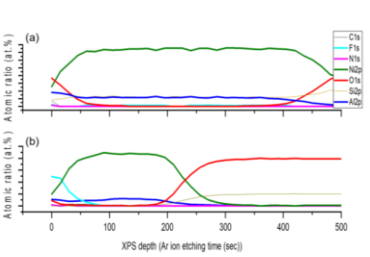

Figure 2. XPS depth profile of NiAl films (a) pristine sample (b) after etching by 20 super-cycles.

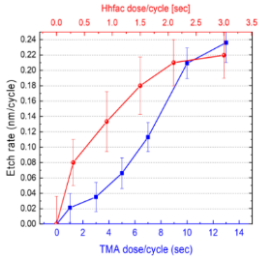

Figure 3. Dependency of etch rate of pure Ni and Al on Hhfac and TMA exposure time/cycle, respectively.

References

1. Soulié, Jean-Philippe, et. al. "Reduced resistivity of NiAl by backthinning for advanced interconnect metallization." 2023 IEEE International Interconnect Technology Conference (IITC) and IEEE Materials for Advanced Metallization Conference (MAM)(IITC/MAM). IEEE, 2023.
2. Luong, Vu, et. al. “Ni-Al alloys as alternative EUV mask absorber.” Applied Sciences 8.4:521 (2018).

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Fluorine doping of barium bismuthate for topological qubits

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Quantum computing promises to greatly decrease the time required to solve problems that benefit from parallel computation, with applications in many different fields such as cryptography, machine learning, logistics or drug development. At the core of a quantum computer there are the qubits, systems in which a superposition of two states can be precisely prepared and manipulated. In the literature many different proposals for physically realizing a qubit can be found, each one with its own advantages and disadvantages. Among them, we can find topological qubits. Instead of being based on a two-level system like most of the other qubits, topological qubits would use the physical braiding of non-abelian anyons, particles that pick up a phase shift different than π or 2π when exchanged, to execute quantum computations. In this way, the impact of the major obstacle to quantum devices, the decoherence of the qubits due to their interaction with the environment, could be drastically decreased [1]. Theoretically, one approach to realize topological qubits is through the deposition of superconductive (SC) islands on a topologically insulating (TI) continuous film. [2]

A very promising material for this approach is barium bismuthate ($BaBiO_3$, BBO), a perovskite expected to behave both as a SC and a TI, depending on the doping, allowing the realization of high-quality SC-TI heterostructures. In particular, p-doped BBO is a well-known SC with a critical temperature up to 30K [3], while n-doped BBO (*e.g.* by substituting the oxygen with fluorine atoms), is expected by ab-initio DFT to be a TI [4]. Furthermore, the topological bandgap of BBO is expected to be around 0.7 eV [4], higher than the other TIs extensively studied in the literature like Bi_2Se_3, Bi_2Te_3 or Bi_xSb_{1-x} [5], further improving the quality of a BBO based-topological qubit.

Despite its potential, the realization of a TI BBO is still an open question in the literature. Here we report our attempts at introducing fluorine into the structure of 20nm-thick MBE-grown epitaxial BBO thin films on grown on Si (001) through an STO buffer layer. From the literature, we expected oxygen deficient perovskites to be more efficiently fluorinated [6], thus, we also investigated the effect of the process on oxygen deficient films. As fluorinating agent, we chose plasma of a gas commonly found in semiconductor facilities: SF_6.

After finding processing conditions for which the film' integrity is conserved, we studied the effect on crystallinity by XRD and composition by XPS and SIMS. By XRD we were able to assess an increase in the out-of-plane lattice parameter in the BBO samples. By XPS, a clearly visible F 1s core level peak, with a component compatible with the formation of a metal fluoride was detected. Finally, SIMS investigation allowed us to further confirm an increase of fluorine into the processed samples coupled to a decrease in oxygen concentration. In SIMS data we also saw a higher concentration of fluorine in the oxygen deficient samples, confirming our initial hypothesis. All these results seem to indicate at least a partial substitution of oxygen with fluorine in the BBO samples. We also performed a second anneal in oxygen on some of the fluorine samples and observed an increase in crystallinity and a decrease in the lattice parameter by XRD, suggesting a partial reversibility in the process.

In the future a more detailed investigation on the structure by TEM and an investigation of the impact on the transport properties will be carried out.

References

1. S. Das Sarma, M. Freedman, and C. Nayak, Phys. Rev. Lett. 94, 166802 (2005)
2. L. Fu and C. L. Kane, Phys. Rev. Lett. 100, 096407 (2008)
3. H. Yamamoto, K. Aoki, A. Tsukada, and M. Naito, Physica C 412-414, 192 (2004)
4. B. Yan, M. Jansen, and C. Felser, Nat. Phys. 9, 709 (2013)
5. J. Yun and L Xi, Adv. Quantum Technol. 7, 2400041 (2024)
6. O. Clemens and P. R. Slater, Rev Inorg Chem, 33, 105 (2013)

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Kinetics of Phase Formation in Ni-Co-Si Ternary system using Bilayer and Alloyed thin films

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From 5G to automotive tech, next-generation microelectronic circuits hinge on high-performance nanometric MOS transistors. Central to these devices are silicides of Co and Ni, which are essential for creating low-resistance contacts that ensure optimal functionality and elevate semiconductor performance [1]. These contacts are obtained by solid state reaction between a metal film and the Si substrate. This study explores the phase formation kinetics in thin films of Ni and Co silicides, with a focus on the ternary Ni-Co-Si system. By integrating in situ experimental techniques and computational simulations, this work explores the relationship between phase formation, metal distribution, and the Ni-Co-Si phase diagram under thermal annealing conditions.

Bilayer thin films with varying Ni and Co thicknesses and as well as the corresponding alloys films (figure 1), were thermally annealed under different conditions to study the sequences of phases and kinetics of phase formation. After cleaning the silicon substrate, Co and Ni bilayer and alloys films were deposited using magnetron sputtering using Co and Ni targets. In situ X-ray diffraction (XRD) was employed to observe real-time phase evolution during step annealing with increasing temperatures, complemented by isothermal XRD annealing for detailed phase transition analysis. Resistance measurements were also conducted to observe the changes in electrical properties as the silicides formed. To understand the atomic-scale distribution of nickel and cobalt during phase formation, atom probe tomography (APT) was utilized. APT provided high-resolution, three-dimensional maps of the elemental distribution.

The results (figure 2) show that nickel significantly influences the formation temperatures of CoSi and MSi_2 phases, accelerating their growth. The diffusion of nickel occurs faster than cobalt, consistent with theoretical expectations. In bilayer films, the simultaneous growth of NiSi and CoSi phases was observed, notably when the nickel concentration exceeded 25%, which agrees with phase diagram predictions. Additionally, the study highlights the role of film composition and thickness in tuning phase transitions and silicide stability. The formation temperature of the M_2Si phase varies based on the initial layer in contact with silicon (figure 3). The M2Si formation temperature is ~280°C when nickel contacts silicon but increases with cobalt thickness when the Co layer is in contact with Si, confirming Co layer as a diffusion barrier. Higher cobalt concentrations also raise the temperature for complete M2Si consumption. These results can be described using the ternary phase diagram (Figure 4). This research gives valuable insights into silicide formation mechanisms and their impact on device performance, contributing a new path for optimizing contact materials in advanced microelectronic circuits.

References

1. D. Mangelinck, The Growth of Silicides and Germanides, Handbook of Solid-State Diffusion, 2017.
2. Mangelinck, D, 2019. Mechanisms of silicide formation by reactive diffusion in thin films. *Diffusion foundations*, *21*, pp.1-28.

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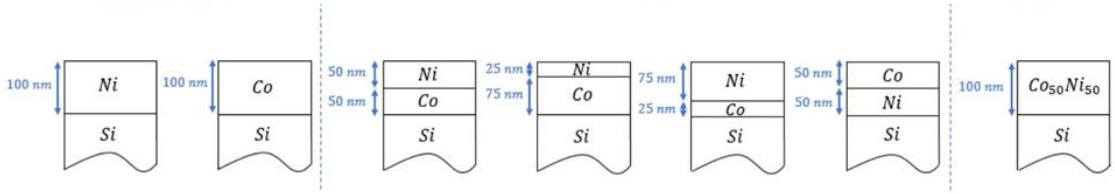

Figure1. Schematic representation of samples analyzed

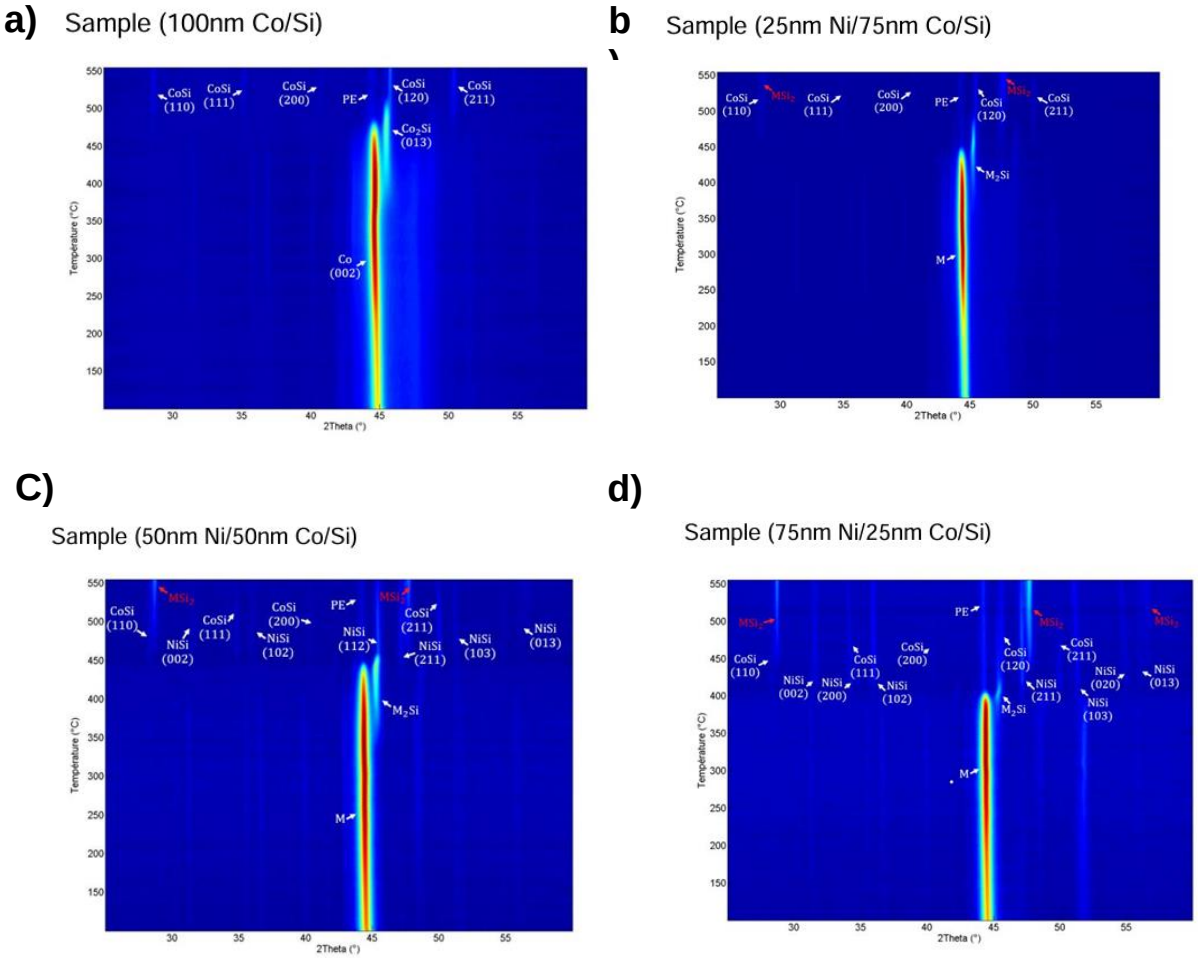

Figure 2. In situ XRD patterns for the bilayer samples

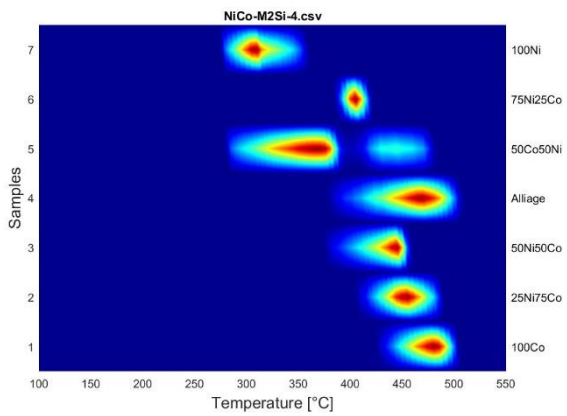

Figure 3. Comparative kinetics of the M2Si phase in the different samples

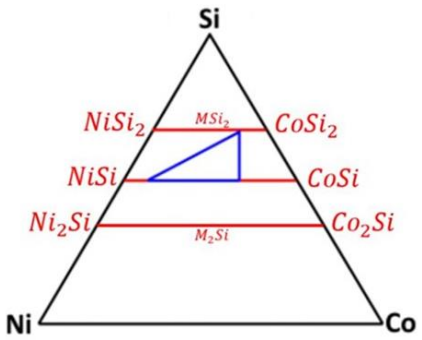

Figure 4. calculated Co-Ni-Si ternary phase diagram at 400^{0}C for thin film reaction. The equilibrium between CoSi, NiSi, and MSi_2 is drawn in blue

E-beam defectivity analysis of metal filled vias to determine yield of EUV lithography processes

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In this work we demonstrate a method to use metal fill process combined with voltage contrast SEM imaging to determine the yield of a via lithography process. In this method vias are formed with a CAR photo-resist using EUV lithography on both 0.33NA (NXE 3400) and 0.55NA (EXE 5000) and etched into a patterning stack containing a Ti base metal plate. In an ideal case, where both the lithography and etch are processed correctly, the via lands on the Ti base metal plate and a bright circular image is observed after metal fill. However, if defect occurs during these processes, the via may not land on the Ti base metal plate and a grey or black image is seen and a defect is identified. Using high NA (0.55NA) lithography CD-SEM images show a defect-free random vias pattern with a centre-to-centre (C2C) distance of 29.7nm.

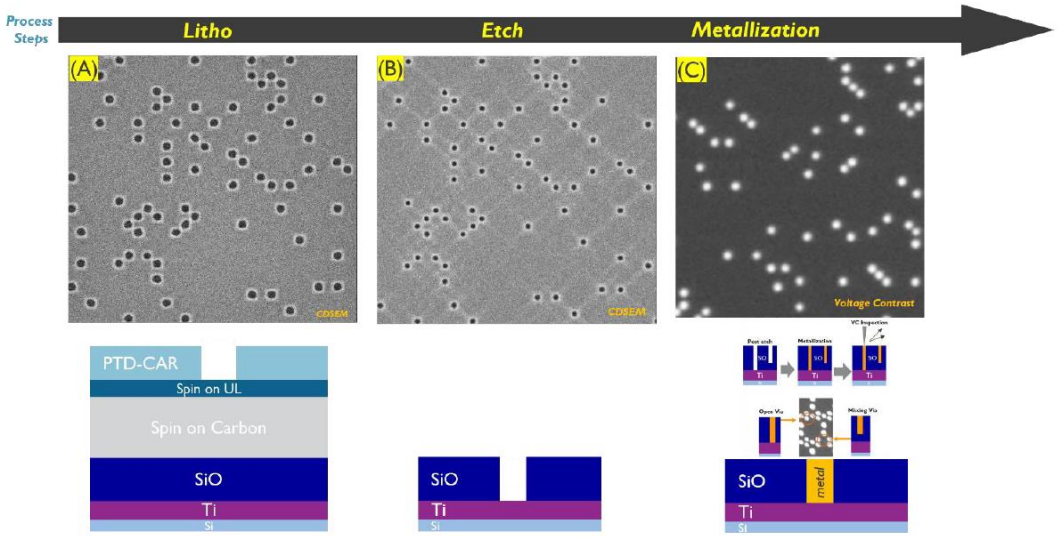

Figure 1: ***Baseline Process flow for random logic via***. (A) LNA EUV lithography and top-down CDSEM image. (B) Etch shrink showing defect free CD. (C) Voltage Contrast metrology principle and read out.

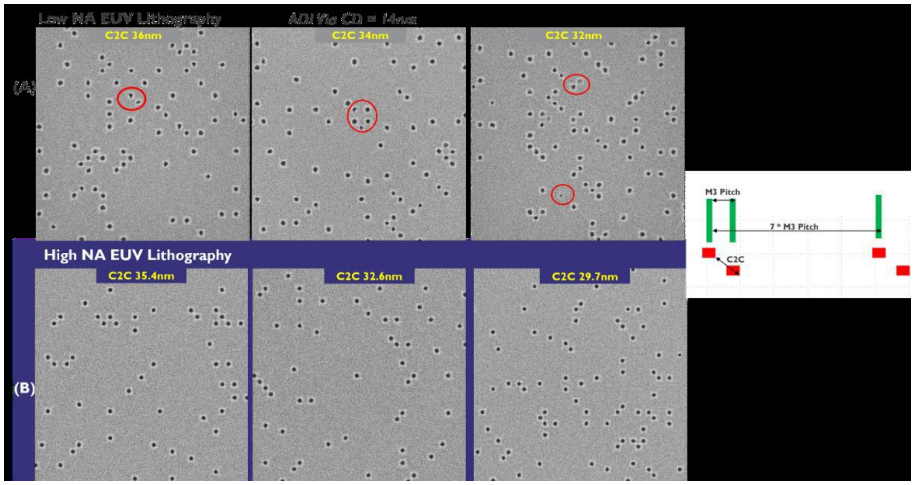

Figure 2: Comparison of Low NA EUV Lithography vs. High NA EUV Lithography. (A) At LNA, it is challenging to print defect-free via CD = 14nm and below. The red circles indicate the defects. (B) The bottom images are from High NA EUV lithography, showing zero defects even for smallest center-to-center distance of vias. The right image explains the alignment of the C2C distance of vias to the respective metal layers.

References

1. L. Tan, W. Gillijns, J. Lee, D. Xu, J. Kerkhove, V. Philipsen, R. Ki, " EUV low-n attenuated phase-shift mask on random logic Via single patterning at pitch 36nm", Proc. SPIE 12051, Optical and EUV Nanolithography 2022, 120510P (2022) https://doi.org/10.1117/12.2614000
2. V.M Blanco, S. Paolillo, M van der Veen, S Lariviere, G Lorusso, E Poortere, C Tabery, F Qiao, S Lai, M Kea, L Wang, Y Su, J Oh, J Huang, J Chen, J Huang, "Large Area EUV Via Yield Analysis for Single Damascene Process: Voltage Contrast, CD and Defect Metrology", Proceedings Volume 11147, International Conference on Extreme Ultraviolet Lithography 2019; 111470B (2019) https://doi.org/10.1117/12.2536943
3. O. D. Patterson, H. Wildman, A. Ache, K. Wu, "In-Line Voltage Contrast Inspection of ungrounded Chain Test Structures for Timely and Detailed Characterization of Contact and Via Yield loss", Proceedings of ISTFA, pp 401-406, Nov 2005.

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WCMP contact slurry influence on the formation of TaNTa barrier residues after metal 1 CuCMP

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It is well known that the morphology of incoming wafers to the CMP process is critical for its proper execution. Additionally, it is understood that various CMP processes can influence the successful polishing of the upper layers [1-2].
In this work, we present a comprehensive study on one of the root causes of barrier residue formation during the Metal 1 Chemical Mechanical Planarization (CMP) process in single damascene structures. This type of defect is particularly critical as it can lead to shorts, compromising the functionality of the device. Our focus is specifically on the influence of two different slurries used during the Tungsten CMP (WCMP) process of the underlying layer.
Typically, in the WCMP process, oxide erosion is closely tied to the tungsten pattern density. Structures with a high density of contacts, exhibit a higher local removal rate, which induces erosion. This phenomenon is further exacerbated by the use of tungsten-selective slurries (Fig. 1). These slurries demonstrate a higher tungsten removal rate, leading to increased erosion compared to non-selective slurries. Moreover, the low oxide removal rate of these slurries is insufficient to mitigate the resulting non-uniformity (Fig. 2). In high contact density structures, we observed erosion values more than tripled when using a selective slurry process (Fig. 3).
The topography created by contact WCMP is subsequently transferred to the Metal 1 layer, as copper puddle [3] especially if high copper to barrier selective slurries are used. During the Copper CMP (CuCMP) process, the non-uniform morphology cannot be adequately compensated, resulting in the presence of copper and barrier residues within the depressions formed by the erosion of the underlying layer. This defect becomes even more critical in CuCMP processes when consumables approach end-of-life, as the barrier removal capability decreases (Fig. 4).
This study aims to elucidate the mechanisms behind barrier residue formation and provide insights into optimizing the CMP process to minimize such defects. By understanding the impact of slurry selection and pattern density on erosion and residues formation, we can enhance the reliability and performance of semiconductor devices.

References

1. S.H. Chang, “A dishing model for chemical mechanical polishing of metal interconnect structures”, Microelectronic Engineering, vol.77, 2005, pp. G664-G668.
2. J.B. Lin, S.C. Lin, and H.C. Hong, “A Simulation Approach of Dishing in Chemical Mechanical Polishing of Inlaid Copper Structures, J. Electrochem. Soc., vol. 152, 2005, pp. G664-G668.
3. H. Yu, Y. Moon and H. Liu, "Topography Understanding of Tungsten Chemical Mechanical Polishing for Advanced Technology," ICPT 2012 - International Conference on Planarization/CMP Technology, Grenoble, France, 2012, pp. 1-6

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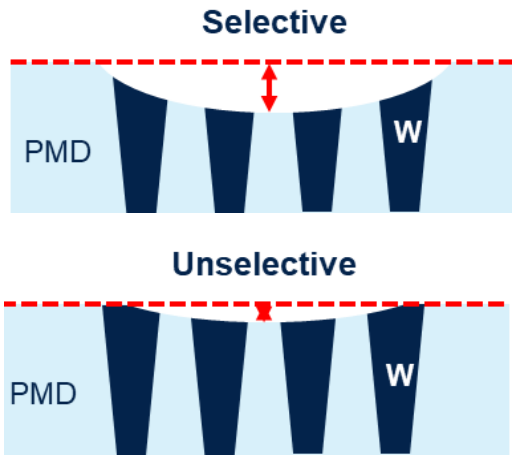

Figure 1 Sketch of erosion mechanism on dense contacts at WCMP process using different slurries.

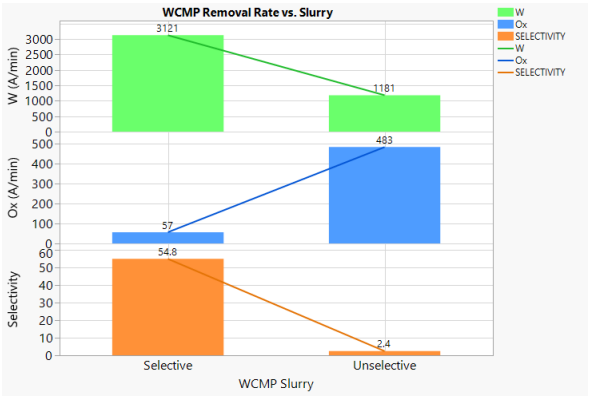

Figure 2 Removal Rate and selectivity at WCMP vs. Slurry

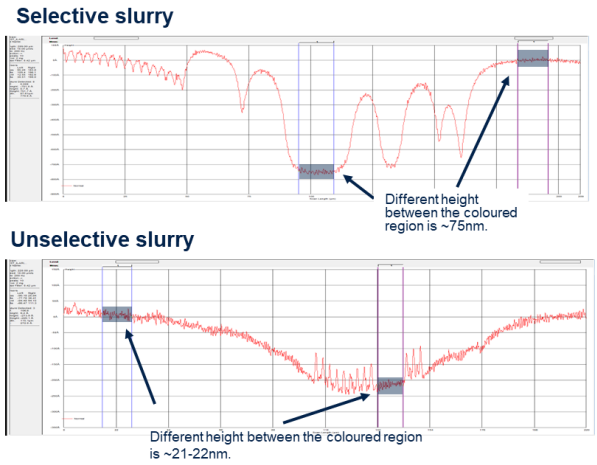

Figure 3 Profilometer post WCMP of a critical structure polished with selective and unselective slurry

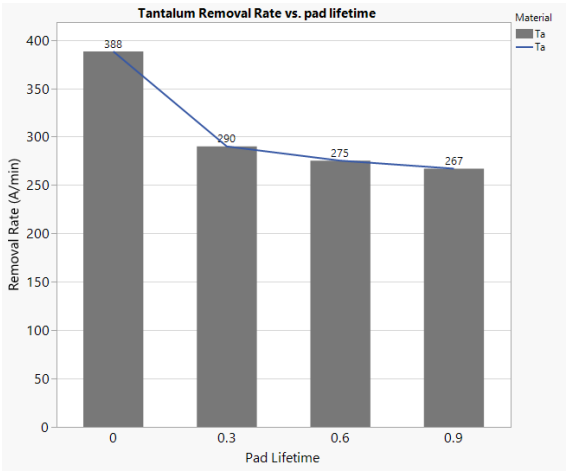

Figure 4 Tantalum removal rate vs. pad lifetime.

$Si_xGe_{(1-x)}$ simulations with hybrid exchange-correlation functionals

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Silicon-germanium random alloys have many applications in microelectronics, including photovoltaic and infra-red sensors. Work in these fields requires a good knowledge of the electronic bands structure, thus ab-initio simulations can be a useful tool for the design and production of effective devices. Experimental evidences show that the band gap in $Si_xGe_{(1-x)}$ random alloy, where x represents the silicon concentration, varies as a function of x following two distinct trends; for 0.0 < x < 0.15, the conduction band minimum is positioned along the <1 1 1> direction at the edge of the Brillouin zone, like in germanium, and its value varies linearly with x, whereas for x > 0.15 the conduction band minimum is positioned along the <1 0 0> direction, like it happens in silicon, and the band gap dependence is parabolic [1]. However, standard GGA-DFT calculations severely underestimate the band energy gap in silicon and makes germanium a semimetal, instead of the correct indirect gap semiconductor. To solve this problem, this contribution proposes and implements a variation of the technique presented in Darmody et al. 2015 [2], that uses a combination of lattice compression and hybrid PBE0 exchange-correlation functional.
We fit the energy gaps of both bulk materials to a second degree polynomial function in which the mixing parameter of the hybrid functional and the lattice pressure are independent variables; we then use these fitted functions to find the values of the two variables that makes the simulated energy gaps the closest to the experimental evidence. Since we are trying to simulate the correct gaps for two different materials at the same time, some level of compromise must be accepted. We found the best parameter to recreate the values of the energy gaps within 1% of the experimental values at the cost, however, of having the direct band gap of germanium being only 0.01 eV larger than the indirect one, instead of the correct 0.15 eV. Then, we simulate the evolution of the energy gap in $Si_xGe_{(1-x)}$ using the best-fit values of pressure and mixing parameter with 8, 16 and 32-atom-supercells in QUANTUM ESPRESSO [3]. The random structure of the alloy is mimicked using the Special Quasi Random Structure (SQS) approach [4], implemented through the mcsqs software of the Alloy-Theoretic Automated Toolkit (ATAT) [5]. Our calculations show that using 8-atom-supercells produces gaps in good agreement with the experimental data for 0.0 < x <0.15, but not for 0.15 < x < 1.0, nor it correctly models the change in position of the band gap minimum. On the other hand, when 16-atom-supercells are used, the agreement is bad in the linear region, but it improves for x > 0.3, while again failing in predicting the transition of the conduction band minimum. The 64-atoms-supercells provided the best results, with the gaps showing linear and quadratic evolution in the correct intervals (Fig.1) and correctly predicting the position of the conduction band minimum for all but two (x=0.1875 and x=0.25) of the simulated compositions.

References:

1. J. Weber, M.I. Alonso, Phys. Rev. B 40, 5683—5693 (1989)
2. C. Darmody, D.P. Ettisserry, N. Dhar, 2015 International Conference on Simulation of Semiconductor Processes and Devices, (IEEE, 2015,Washington DC) 329-332.
3. P Giannozzi et al 2017 J. Phys.:Condens. Matter 29 465901
4. A. Zunger, S. H. Wei, L. G. Ferreira, J. E. Bernard, Phys. Rev. Lett. 65, 353-356 (1990)
5. A. van de Walle, P. Tiwary, M. de Jong, D.L. Olmsted, M. Asta, A. Dick, D. Shin, Y. Wang, L.Q. Chen, Z.-K. Liu, Calphad 42, 13-18 (2013)

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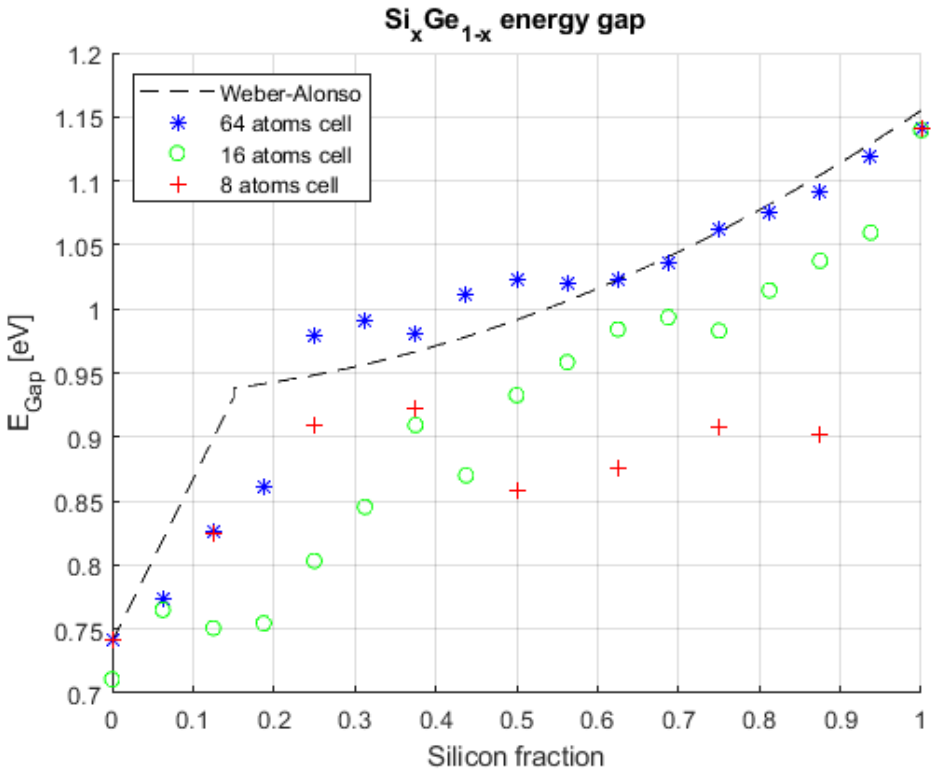

Fig 1: energy gap as a function of x, the dotted line represents the experimental evidence from [5]

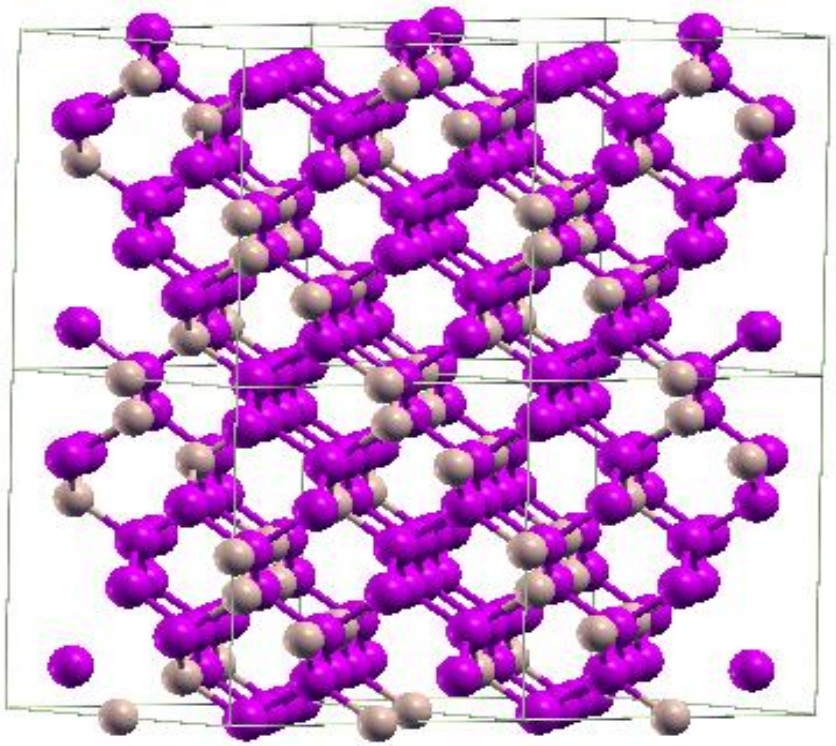

Fig 2: 16-atom-supercells with x=0.25, 4 supercells are shown in total

Cross correlation of DSC / XRD on phase change thin film used in PCRAM technology

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In situ XRD (X-Ray Diffraction: structural analysis) and DSC (Differential Scanning Calorimetry: thermal analysis) offer the possibility of following state change induced by an environmental temperature surroundings. The coupling of DSC / XRD (concomitant or not) makes possible the correlation of thermodynamic and structural state evolution under the effect of thermal treatments. A more reliable characterisation is expected by giving new insights on a material behaviour: polymorphic phase transitions, fusion, crystallization or relaxation, segregation …
Phase Change Random Access Memories (PCRAM) are likely the successors to flash memories and show growing technological interest. As focus point of this type of memory, the amorphous/crystalline transition is crucial to store information. The phase changes and their stability are the topic of interest to improve the reliability of the memory devices. Many PCM materials are under investigations, and here in this work, the material case study is the $Ge_2Sb_2Te_5$ (GST), a reference material for PCRAMs [1].
The target of this study is to compare both analytical point of view as a first approach evaluation. a cross correlation of non-concomitant XRD / DSC techniques on a sample is presented and discussed: thermal in situ XRD analysis and thermal DSC analysis are carried out firstly and secondly under a same sample and in a comparable controlled thermal environment.
As commonly powder material sample is generally necessary for DSC [2], a specific thin film approach is investigated for DSC analysis. The discussion is open in this way under the support of instrumental, experimental and material considerations.

[1] F. Fillot et al., JAC, 51, 1691-1705, 2018
[2] C. Cabral et al., APL, 93, 071906, 2008

Investigation of Phase Formation at the Ni/Sn Interface during the Soldering Process

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Soldering is a well-established method for creating permanent bonds between metal parts, often resulting in the formation of intermetallic compounds. For the purpose of soldering, various elements like Sn, Pb, Bi, Sb, Ag and Cu, or their alloys, are utilized in different compositions based on the respective field of application. The shift towards lead-free solder, driven by environmental regulations, has increased interest in Sn-based solder alloys. However, soldering interconnects involves complex processes related to material transport, phase stability, phase formation, and kinetic aspects of phase transformation. [1, 2]

In the present work, we investigated the interdiffusion and diffusion-controlled phase formation processes in a Sn-Sb solder alloy between a Ni-based layer with a small amount of Si and a Cu substrate using various electron microscopy techniques. Initial scanning electron microscopy analyses of cross-section samples provided an overview of the interfaces, including the Sn-Sb solder alloy. For detailed examination, focused ion beam techniques were employed to create electron-transparent samples for analysis using analytical transmission electron microscopy.

Examination of the untreated states of the Ni-based layer and the solder alloy enables differentiation between the initial microstructure and post-soldering changes. The Ni-based layer exhibited a lamellar-type structure with a uniform elemental distribution perpendicular to the soldered interface, while the raw solder alloy consisted of a tetragonal β-Sn phase as a matrix and a trigonal SbSn phase. Following the soldering process, CuSnNi and SnCu intermetallic compounds are formed with various shapes, surrounded by the β-Sn matrix. The SbSn phase remained as small inclusions throughout the process. Moreover, the Ni-based layer initially shrank due to diffusive interactions with Cu and Sn, resulting in a residual film that displayed an increased Si content compared to its untreated counterpart, eventually leading to complete consumption of the Ni-based layer.

This study highlights the complex processes involved in Cu transport from the substrate through the solder material, emphasizing the significant role of Cu in forming intermetallic compounds. Alongside with Sn, Cu drives the transformation of the Ni-based layer, ultimately to its complete consumption. In addition to elemental influences, microstructures play a crucial role in the Ni consumption process.

References

1. K. N. Subramanian, *Lead-Free Solders: Materials Reliability for Electronics*, (John Wiley and Sons Ltd Registered, 2012).
2. G. Humpston and D. M. Jacobson, *Principles of Soldering* (ASM International, 2004).

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In situ TEM investigation of the deformation mechanism of thick copper metallizations

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The structure of power semiconductor devices is constantly evolving to meet industry demands for higher power density, operating temperatures, miniaturisation and reliability. Typically, these devices contain several layers of different materials with different coefficients of thermal expansion (CTE) that induce thermomechanical strains and fatigue in operation. During fast switching between on and off states, the temperature in the device can rise to over 200°C and the associated differences in CTE produces high mechanical stresses that can cause irreversible deformation of the various layers, ultimately leading to device failure. In silicon-based devices, an example of this damage is the surface roughening and cracking of the thin top metal layer (usually aluminium (Al)).
The transition from Al to Copper (Cu) metallization is one of the major improvements in power semiconductors that has significantly increased the possible operating temperature, switching frequency and reliability of devices. Several modifications were implemented such as the deposition technique from sputtering to electrochemically deposited films (ECD). The Cu metallization thickness was also increased from 5µm to about 20µm to improve their reliability and provide the mechanical stability of thick Cu ultrasonic wire bondings connected to them.
To investigate the deformation of these thick Cu films , Moser et al [1] designed microelectronic chips that have been customized to replicate the heating rates and temperatures in real applications for 20µm Cu metallization deposited on Silicon wafers. Joule heating through an electrically resistive polysilicon layer generates the heating pulses; these devices are commonly referred to as polyheaters and serve as the devices under test for this work.

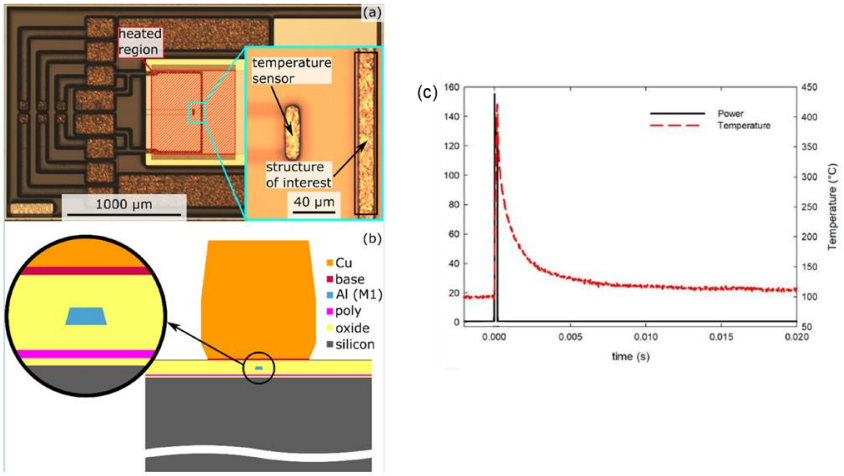

Figure 1 (a) An optical micrograph of the test chip used to thermal cycle rectangular Cu pad of 700×700×20µm^3 (b) Schematic representation of the cross-section showing the layers beneath the Cu metallization. The electrically resistive poly (polycrystalline silicon) layer facilitates the active heating of the chip via Joule heating (c) An example of the pulse with heating duration of 0.2ms applied to the Cu pad that results in temperature pulse of 100-400°C [1]

Moser et al [1] demonstrated that for base temperatures of ≥ 95°C the heating duration (length of pulses) dictates the degradation observed in the films. In this instance it is seen that shorter heating rates (0.2ms) result in inter granular cracking while for longer heating rates (5.4ms) the main degradation observed is extensive surface reconstruction. This work focuses on the microstructure evolution of the Cu films in which the heating duration is 0.2ms and the base temperatures of about ≥ 95°C. From the SEM surface images (Figure 1) we observe that as the number of cycles increases the apparition of pores is observed. The size and the occurrence of these pores increase as the cycles increase. After about 10k cycles we observe that the cracks have propagated from the surface of the film to the barrier in between the copper and silicon. A recent investigation on synchrotron dark field X-ray microscopy and in situ and ex situ scanning microscopy have attributed this degradation to the intragranular microstructural refinement and a gradual condensation of structural defects near high angle grain boundaries as driving forces for void formation in thick Cu films [2].

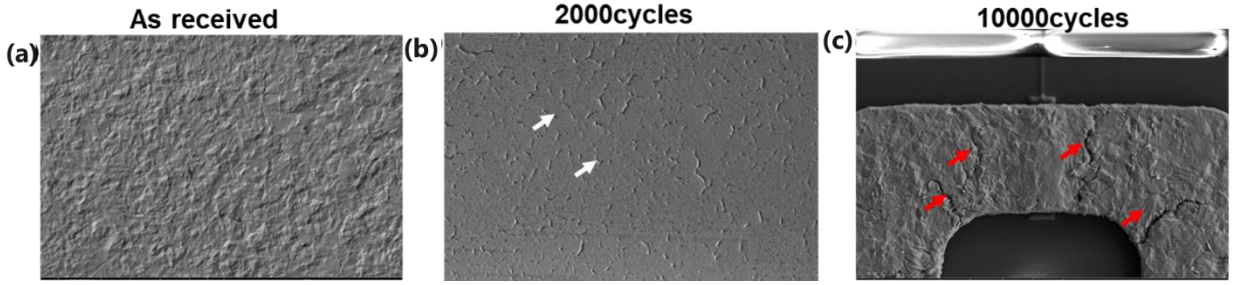

Figure 2 The evolution of the pore structure after several pulses. The white arrows point to the pores and the red arrows indicate the cracks on the surface of the thin film

In comparison to bulk materials, metallic films deposited on hard substrate deform in different manner with several intrinsic factors affecting their degradation such as their microstructure, grain size, film thickness… A common way to assess their mechanical properties and deformation mechanisms is to observe the thermal stress evolution during a heating and cooling sequence (also known as the wafer curvature experiment).

During a given thermal cycle, the biaxial stress in the film is measured through wafer curvature and the Stoney equation at heating rate on the order of 10°C/min [3]. This results in stress-temperature curves where the elastic to plastic deformation of these films can be monitored. These curves where subsequently interpreted to lay down hypothesis on the possible deformation mechanisms responsible for their degradation. Nonetheless, most of the hypothesis presented based on these curves such as the reversible motion of threading dislocations [4], the dislocation glide [5] and the combination of several mechanisms (dislocation glide, creep and grain boundary diffusion) [6] at different temperatures and stresses could not explain degradation features such as surface roughening and crack formation.

In-situ TEM (Transmission Electron Microscopy) has proven to be effective in directly observing the microstructural changes induced by the thermal cycling of thin films by partially reproducing thermal stresses acting on the metal part. Particularly in Al films the work of Martineau et al and Rufilli et al [7-8] have shown that the TEM is a direct way to confront existing deformation models, particularly those based on easily observable defects such as dislocations. As the dislocations are progressively trapped in grains, sub-grain boundaries and interfaces, a qualitative model based on grain-boundary accelerated diffusion was presented to explain the crack initiation and propagation during the thermal aging of Al films . Similar in-situ TEM observations where carried out in a previous study on thick copper films cycled at low base temperature (50°C) and longer heating durations (4.5sec)[9]. It corroborates the hypothesis that within the initial thermal cycles, the intragranular microstructural refinement is mainly caused by dislocations gradually reorganizing themselves into cell structures.

As the cycling rates increase the behaviour of dislocations (intragranular structure) may change, and so their, contribution to the voiding and fracture observed in the films. This work aims to utilize advanced microscopy techniques such as conventional and in-situ TEM to elucidate the mechanisms responsible for pore formation and crack propagation in thick Cu films.

References

[1] S. Moser, M. Kleinbichler, J. Zechner, M. Reisinger, M. Nelhiebel, and M. J. Cordill, Fatigue of copper films subjected to high-strain rate thermo-mechanical pulsing, Microelectronics Reliability **137**, 114782 (2022).
[2] K. Hlushko, T. Ziegelwanger, M. Reisinger, J. Todt, M. Meindlhumer, S. Beuer, M. Rommel, I. Greving, S. Flenner, and J. Kopeček, Intragranular thermal fatigue of Cu thin films: Near-grain boundary hardening, strain localization and voiding, Acta Materialia **253**, 118961 (2023).
[3] S. Bigl, C. O. W. Trost, S. Wurster, M. J. Cordill, and D. Kiener, Film thickness dependent microstructural changes of thick copper metallizations upon thermal fatigue, J. Mater. Res. **32**, 2022 (2017).
[4] W. D. Nix, Mechanical properties of thin films, Metall Trans A **20**, 2217 (1989).
[5] P. A. Flinn, D. S. Gardner, and W. D. Nix, Measurement and Interpretation of stress in aluminum-based metallization as a function of thermal history, IEEE Trans. Electron Devices **34**, 689 (1987).
[6] M. Thouless, J. Gupta, and J. Harper, Stress development and relaxation in copper films during thermal cycling, Journal of Materials Research **8**, 1845 (1993)
[7] Martineau, D., Levade, C., Legros, M., Dupuy, P., & Mazeaud, T. (2014). Universal mechanisms of Al metallization ageing in power MOSFET devices. Microelectronics Reliability, **54**(11), 2432-2439
[8] Ruffilli, R. (2017). *Modes de fatigue des métallisations à base d'aluminium dans les composants MOSFET de puissance*| *Theses. fr* (Doctoral dissertation, Toulouse 3)
[9] Karanja, L. (2024) Mécanismes d'endommagement des interconnexions en cuivre et en aluminium dans les IGBT de puissance. *Theses. fr* (Doctoral dissertation, Toulouse 3).

Resistance of advanced interconnects with anisotropic conductors: finite element simulations

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The continued decrease in feature sizes in integrated circuits result in strong increasing resistivity in copper interconnect due to additional charge carrier scattering at small dimension due to interfaces and grain boundaries. This is now considered as a severe limitation for the further downscaling of Cu interconnects [1,2]. Among potential alternative metals to replace Cu metallization in future technology nodes, several considered materials possess two-dimensional anisotropic resistivities. Examples are MAX materials [3] or delafossite oxides. In particular the latter are interesting since they possess in-plane resistivity around 2 µΩcm, comparable to Al [4]. However, delafossite oxides are characterized by a strong resistivity anisotropy with a much higher resistivity along the hexagonal axis [5]. In this work, we study the effect of resistivity anisotropy in 2D metals for advanced interconnects by finite element simulation to understand its impact on interconnect performance and materials characterization.

To address the impact of strong resistivity anisotropy of a two-dimensional interconnect, a “top contact” model is built by COMSOL Multiphysics, as shown in Fig. 1a. The line consists of an metal with varying degree of anisotropy, including isotropic transport as a limit. Simulated results for out-of-plane/in-plane resistivity anisotropies of 100 and 1 (isotropic) in Figs. 1b and 1c, respectively. The simulations show that the simulated line resistance of the anisotropic metals is 6 times larger than that of an isotropic metal for the same resistivity along the line direction. This can be explained by a large spreading resistance and surface current crowding for anisotropic metals with large out-of-plane resistivities. This can be mitigated by a side contact model with (isotropic metal) vias inside the anisotropic metal line, as shown in Fig. 1d. The simulations show that the side contacts strongly reduce the impact of the resistivity anisotropy on the line resistance, although further design optimization is needed to fully recover isotropic metal values.

This indicates that the full characterization of the anisotropic resistivity in thin films is critical for materials benchmarking. Macroscopic Four-Point-Probe (4PP) measurement have thus also been modelled in by COMSOL, as shown in Fig. 2a. Two types of metal films are compared, both isotropic as well as two-dimensional anisotropic films. Fig. 2b shows that the simulated resistivities for both cases correspond to the in-plane resistivity, here 2 µΩcm. Hence, 4PP measurements can assess accurately the in-plane resistivity but are not sensitive to the out-of-plane resistivity. Therefore, an alternative transmission line method (TLM) test structure is proposed to access out of plane resistivity of two-dimensional metals.

Commonly used to characterize contact the contact resistance of semiconductor/metal interfaces, TLM can also be used to extract the spreading resistance increase due to the resistivity anisotropy, independent of the sheet resistance. The simulations in Fig. 3a indicate that µm distances between contacts is necessary for the TLM model to be sensitive (Fig 3b). For very short distances, however, the overlap of the spreading resistance areas modifies the behavior qualitatively. Moreover, as shown in Fig 3c, sub-µm contact sizes are needed for the spreading resistance to be measurable. This demonstrates that simulations can further drive the study of two-dimensional metals for advanced interconnect metallization.

References

[1] D. Gall, J. Appl. Phys. **127**, 050901 (2020).
[2] J.-P. Soulié *et al.*, J. Appl. Phys. **136**, 171101 (2024).
[3] K. Sankaran, *et al.*, Phys. Rev. Mater. **5**, 056002 (2021).
[4] A. P. Mackenzie, Rep. Prog. Phys. **80**, 032501 (2017).
[5] M. D. Bachmann *et al.*, *Nat. Phys.* **18**, 819 (2022).

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Figure 1: Simulation of isotropic and anisotropic metals on top contact and side contact interconnect

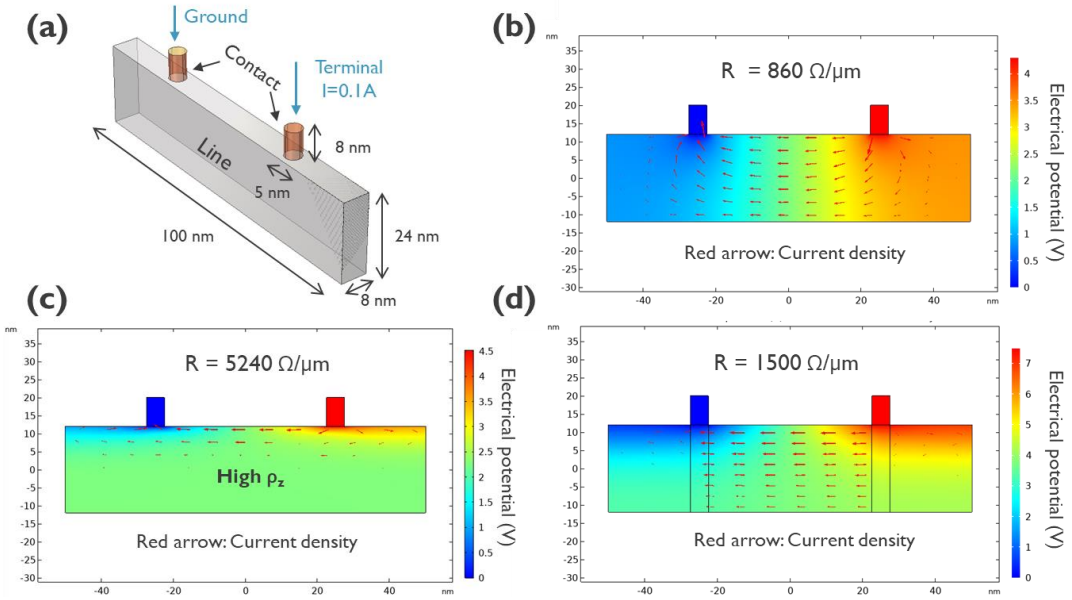


Figure 2: Simulation of macroscopic Four-Point-Probe (4PP) measurement on isotropic and anisotropic metal films

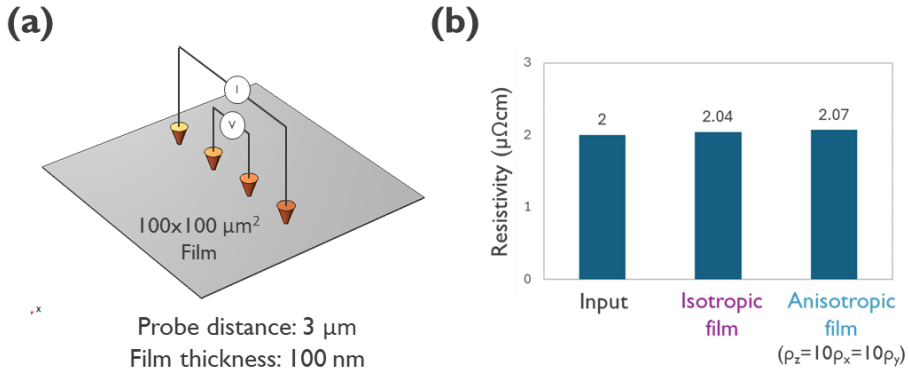
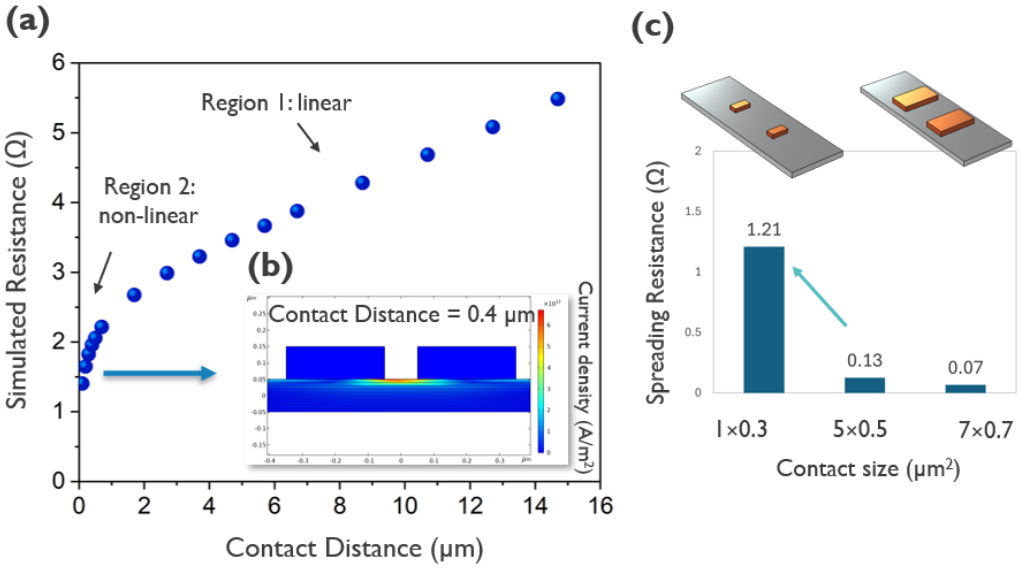


Figure 3: Simulation of Transmission Line Model (TLM) on anisotropic thin metal films



Porosity engineering for ultra-low k spin-on dielectric materials

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Ultra-low dielectric constant (ULK) materials are attractive option for the next generation intermetallic and interlayer dielectric materials due to their significant contribution for resistive-capacitive (RC) delay decrease. A common strategy for ULK material development is to reduce the dielectric constant (κ) of the material by introducing air to the structure with porosity. Typically, ULK materials include thermally labile components "porogens" which can be removed during the material curing [1]. Challenges associated with the increasing porosity include compromised mechanical properties and higher risk for plasma-induced damage, which can be detrimental for the dielectric performance during the process integration. Often, dielectric strength is compromised as well. However, not all porosity is the same: size, connectivity and structure of the pores have huge impact on the material performance.To achieve ULK SOD material with acceptable hardness and dielectric strength, careful porosity engineering is required to form a material with controlled pore structure consisting of small, isolated and well-organized pores. For uniform pore distribution, porogens bound to the polymer matrix are preferred. We have introduced a polymer-bound porogen to an organosiloxane polymer composition and carefully characterized the material properties. In addition, we investigated if polymerization process conditions could affect the material performance. Materials were cured with combined thermal and UV curing for effective porogen removal [2].

Material characterization revealed significant differences between the different polymerization processes, even though polymers consist of the same amount of organosiloxane polymer matrix and polymer-bound porogen. "Process A" refers to our typical polymerization process and "Process B" to a new-found, optimized polymerization process. "Reference" material is used to benchmark ULK material performance compared to porogen-free SOD. Refractive index (RI) comparison shows decreased RI for both porogen containing samples, as expected when air is introduced to the material (Figure 1). Film shrinkage between soft bake and cure increases similarly (Figure 2). Dielectric properties are excellent for both Process A and B materials: low $\kappa < 2.4$ is achieved (Figure 3). In addition, breakdown voltage of both ULK materials are comparable or even increased compared to Reference, which is not typical for highly porous materials (Figure 4). Modulus and hardness of the materials were analyzed with nanoindentation. Process A material had clearly lower hardness compared to the reference (Figure 5). However, Process B material had higher hardness than process A, providing mechanical properties close to the porogen-free Reference material. Porosity analysis with variable angle spectroscopic ellipsometer (VASE) revealed major differences between the materials as well: Process B had lowest relative porosity below 2%, whereas Process A and even the Reference had relative porosity 9 and 6%, respectively (Figure 6). Therefore, Process B material possesses a rare combination of ultra-low dielectric constant, high dielectric strength and decent mechanical properties. Low RI suggests that pores have been formed into the material, but VASE method did not detect significant amount of porosity. Our hypothesis is that Process B can form isolated pores to the material, whereas process A has more connected pores. Isolated pores may not be detected with VASE, as it is based on solvent penetration to the pores, and penetration is easier for an open, connected pore network. To confirm the hypothesis, more advanced porosity analysis is required, e.g. positron annihilation lifetime spectroscopy (PALS).

To summarize, the polymerization process was found to have a dramatic effect to the performance of ULK SOD by improving mechanical properties while maintaining excellent dielectric performance. Therefore, it is a promising alternative to be the next generation interlayer or intermetal dielectric material.

References

1. D.J. Michalak *et al.*, Porosity scaling strategies for low-k films, Journal of Materials Research, **30**, 22 (2015)
2. Zenasni, Aziz *et al.* The role of ultraviolet radiation during ultralow k films curing: Strengthening mechanisms and sacrificial porogen removal, Journal of Applied Physics, **102**, 9 (2007).

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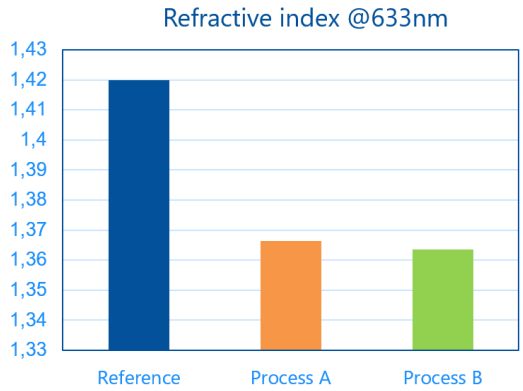

Figure 1. Refractive index comparison.

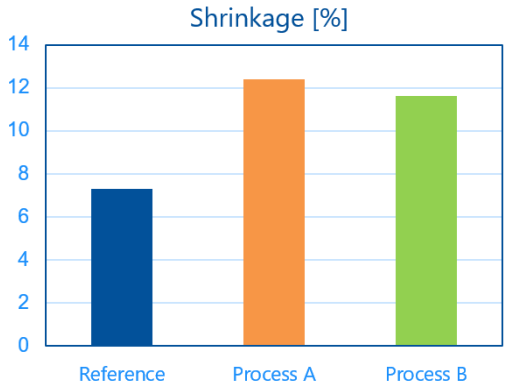

Figure 2. Shrinkage between soft bake and cure.

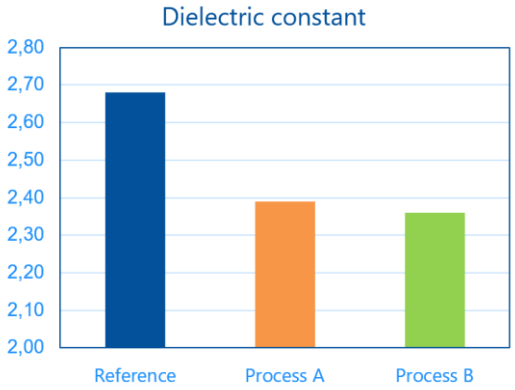

Figure 3. Dielectric constant reduction demonstration.

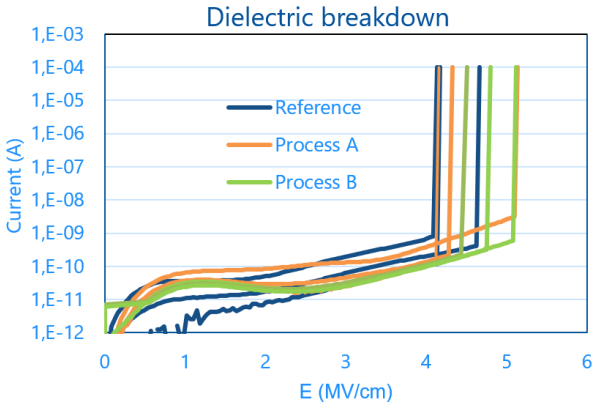

Figure 4. Current vs electrical breakdown voltage.

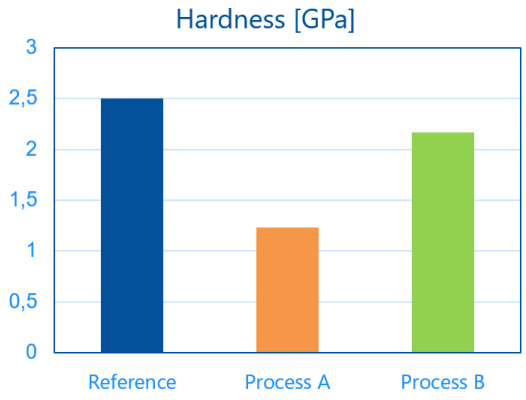

Figure 5. Hardness comparison.

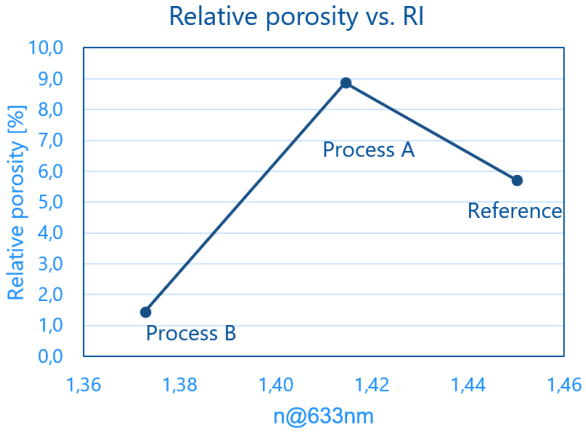

Figure 6. Relative porosity vs refractive index.

Challenges in Ru Damascene Integration for Future Interconnects

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Node-to-node scaling is reducing the transistor size and requires the interconnect pitch to follow to be able to connect the increased transistor density. Providing such tight pitch interconnects with conventional DD Cu structures is becoming more challenging below the 14nm critical dimension due to the intrinsic material properties of Cu. Here Ru has advantages as an alternative metal to Cu. Ru enables barrierless interconnects that have a lower resistance, better electromigration properties [1] and they can be used in direct metal processing.

Ru integrated in a semi-damascene offers [2] several benefits such as high aspect ratio lines, airgap incorporation to reduce intra-level capacitance and reduce RC delay [3], and the fact that it does not need a chemical mechanical polishing step (CMP) for the integration. However, moving towards Ru semi-damascene interconnect structures is a significant change in complexity and integration, while such schemes need damascene Ru lines as well to create multilevel interconnects.[4]

Therefore, this paper addresses the challenges for the dual damascene integration of Ru. We discuss the learning on the Ru fill in lines studied in 11 – 36 nm wide structures. More specifically, we address the difficulties in processing encountered resulting from high Ru melting temperature and the resistance of Ru to oxidation making the planarization by chemical mechanical polishing challenging.

References

[1] O. V. Pedreira et al., IEEE IRPS, pp. 1-7 (2020)
[2] G. Murdoch et al., IEEE VLSI 2022, p.427 (2022)
[3] A. Farokhnejad et al., IEEE IITC, p.137 (2022)
[4] A. Gupta et al., IEEE IEDM, S.13-2 (2023)

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Carbene Functionalization of 2D-Mo_2C, Ru, and Graphene on Ru

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Ruthenium, molybdenum and molybdenum carbide are among potential next-generation interconnect materials. (1,2) We will present studies of the chemical modification and or passivation of Ru, graphene covered Ru, and molybdenum carbide surfaces, with a focus on the use of surface carbenes. Experiments on molybdenum carbide show that a robust carbene surface layer can be readily formed through exposure to oxygenates such as ketones. (3) Data will be presented for N-heterocyclic carbene (NHC) functionalization of Ru and graphene covered Ru. (4) The oxygenate approach is suitable for modifying molybdenum carbide in that Mo can extract an oxygen atom to form a surface carbene while the NHC approach is better adapted to the less oxophilic Ru and graphene covered Ru surfaces.

References

1. J.-S. Kim, J. Kim, D.-Ji. Yang, J. Shim, et al. Addressing Interconnect Challenges for Enhanced Computing Performance. Science **386**, 1238 (2024).
2. K. Deng, I. Erofeev, A. R. Chowdhuri, H. Philipsen, et al. Nanoscale Wet Etching of Molybdenum Interconnects with Organic Solutions. Small **20**, 2406713 (2024).
3. M. Siaj, P. H. McBreen, Creating, Varying, and Growing Single-Site Molecular Contacts. Science, **309**, 588 (2005).
4. T. Zhang, S. B. Khomane, I. Singh, C. M. Crudden, P.H. McBreen, Functionalization of Metal-Supported Graphene by an *N*-Heterocyclic Carbene, *J. Phys. Chem. C* ***126*****,** 14430 (2022).

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Exploring the Relationship Between Doping and Ti-Silicidation for Advanced FDSOI Applications

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In advanced node transistors, contact resistance becomes more important due to the shrinking of dimensions [1]. This has led to a switch from Ni to Ti silicides to achieve resistance reduction [2]. This change requires optimization to achieve low contact resistivity. The doping process is known to affect the silicidation process [3]. However, the effect of the high dopant concentration - required for today's transistor - on phase sequence remains unclear. In this work, we study the effect of phosphorus concentration on titanium silicidation on n-doped Si layers with low-doped (few 10^{20} atoms/cm^3) and high-doped (few 10^{21} atoms/cm^3) epitaxial layers of about 30 nm on which 10 nm thick Ti films have been deposited. The samples were then annealed to form Ti-silicide compounds.

The evolution of the phase sequence of the Ti/Si:P system for low and high-doped Si:P epitaxial layers is described in Figure 1. For both systems, the reaction starts with the consumption of the titanium layer. Around 450 °C, the metal layer is completely consumed and the C49-$TiSi_2$ phase is identified. Then, the evolution of the C49 and C54-$TiSi_2$ phases is highly dependent on the P doping concentration: in the low-doped Ti/Si:P system, the C49-$TiSi_2$ phase is completely consumed around 730 °C and then no significant diffraction line appears up to 850°C. In the high-doped Ti/Si:P system, the complete consumption of the C49-$TiSi_2$ phase is shifted from 730 °C to 580 °C. Then a diffraction line corresponding to the C54-$TiSi_2$ phase appears around 700 °C.

In addition to the in-situ X-ray measurements, the sheet resistance (Rs) was measured as a function of annealing temperature for 30 s duration in an N_2 atmosphere. As shown in figure 2, the curves show three distinct regimes : Below 600°C, the R_s decreases slightly and then remains stable at about 40 Ω/sq up to 950 °C in the low-doped Ti/Si:P system and up to 800 °C in the high-doped Ti/Si:P system. The last regime is only observed at high doping concentration, where R_s drops to 30 Ω/sq. To better understand these phase transition curves, grazing incidence X-ray diffraction measurements were performed for different thermal annealing temperatures (Figure 3). The first regime appears to be associated with the formation of the Ti_5Si_4 phase (identified as diamond symbols in Figure 3) as also observed in [4]. However, the formation of Ti_5Si_4 is not correlated with an R_s plateau that generally characterizes phase formation. The phase observed in the plateau is the C49-$TiSi_2$ (triangle symbols) which remains stable up to 950°C in the low-doped system, in contrast to the high-doped system where the drop in R_s observed around 800 °C concerns the nucleation of the C54-$TiSi_2$ phase (circle symbols) in coexistence with the C49-$TiSi_2$ phase.

The effect of P doping concentration on Ti-based silicidation described in this work is discussed compared to the results shown by S. Park *et al.* in the Ti/Si:P system for similar dopant concentrations [5]. Indeed, they observed that increasing the phosphorus concentration inhibited the formation of the C54-$TiSi_2$ phase. In contrast, by combining different characterization methods, we observed that the phase transition from the C49 to the C54-$TiSi_2$ phases is shifted to a lower temperature for the high-doped sample.

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References

1. A. V.-Y. Thean et al., in *2015 Symp. VLSI Technol. VLSI Technol.* (2015), pp. T26–T27.
2. C. Lavoie et al., ECS Trans. **77**, 59 (2017).
3. E. Rosseel et al., ECS Trans. **98**, 37 (2020).
4. H. Yu et al., IEEE Trans. Electron Devices **63**, 4632 (2016).
5. S. Park et al., Phys. Status Solidi A **216**, 1800620 (2019).

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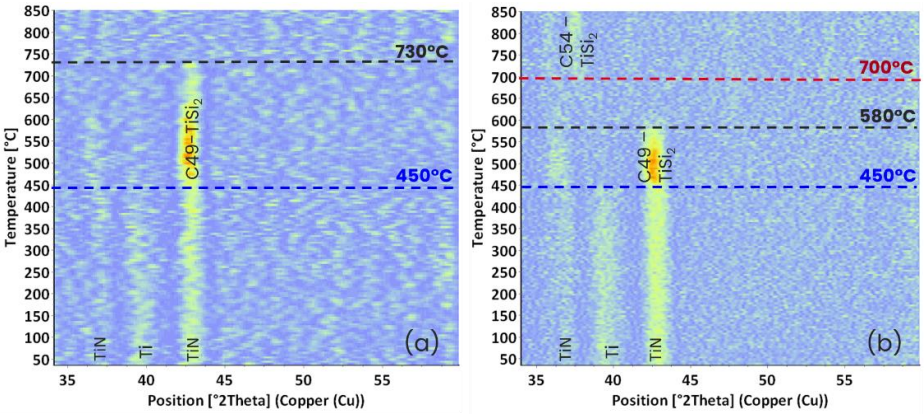

Figure 1. *In-situ* X-ray diffraction mappings corresponding to the reaction between a 10 nm Ti metal layer deposited on (a) low-doped and (b) high-doped Si:P (100) epitaxial layers. The blue dashed lines correspond to the temperature of full metal consumption and the C49 $TiSi_2$ identification. The black lines correspond to the C49 phase disappearance and the red lines to the growth of the C54 phase.

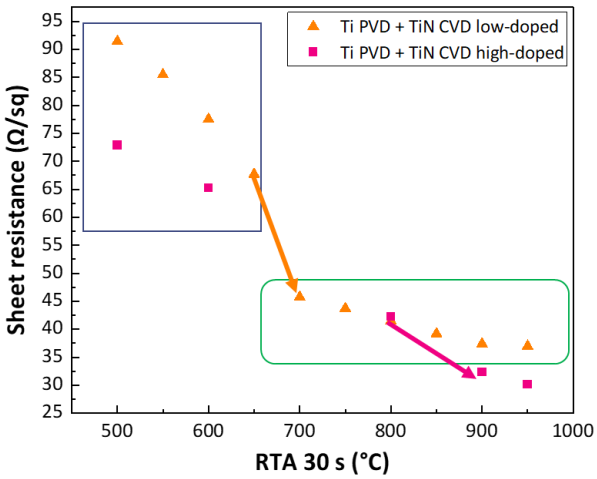

Figure 2. Evolution of the sheet resistance R_S for different rapid thermal annealing temperatures in the Ti/Si:P system with high-doped (pink squares) and low-doped (orange triangles) Si:P epitaxial layers. Samples were annealed for 30 s in an N_2 atmosphere.

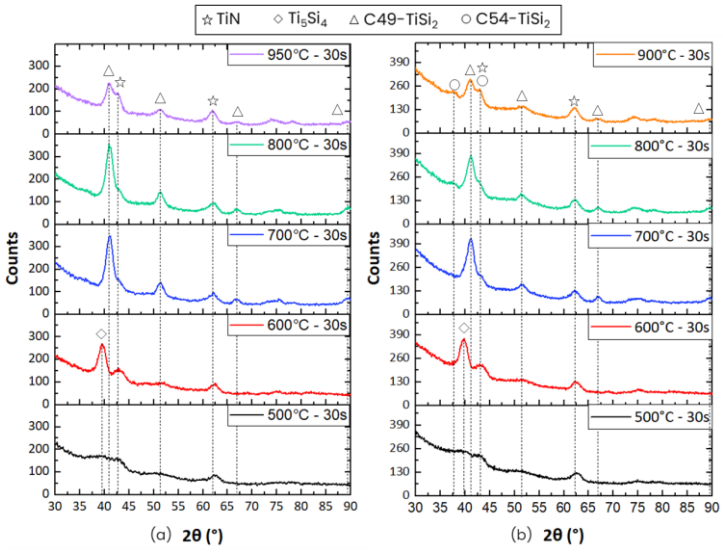

Figure 3. Grazing incidence X-Ray patterns corresponding to the evolution of the Ti/Si:P system as a function of different rapid thermal annealing temperatures, 30 s annealed in an N_2 atmosphere for (a) low-doped and (b) high-doped Si:P epitaxial layers.

Electrochemical and Morphological Study of Rhenium Electrodeposition on PVD-Mo Substrates

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A superconducting quantum computer consists of electronic circuits made from superconducting materials and employs qubits that can exist in a superposition of both 0 and 1 states simultaneously, which allows quantum computers to perform more complex computations compared to classical computers. High-critical temperature (T_c) superconductors are attracting significant attention in the electronics industry, particularly for their applications in superconducting quantum computers utilizing Josephson junctions. While low-T_c superconductors require helium-based cooling systems to maintain temperatures of 1–4 K, high-T_c superconductors provide enhanced stability and reliable performance over a broader temperature range. [1]

Superconducting materials commonly used in quantum computing include Nb, Nb-based alloys, Sn, and Ti. These materials are prone to oxidation and pose challenges in soldering. [2] Additionally, Pb exhibits a T_c of 7.2 K, however, its use is limited due to environmental concerns. [3] Rhenium (Re), on the other hand, has a remarkably high melting point of 3186°C and demonstrates excellent resistance to electromigration, making it a reliable material for circuit applications.

Re powder obtained by heating rhenium salts, such as ammonium perrhenate, in a hydrogen atmosphere at high temperatures exhibits a T_c of approximately 1.7 K. In contrast, Re thin films formed through electrodeposition demonstrate a significantly higher T_c of up to 6 K compared to the previous method. [4] Re electrodeposition occurs at potentials lower than the potential at which the hydrogen evolution reaction (HER) sets on. Consequently, hydrogen gas is generated during the deposition process which induces hydrogen embrittlement, resulting in cracks that can significantly degrade device performance. [5]

In this study, polyethylene glycol 20000 (PEG 20000) and sodium dodecyl sulfate (SDS) were employed as additives to prevent crack formation caused by the HER during Re electrodeposition on PVD-Mo substrates. Constant potential electrodeposition was conducted using PEG 20000, SDS, and a combination of PEG 20000 and SDS. Scanning electron microscopy (SEM) confirmed that the addition of PEG 20000, SDS, and the simultaneous use of PEG 20000 and SDS effectively eliminated cracks in the deposited films. Furthermore, atomic force microscopy (AFM) analysis was used to investigate the influence of the additives on nucleation and growth mechanisms (instantaneous nucleation or progressive nucleation) throughout the initial stages of electrodeposition on PVD-Mo substrates. Through electrochemical quartz crystal microbalance (EQCM) and Rutherford backscattering spectrometry (RBS) analyses, the amount of deposited Re was quantified and compared under additive-free conditions, with PEG 20000, with SDS, and with a simultaneous use of PEG 20000 and SDS. The combined use of PEG 20000 and SDS resulted in the highest deposition amount after 50 seconds at a potential of -0.7 V vs. Ag/AgCl.

References

1. Nature Materials 23, 612–618 (2024)
2. Journal of Alloys and Compounds 960, 170808 (2023)
3. Reviews of Modern Physics 26, 277–301 (1954)
4. Applied Physics Letters 112, 182601 (2018)
5. Electrochemistry Communications 93, 53–56 (2018)

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Influence of TaN/Ta Barrier Layer Thickness on Wafer Curvature and Via Chain Resistance

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Tantalum (Ta) and tantalum nitride (TaN) are extensively utilized in the semiconductor industry, particularly as barrier layers in integrated circuits. A common approach involves using a bilayer structure, where a layer of TaN is first deposited, followed by a layer of Ta to provide effective barrier performance against copper diffusion and ensures good adhesion to various substrates. [1] One of the most widely used techniques to obtain these thin bilayers is DC magnetron sputtering. [2] This study aims to analyze the effect that variations in bilayer thickness have on wafer curvature and via chain resistance. Bilayers are deposited on 300 mm wafers in a standard PVD chamber by Applied Materials (AMAT). During TaN deposition nitrogen (N_2) is used together with argon (Ar). During Ta deposition the same Ar flux is maintained and N_2 flow is stopped. The chamber is heated at 200°C. As a substrate, a silicon wafer with a 200 nm silicon oxide layer is used. The composition of the bilayer is varied by changing the deposition time for each layer. In Table 1, the RECIPEs used for this study are presented, distinguished by deposition time and deposition time ratio of TaN deposition time to bilayer deposition time.

The thicknesses of Ta and TaN layers are measured using Transmission Electron Microscopy (TEM) at the center of the wafer, with each measurement repeated three times for accuracy. Deposited bilayers have an average thickness between 65 nm and 85 nm. By analyzing the results, it is observed that the TaN deposition rate is slower compared to the Ta deposition rate by 5%. This behavior must be considered when designing deposition recipes.

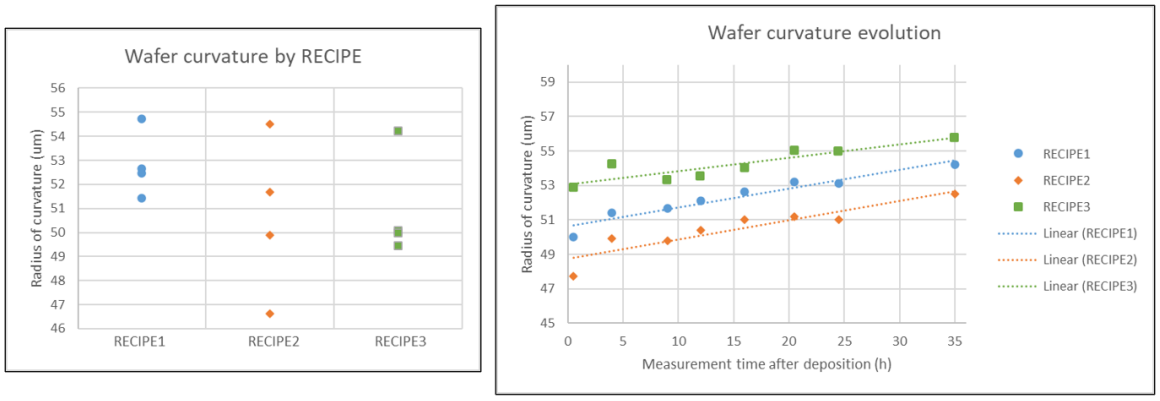
Thin metallic films deposited on wafers can induce stress, which can alter the wafer's curvature. A study was conducted to investigate the impact of bilayer thickness on curvature and its evolution over time. Films using RECIPE1, RECIPE2 and RECIPE3 were deposited to investigate composition influence by maintaining the same bilayer thicknesses. Four samples per each RECIPE were obtained and the change in the radius of curvature after deposition with respect to before deposition was measured (Figure 1a). Measurements for one sample of each kind were repeated at different times to monitor stress evolution (Figure 1b). The analysis demonstrates that the TaN/Ta bilayers induce a positive curvature, indicative of compressive stress, without a recipe dependence. Since tantalum is a high-density material, the induced stress is likely to be of intrinsic nature, given that the deposition temperature of 200°C is significantly lower than the tantalum melting point. [3] A slight change in curvature is observed over time, with a variation of about 4 µm detected 35 hours after deposition. For industrial applications, stress relaxation is negligible for this bilayer.

Via chain resistance is a critical parameter for barrier layers, as it directly impacts the performance of semiconductor devices. The influence of variations in the bilayer thickness on Copper Bondpad (CB)-via chain resistance was studied. Samples were tested on 9 different sites, and the CB-via chain resistance median for each wafer was calculated. The normalized resistance by wafer is reported in Figure 2a and Figure 2b. An increase in resistance is observed as the TaN thickness increases while maintaining the same total bilayer thickness. By changing the ratio of TaN deposition time to bilayer deposition time in the recipes from 0.23 to 0.26, an increase of 0.6% in the CB-via chain resistance of the device is observed. Additionally, an increase in resistance is also noted with an increase in the total bilayer thickness. By applying a change of 2s in the deposition time, the CB-via chain resistance in the device changes by 1%. However, the individual contributions of the TaN and Ta layers to this increase in resistance are more challenging to discern.

In this study, the TaN/Ta bilayer was first characterized by measuring single layer thicknesses using TEM; it was then observed that bilayer composition does not influence wafer curvature while an influence was shown for chain resistance. Correlations to thickness variations were evaluated. Given the significant role these films play in semiconductor devices, further studies are necessary to deepen our understanding and optimize their application.

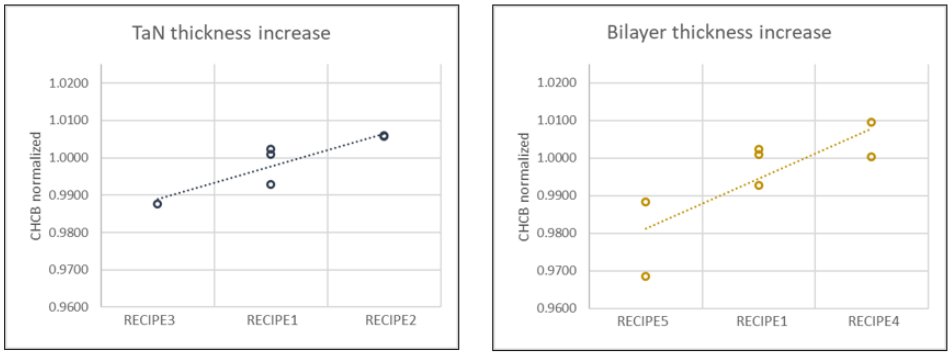
Table 1 The recipes used for this study are distinguished by deposition time and the ratio of TaN deposition time to bilayer deposition time.

RECIPE	BILAYER DEP TIME	TAN/BILAYER DEP TIME
RECIPE1	T1	0.25
RECIPE2	T1	0.28
RECIPE3	T1	0.23
RECIPE4	T1+1S	0.25
RECIPE5	T1-1S	0.25



a) b)

Figure 1 The change in the radius of curvature before and after deposition is plotted. a) Measurements for four different samples for each of RECIPE1, RECIPE2, and RECIPE3, which differ by TaN thickness, are reported. b) The evolution of the wafer curvature with respect to the time at which the measurement was performed after deposition is reported.



a) b)

Figure 2 The CHCB values are plotted by calculating the median value for each wafer and normalizing it by the average value of all measured values. a) Samples with the same bilayer thickness and different TaN thicknesses are compared. b) Samples with the same ratio of TaN deposition time to bilayer deposition time and different total bilayer thicknesses are compared.

References

1. Kim, Deok-kee, et al. "Electrical and mechanical properties of tantalum nitride thin films deposited by reactive sputtering." *Journal of crystal growth* 283.3-4 (2005): 404-408.
2. Bernoulli, Daniel, et al. "Magnetron sputter deposited tantalum and tantalum nitride thin films: An analysis of phase, hardness and composition." *Thin Solid Films* 548 (2013): 157-161.A. N. Example, Journ. Nam. **53**, 1256 (2007).
3. Thornton, J. A., & Hoffman, D. W. “Stress related effects in thin films”. Thin Solid Films (1989): 171(1-2), 5-31.

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Mechanisms of Edge Over Erosion Formation in Copper CMP

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Edge-Over-Erosion (EOE), also known as "fang," is a well-documented phenomenon that occurs during tungsten and copper Chemical Mechanical Planarization (CMP) [1-2]. This is typically observed at transitional regions between the edge of large non-patterned areas and an array of trenches (Fig. 1).

In this study, we present a comprehensive analysis of the formation mechanisms of this defect, examining both mechanical and chemical contributions.

The root cause of copper (Cu) dissolution is driven by the spontaneous reaction between copper and tantalum (Ta), which has a potential of 1.09V on the electrochemical series scale. This reaction can be represented as $2Ta + 5Cu^{2+} + 5H_2O <-> 5Cu + 2Ta_2O_5 + 10H^+$.

This dissolution process can be enhanced by mechanical factors, such as the contribution of the polisher, or controlled by kinetic factors by reducing the exposure time of copper to the electrolyte (slurry). Typically, the endpoint time, and therefore the exposure time, can be minimized by increasing the chemical removal rate of copper through higher concentrations of oxidizer (H_2O_2) and slurry (Fig. 2). Additionally, mechanical stress can be managed by adjusting the polishing pressure.

Several experiments were conducted to confirm the role of the oxidizer versus mechanical stress. The first test was focused on chemical factors, studying the roles of the oxidizer (H_2O_2) and process time, while on the second test we studied the mechanical factors, such as polishing pressure and endpoint.

The results confirmed that the primary parameter impacting EOE formation is the mechanical factor, specifically polishing pressure. This was followed by the kinetic factor, where the main contribution comes from the over-polish time. During this step, the galvanic couple is formed, and copper is exposed to the electrolyte (slurry). These findings highlight the importance of optimizing process parameters, polishing pressure and time, to mitigate the formation of EOE defects in copper CMP processes (Fig. 3).

References

1. Vacassy, Robert & Chen, Z.. (2006). EDGE-over-erosion in tungsten CMP. 632-639.
2. Y. Gotkis, D. Schey, S. Alamgir, J. Yang and K. Holland, "Cu CMP with orbital technology: summary of the experience," *IEEE/SEMI 1998 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop,* Boston, MA, USA, 1998, pp. 364-371

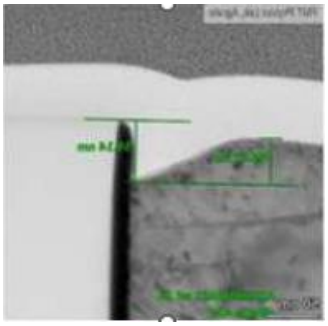

Figure 1 Cross section of a wafer impacted by EOE. Copper depletion is visible at the interface with TaNTa

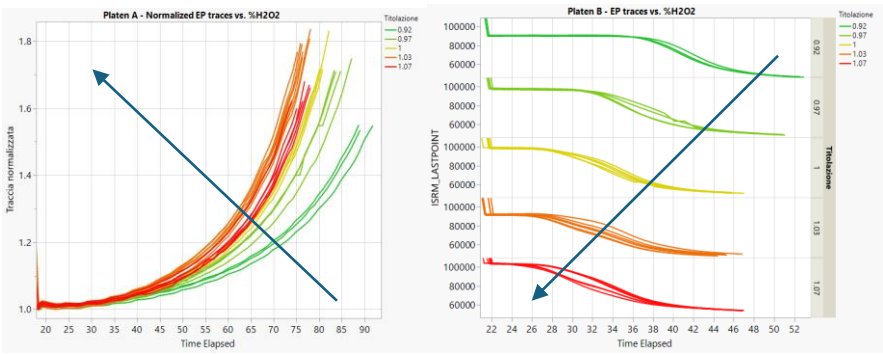

Figure 1 H_2O_2 is confirmed to increase RR and thus reducing the endpoint time both on Platen A (left) and Platen B (right)

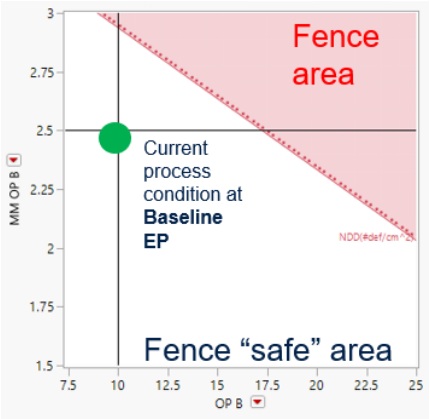

Figure 3 Defectivity response vs. overpolish time and pressure

Localized sub-25nm Ruthenium and Rhodium Vertical Interconnect Access (VIA) Formation Implementing Airgaps

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This presentation focuses on the fabrication of localized sub-25nm ruthenium and rhodium vertical interconnect accesses implementing surrounding airgaps. The semiconductor industry has reached a point where, in principle, only a few options for highly specialized processes are possible for a particular manufacturing step. In recent years, the implementation of ruthenium and rhodium has become increasingly important due to its higher conductivity at nano meter scale. The subtractive approach has become the dominant process to manufacture vertical interconnects using these metals. [1] On the other hand, these metals are very expensive in their purest form and are only controlled by very few mining countries. As long as the electronic properties outweigh the high cost of the materials, the subtractive approach is going to be attractive. Our research focuses on the opposite of this approach: additive formation of vertical interconnects [2]. Metallic clusters (<0.5 nm) are generated by a spark discharge of 5 to 10 W. An inert forming gas flow (5% H_2 in N_2) transports the clusters onto a pre-patterned substrate, where the metal clusters deposit in a localized fashion. The funneling effect to guide the clusters into the patterns is controlled by the transport gas ions, which are in the clear majority within the process. [3] The gas ions charge up the insulating oxide layer and act as a pillow which deflects the metal clusters into a localized vertical interconnect access. The flux of material is self-alinging centered to the middle of the VIA and is free-standing without interaction to the VIA wall. [4] The resulting vertical interconnect is surrounded by an airgap. The size of the airgap can be controlled by the number concentration of surface charges which create the funnel. This number concentration is a function of the VIA aspect ratio and the spark discharge power. [2]

References

[1] S. Dutta, S. Kundu, A. Gupta, G. Jamieson, J. F. G. Granados, J. Bömmels, C. J. Wilson, Z. Tokei, and C. Adelmann, Highly scaled ruthenium interconnects, IEEE Electron Device Lett. (2017).

[2] L. Schlag, N. A. Isaac, M. M. Hossain, A. L. Hess, B. C. Wolz, J. Reiprich, M. Ziegler, J. Pezoldt, and H. O. Jacobs, Self-Aligning Metallic Vertical Interconnect Access Formation through Microlensing Gas Phase Electrodeposition controlling Airgap and Morphology, Adv. Electron. Mater. **8**, (2023).

[3] L. Schlag, N. A. Isaac, H. Nahrstedt, J. Reiprich, A. Ispas, T. Stauden, J. Pezoldt, A. Bund, and H. O. Jacobs, Nanoparticle gas phase electrodeposition: Fundamentals, fluid dynamics, and deposition kinetics, J. Aerosol Sci. **151**, 105652 (2021).

[4] M. M. Hossain, L. Schlag, B. Wolz, M. Ziegler, H. Nahrstedt, H. Reichel, J. Pezoldt, and H. O. Jacobs, Ruthenium and Rhodium Vertical Interconnect Formation Using Gas Phase Electrodeposition, 2023 IEEE Int. Interconnect Technol. Conf. IEEE Mater. Adv. Met. Conf. IITC/MAM 2023 - Proc. 2023 (2023).

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Impact of Ti interlayer on the formation of Co silicides.

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In microelectronics, particularly in CMOS technology, metal silicides ($TiSi_2$, NiSi, and, $CoSi_2$) have been widely used as contacts (i.e., to form source, drain, and gate contacts) [1]. Specifically, the $CoSi_2$-based contacts are still interesting for 65 nm technology despite the difficult nucleation of $CoSi_2$ in small dimensions [2]. Besides, the $CoSi_2$ phase in hetero-epitaxy offers low resistivity, better thermal stability, and low interface roughness, which are key parameters for small-dimension devices. Several studies have shown that adding an interlayer, such as Ti, Ta, Zr, Cr, V, and Mo, between Co and the Si substrate significantly boosts the growth of epitaxial $CoSi_2$ on Si [2,3]. Also, interlayers play a crucial role as a diffusion and reaction barrier for initial Co-Si reactions. However, the impacts also rely on the various experimental parameters like annealing ambient and temperature, layer thicknesses, etc [2,3]. Hence, understanding the effect of the Ti interlayer on the formation of $CoSi_2$ is important.

Therefore, in this work, we systematically investigated the impact of thin Ti interlayer on the formation of Co disilicides. After cleaning the Si_{100} substrate (i.e., 300 mm), 3 nm and 5 nm Ti interlayers, 7.5 nm Co films, and a 10 nm TiN protective layer were prepared using the PVD technique. Numerous sample pieces (i.e., TiN/Co/Si (reference, without Ti), TiN/Co/3nm_Ti/Si, and TiN/Co/5nm_Ti/Si) were annealed using rapid thermal annealing (RTA) between 100 and 900°C with a temperature step of 20°C. Then, the X-ray diffraction (XRD) and the surface resistance (Rs) measurements were carried out at ambient conditions to understand the Ti interlayer impacts on the formation of Co silicides. The XRD results (**Fig. 1**) show that the presence of 3 nm and 5 nm Ti interlayer during the formation of Co silicides significantly modifies the formation temperatures and possibly the phase sequence (**Fig. 1b**). In particular, an additional phase called X is formed at low temperatures (around 300 °C). Mainly, the diffraction peak of the $CoSi_2$ phase is noticed between 530 and 630°C for 3 nm_Ti and between 550 and 610°C for 5 nm_Ti compared to the reference sample (observed up to 900°C). At temperatures higher than 660°C, diffraction peaks at $2\theta = 27.4°$ and $2\theta = 39.3°$ were noticed and attributed to the TiO_x and $TiSi_2$. Moreover, from 820 to 900°C, various diffraction peaks (i.e., $2\theta = 40.8°$, $2\theta = 42.8°$ and $2\theta = 45.0°$) were observed. In **Fig. 2**, especially for the reference sample, the Rs behavior remains stable below 200°C then gradually increases up to 400°C, attributed to the successive formation of the Co_2Si and CoSi phases. Then, a plateau is noticed until a sharp decrease in Rs around 520°C, attributed to the formation of the $CoSi_2$ phase. However, the behavior is slightly different for Ti interlayer samples. In addition, a specific annealing temperature (600°C, 10 mins) was chosen to study the presence of heteroepitaxy of fully formed $CoSi_2$ phase, verified with XRD measurements (**Fig. 3**). The reference and Ti interlayer films (without TiN capping) show a diffraction peak at $2\theta = 33.7°$, attributed to the $CoSi_2$ (200) phase in hetero-epitaxy, which is not observed for Ti films (with TiN). Also, TEM-EDX observations were carried out on TiN/Co/Si and TiN/Co/5nm_Ti/Si films after a Salicide process (RTA1@550°C 60 s/selective etching/RTA2@790°C 20 s) to confirm the hetero-epitaxy of the $CoSi_2$ layer obtained during the growth of Co silicides through Ti interlayer (**Fig. 4**). The TEM images show a $CoSi_2$ layer above the Si substrate, and the thicknesses vary between 22 & 29 nm (TiN/Co/Si) and 7.7 & 13 nm (TiN/Co/5nm_Ti/Si). These difference in thicknesses possibly comes from the weaker diffusion of Co through a Ti interlayer, which induces limited reaction during the Salicide process. Overall, this study is beneficial for understanding the Ti interlayer effect on the Co silicide formations and for the integration of contact formation in microelectronics.

References

[1] C. Lavoie, et al., ECS Trans. **77**, 59 (2017).
[2] Andréa Newman Thesis, 2023AIXM0518, https://theses.fr/s388642?domaine=theses (2023).
[3] Hannes Zschiesche Thesis,http://www.theses.fr/2019AIXM0219 (2019).

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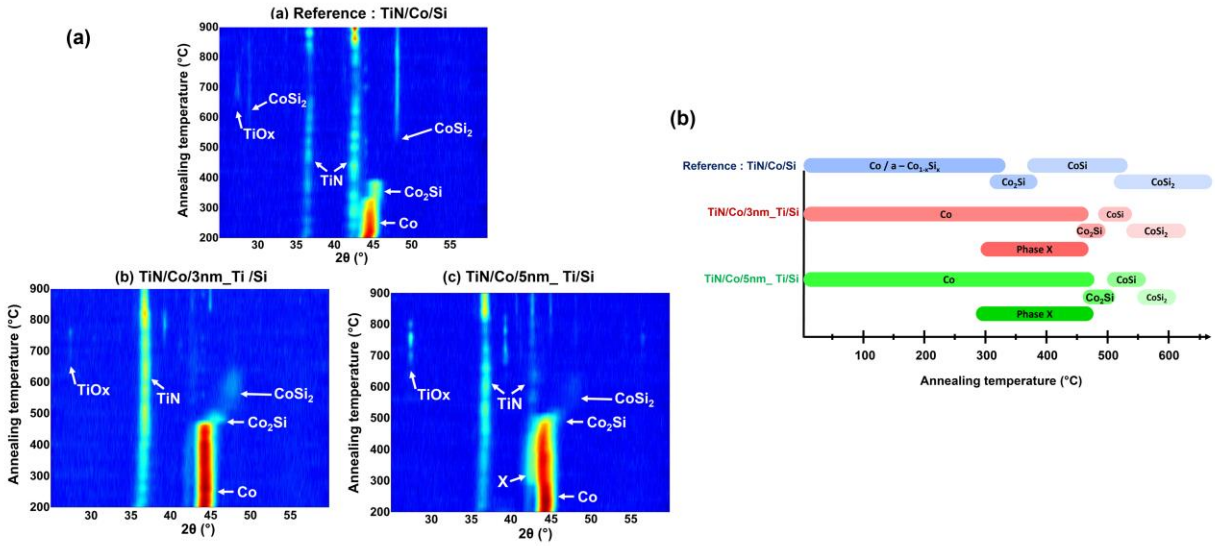

Fig. 1 (a) XRD patterns and (b) Schematic of phase formation, as a function of annealing temperatures for reference, and 3nm & 5nm Ti samples.

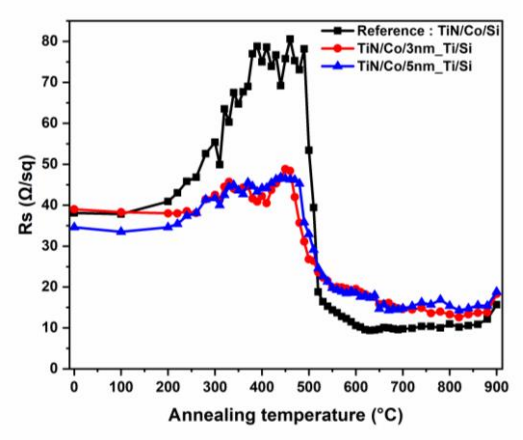

Fig. 2 Evolution of the Rs as a function of annealing temperatures for reference, and 3nm & 5nm Ti films.

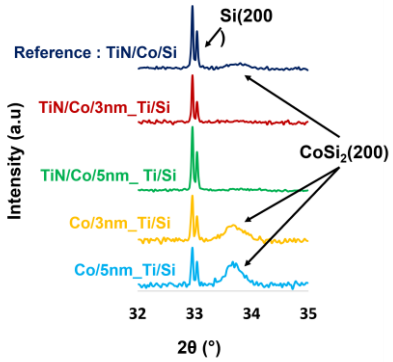

Fig. 3 XRD patterns for reference, and 3nm & 5nm Ti (with and without TiN) films annealed @ 600 °C/10 mins. .

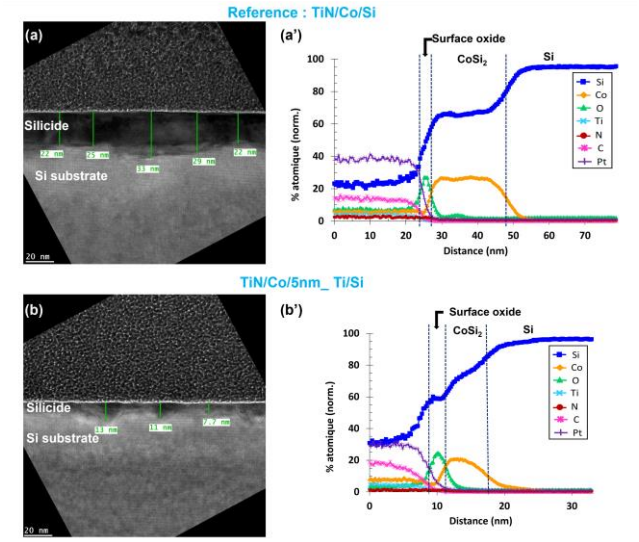

Fig. 4 TEM and EDX profile images after a Salicide process (550°C 60s/etching/790°C 20s) on samples (a and a') Reference TiN/Co/Si and (b and b') TiN/Co/5nm_Ti/Si films.

Chemical composition and thickness homogeneity of phase change materials based thin films on an industrial-scale wafer

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Phase change material (PCM), such as germanium telluride (GeTe) from the chalcogenide family, can undergo reversible transitions between amorphous and crystalline phases when subjected to optical or electrical pulses. This rapid and reversible structural transformation makes GeTe an excellent candidate for applications such as phase-change random access memory (PCRAM) [1] and photonics [2]. A significant amount of literature has been available on the synthesis and characterization of GeTe thin films; however, most of them are focused on laboratory-scale fabrication. Transitioning to an industrial scale presents challenges in having good control of chemical composition and thickness homogeneity over a large substrate area. Here, we utilize a magnetron sputtering system to deposit GeTe thin films on 200-mm Si wafers. By optimization of sputtering process, we are specifically looking for good homogeneity of chemical composition and film thickness on a large substrate area.

In this work, we aim to investigate the influence of deposition parameters on material properties of GeTe thin films, especially on chemical composition and thickness homogeneity. The GeTe films are deposited on 200-mm Si wafers using a CS400SR sputtering cluster (Von Ardenne GmbH), with variations in sputtering power and working pressure. To determine the thickness homogeneity of GeTe film, the wafers are structured using lithography and liftoff process to form multiple measurement points from the edge to the center of the wafer. These points are then analyzed using a profilometer and atomic force microscope (AFM) (Figure 1). The chemical composition of the grown layer is measured by Rutherford backscattering spectroscopy (RBS). The phase transition of GeTe layer is identified by measuring sheet resistance with a heating wafer probe. After annealing at different temperatures, the X-ray diffraction (XRD) is used for determination of the crystallized phases of samples.

The thickness homogeneity of GeTe films is minimally influenced by sputtering power but strongly dependent on deposition pressure. Deposition at a pressure of 5 µbar results in a thickness homogeneity of 8.8%, whereas higher deposition pressures result in poorer homogeneity (Figure 2). To prevent oxidation of GeTe film, a 15-nm-thick SiN_x capping layer was deposited on GeTe film. The atomic ratio of Ge/ Te in the films deposited at 200W and 5 µbar is approximately 1.2:1, indicating uniform chemical composition across the wafer (Figure 3). In contrast, higher deposition pressures cause a low Ge/ Te ratio. For annealed GeTe films, polycrystalline GeTe could be observed in low-pressure deposited layer, while high-pressure deposited layers show the presence of GeO_2 and TeO_2, which correlate with higher sheet resistance in the GeTe layer (Figure 4). At a deposition pressure of 5 µbar, the sheet resistance homogeneity is 6.8% at 200 W and 2.8% at 100 W. The transition temperature for these layers is approximately 150 °C.

Working pressure of 5 µbar is the optimum pressure to obtain GeTe thin film with the highest thickness and chemical composition homogeneities, and increasing power from 100 to 200 W increases the film crystallinity. We find the working pressure as a critical process parameter for controlling the homogeneity of chemical composition and thickness in GeTe films deposited on 200-mm Si wafers. It is mainly due to fact that the working pressure has a direct effect on the sputtering yield difference between Ge and Te atoms. The findings obtained from these analyses will provide an experimental guidance for developing potential applications, such as GeTe-based phase-change random access memory and photonic devices.

References

1. Jiang, Y.; Wei, T.-r.; Shi, X., Materials Today Physics 36,101167(2023).
2. Nisar, M.S.; Yang, X.; Lu, L.; Chen, J.; Zhou, L., Photonics 8, 205(2021).

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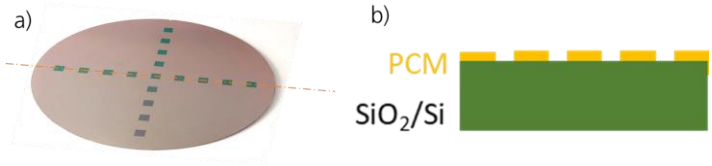

Figure 1. a) overview and b) cross section of the 200-mm wafer

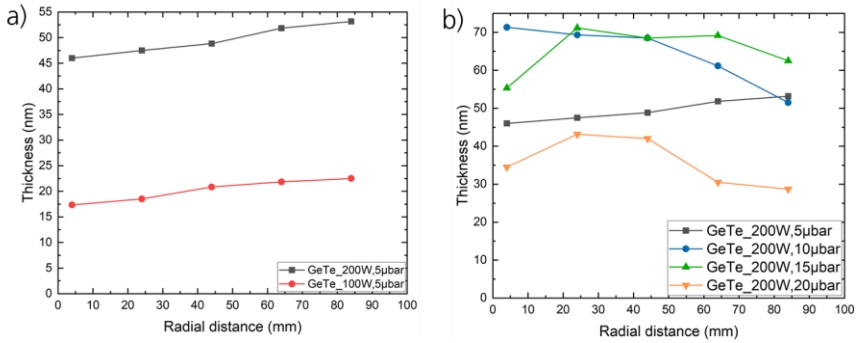

Figure 2. Thickness homogeneity of GeTe film deposited at various power a) and pressure b)

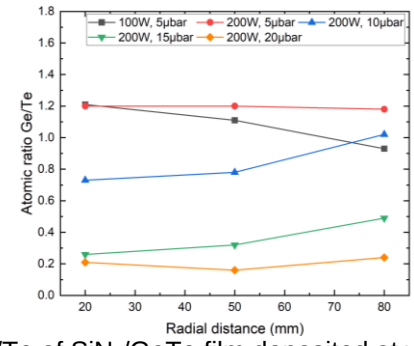

Figure 3. Atomic ratio Ge/Te of SiN_x/GeTe film deposited at various power and pressure

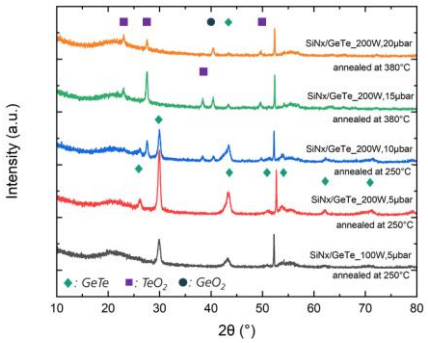

Figure 4. XRD spectra of annealed SiNx/GeTe films

Fabrication of RF device using Intercalated Multilayer Graphene / Nickel Layered Conductor

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With the recent advances in IoT, more RF devices such as antennas and inductors are required. However, the miniaturization of RF devices using conventional metals like copper (Cu) is reaching its limits because the required length and area are determined by magnetic inductance. Unlike conventional metals, graphene has a large kinetic inductance due to its unique carrier transport with long mean free path. Therefore, graphene is expected to be effective in down scaling of RF devices. [1] Previously, we reported that a conductor structure of intercalated multilayer graphene (I-MLG) stacked on a magnetic nickel (Ni) layer reduces the patch antenna area by 66%. [2] In this study, an open stub was fabricated using highly crystalline MLG-CVD and stable $MoCl_5$ intercalation to investigate the potential of size scaling.

Fig. 1 shows a cross-section of the I-MLG / Ni layered structure. Ni layer works as a catalyst for MLG CVD and it also acts as a “magnetic core” since the current is expected to flow the surface through I-MLG layer due to the skin effect at high frequency.

Patterns fabricated with Cu, Ni and I-MLG/Ni are shown in Fig. 2. The quarts glass substrate (1.0 cm × 1.0 cm) surfaces were first cleaned by organic cleaning and then nickel (Ni) film with a thickness of 1μm was deposited by the DC magnetron sputtering. Then, the Ni was patterned by photolithography and wet etching to fabricate the pattern as shown in Fig. 3. MLG-CVD was then performed at 900°C to form MLG films with good film quality using a split precursor supply method developed to improve crystallinity and uniformity, as shown in Fig. 4. [3] Then, $MoCl_5$ intercalation doping was performed at 300°C. Fig. 5 shows a comparison of the G-band shifts in the Raman spectra after intercalation. The shift of the G-band to higher wavenumbers indicates doping. Finally, the pattern was connected to the measurement substrate and connected to a network analyser as shown in Fig. 6.

Fig. 7 shows the transmission characteristics measured with the network analyzer for the Cu, Ni, and I-MLG / Ni stubs. The stub is an open-ended transmission line that is connected in parallel to the main line. In Cu, a peak was obtained at 3.6 GHz. In Ni, the peak was shifted to 3.2 GHz due to the high magnetic permeability. In I-MLG/Ni, a peak was obtained at 3.5 GHz. In an open stub, the length of the line is expressed as 1/4 of the wavelength, at which the peak occurs. The frequency is inversely proportional to inductance and capacitance. Since the capacitance is considered to be the same, this peak shift is considered due to the increased inductance due to the I-MLG / Ni structure. The shift was less than that of Ni, however, the loss seems to be less than that of Ni probably due to the lower resistance than Ni. Table 1 shows the resistance measured with four-terminal method for the Cu, I-MLG / Ni, and Ni. I-MLG / Ni had a higher resistance than Cu, and it is most likely caused the peak intensity of I-MLG / Ni to be 8.7 dB smaller than that of Cu.

In this study, we investigated the possibility of I-MLG / Ni structure by a MLG CVD process and doping of $MoCl_5$ intercalation for RF devices. This structure resulted in a resonance frequency shift indicating the possibility of size reduction, although the effect is less than expected from the previous antenna probably due to the lower frequency and thinner I-MLG thickness. Further improvements will be expected at higher frequencies due to thinner skin depth and with thicker I-MLG which is expected to increase the current through I-MLG layer. The developed structure is expected to be applied to the miniaturization of RF devices beyond the limits of conventional metals with further improvements.

References

1. J. Kang, Y. Matsumoto, X. Li, J. Jiang, X. Xie, K. Kawamoto, M. Kenmoku, J. H. Chu, W. Liu, J. Mao, K. Ueno, and K. Banerjee, Nature Electronics, **1**, 46-51(2018).
2. K. Ueno, K. Masukawa and S Tanaka, Ext. Abst. 2024 Int. Conf. Solid State Dev. Mat. (SSDM), pp.143-144.
3. K. Masukawa, K. Ueno, Abst. Adv. Met. Conf. (ADMETA Plus 2023), 7-3.

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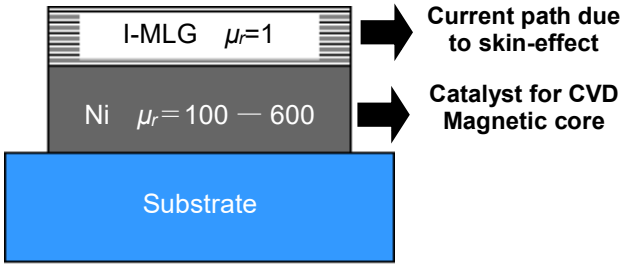

Fig. 1. Cross-section of the I-MLG /Ni layered structure. Higher inductance density is expected with kinetic inductance of I-MLG and magnetic Ni layer.

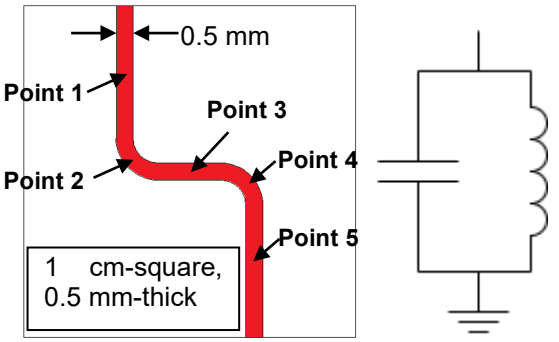

Fig. 2. Stub pattern designed and fabricated and equivalent circuit at a resonance frequency

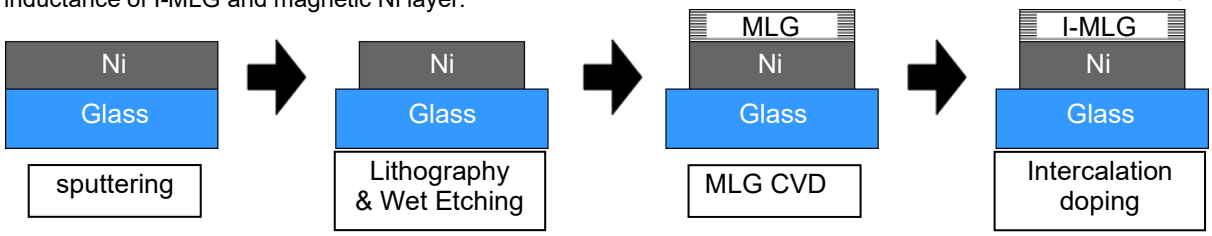

Fig. 3. Fabrication process flow of I-MLG / Ni layered structure. Highly crystalline MLG can be deposited on Ni.

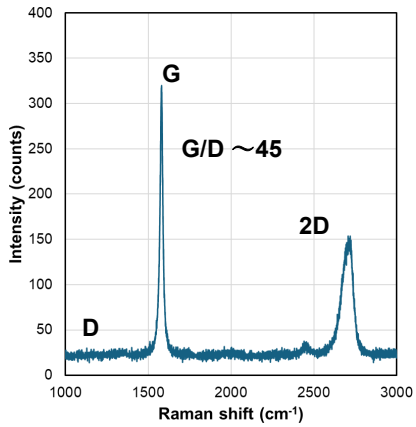

Fig. 4. Raman spectrum after CVD. Highly crystalline MLG was deposited.

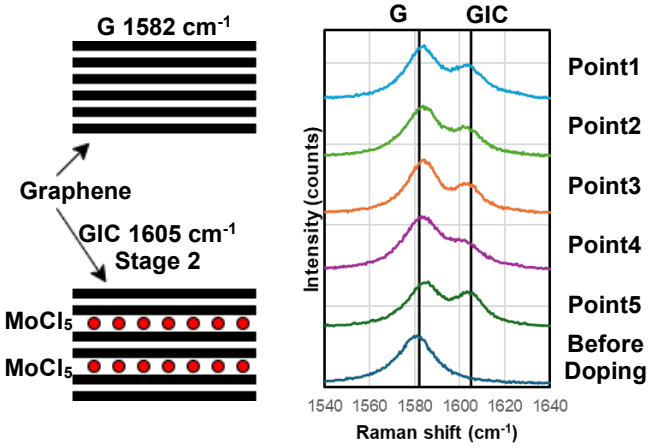

Fig. 5. Raman spectra after intercalation doping. Uniform doping was achieved on the entire pattern.

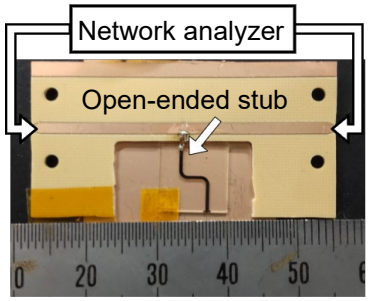

Fig. 6 Photo of fabricated I-MLG / Ni stub connected to measurement substrate.

Table 1. Comparison of sheet resistance between Cu, I-MLG/Ni, and Ni.

Conductor	Sheet resistance (Ω/sq)
Cu	0.021
I-MLG/Ni	0.111
Ni	0.309

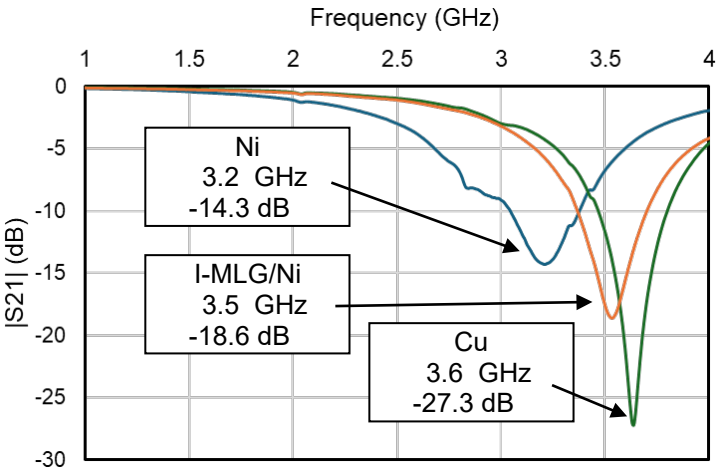

Fig. 7. Transmission coefficient of fabricated Cu, I-MLG / Ni, and Ni open stub. Peak shift of I-MLG / Ni was less than that of Ni, however, the loss seems to be less than that of Ni.

Investigation of Nano-Carbon Cap Formation on Ruthenium by Low Temperature Thermal CVD

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Graphene-capped copper (Cu) interconnects have attracted attention as a candidate for next-generation low-resistance nano-interconnects. [1] It has also been reported that coating ruthenium (Ru) surfaces with graphene reduces the resistance. [2] We previously attempted to form graphene caps on 30 nm Ru films by thermal CVD, but no carbon deposition was observed. [3] The purpose of this study is to apply thermal CVD to Ru to deposit nano-carbon (NC) caps and investigate their potential as NC / Ru low-resistance nano-interconnects.

Ru films of 10, 20, 30, and 50 nm thickness were sputter-deposited on a 100 nm thick thermally oxidized Si substrate (8 inches). Tantalum (Ta) of 3 nm thickness was deposited as an adhesive layer before Ru sputtering. 1 cm square substrates were placed in the quartz tube of the previously described CVD system [3] and heated in an electric furnace to a set temperature of 400 °C in an Ar atmosphere at normal pressure, and once the set temperature was reached, ethanol bubbled with Ar was supplied for 20 minutes, and the CVD was performed under the conditions shown in Table 1. For comparison, samples annealed without ethanol flow and samples annealed under a vacuum condition (1.24×10^{-2} Pa) were prepared. For evaluation, Raman spectroscopy was used to examine NC deposition, and a four-point probe method was used to measure sheet resistance before and after CVD or annealing. XPS were used for analysis.

Fig. 1 shows Raman spectra after CVD at Ru 30 nm with varying precursor supply rate; no carbon deposition was observed at 100 sccm and 300 sccm, while G- and D-band features were observed above 500 sccm, indicating NC film deposition. On the other hand, no clear precursor supply rate dependence was observed from 500 sccm to 1000 sccm. Since no clear 2D-bands were observed, the deposited films are considered as less crystalline and closer to amorphous carbon. Fig. 2 shows the Raman spectra after CVD with Ru film thickness varied from 10 nm to 50 nm, and no NC deposition was observed on 10 nm- and 20 nm-thick Ru. On the other hand, the intensity of the G- and D-bands increased at 50 nm. This indicates that the activity of Ru as a catalyst increases with increasing film thickness. Fig. 3 shows the resistivity for each Ru film thickness before and after CVD; reduction in resistivity was observed for the samples after CVD and annealing, which is considered due to Ru grain growth. No reduction in resistivity was observed with the carbon film deposition. Fig. 5 shows XPS spectra of Ru after CVD or annealing. The surface spectrum after annealing in Ar atmosphere was shifted toward RuO_2 compared to that after CVD, suggesting surface oxidation. In this experiment, the surface oxidation of Ru may have been caused by residual oxygen during annealing, but it is also possible that the oxidized Ru was reduced by the ethanol gas flow. It has been reported that Ru surface oxidation affects the electrical and chemical properties of the interface with the NC film [4], and since it is considered important to remove the oxide film at the interface, it is necessary to establish a CVD process to remove the oxide film on the Ru surface in the future.

In this study, we investigated the possibility of NC-cap formation by thermal CVD on Ru for nano-interconnect application. By increasing the precursor supply, NC caps were successfully deposited on 30 nm Ru, but no NC was deposited on Ru thinner than 30 nm. In addition, no reduction in resistivity with NC-caps was observed probably due to the oxidation of interface between the NC-cap and Ru. Further process improvement to remove Ru-oxide at the interface of NC and Ru will be necessary in the future.

References

1. L. Li, Z. Zhu, A. Yoon, H.-S. P. Wong, IEEE Electron Device Lett. **40**, 815 (2019).
2. S. Achra, *et al*., Carbon **183**, 999 (2021).
3. T. Fukuda, Y. Temmyo, and K. Ueno, 2024 MAM (Milan, 2024)
4. S. Achra, *et al*., Applied Surface Science **538**, 148046 (2021).

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Table 1. CVD conditions.

CVD (Annealing) Temperature (℃)	400
Precursor flow-rate (sccm)	100 , 300 , 500 , 700 , 1000
Ethanol supply-time (min.)	20

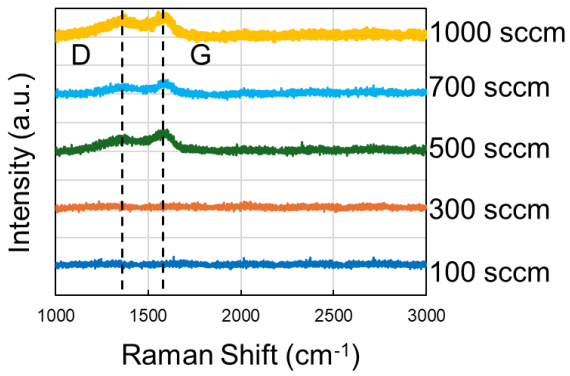

Fig. 1. Raman spectra after CVD between 100 sccm and 1000 sccm on 30 nm-thick Ru.

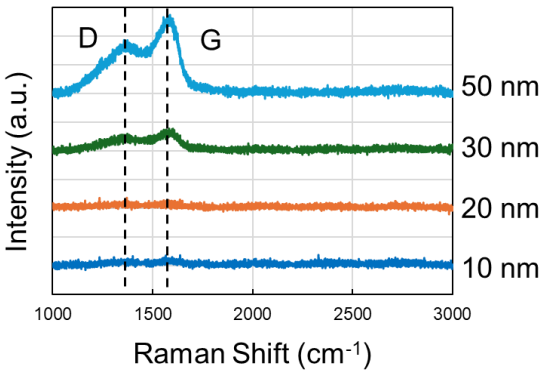

Fig. 2. Raman spectra after CVD between 10 nm- and 50 nm-thick Ru.

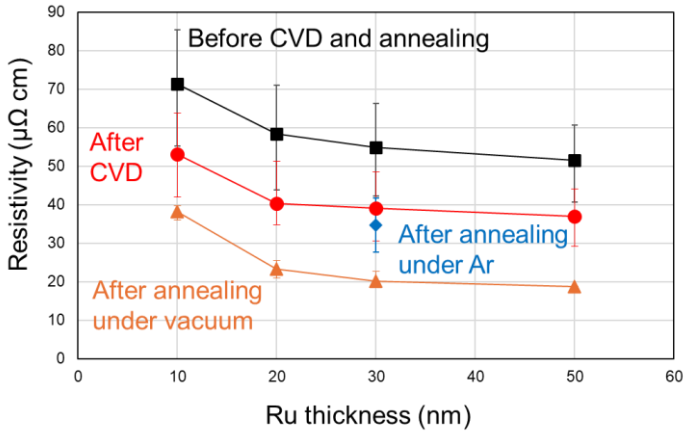

Fig. 3. Resistivity changes of Ru before and after CVD or annealing. Variations in resistivity before CVD or annealing may be due to variations in film thickness. Resistivity is calculated by the total thickness of the Ru and Ta layers.

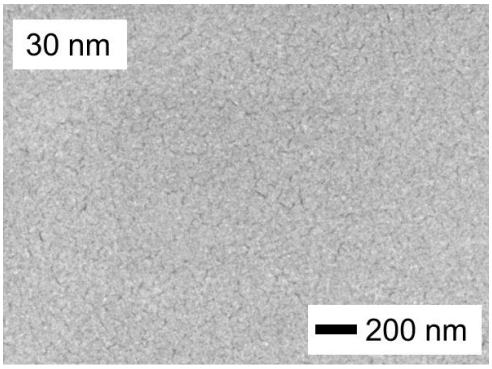

Fig.4. Surface SEM image of NC/Ru of 30 nm-thick Ru after CVD. There is no CNT-like formation on the surface, and NC is considered to be uniformly formed.

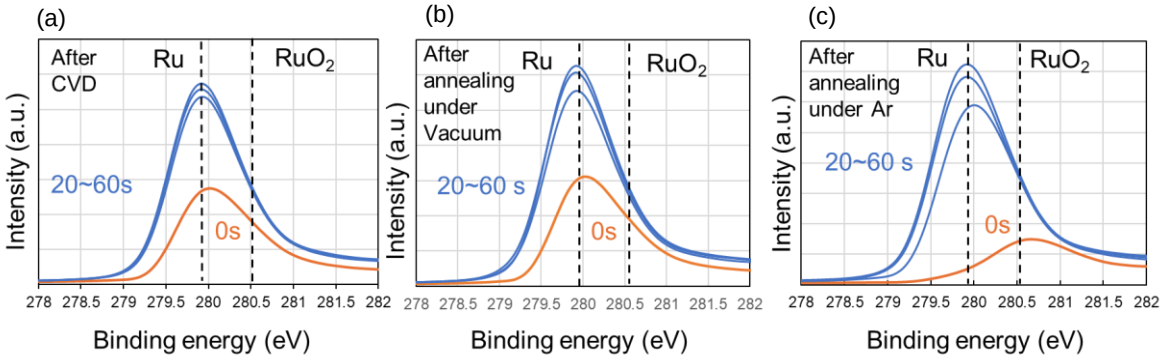

Fig. 4. XPS spectra after (a) CVD, (b) annealing under vacuum, and (c) after annealing under Ar atmosphere.

Reduced compositional fluctuations in epitaxial NiAl layers

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As interconnect dimensions scale down, it is well established that the resistivity of Cu increases significantly due to enhanced electron scattering at surfaces and grain boundaries. These effects, coupled with the challenges associated with metallizing sub-10 nm interconnect lines and the difficulty of scaling diffusion barriers in advanced technology nodes, present substantial limitations for future copper-based metallization schemes. Consequently, there is growing interest in exploring alternative materials and metallization strategies for next-generation interconnects. Extensive investigations have been conducted in recent years, both on elemental metals and binary intermetallic compounds, to identify suitable candidates for this application [1, 2].

NiAl has emerged as a promising binary intermetallic candidate due to its low bulk resistivity of 9 μΩcm, negligible diffusion into SiO_2, and strong adhesion with common dielectrics. These characteristics make NiAl a potential option for barrier- and liner-free interconnects [3]. However, a critical limitation of NiAl is its susceptibility to compositional fluctuations, which are detrimental to thin film and interconnect resistivities, severely hindering its practical implementation as a next-generation interconnect material [4]. Moreover, the length scale of these fluctuations is on the order of the targeted interconnect line width, significantly affecting etch and clean processes. Addressing this issue necessitates advanced characterization techniques to elucidate the underlying mechanisms driving these inhomogeneities. It has been demonstrated that the growth of epitaxial NiAl on (100) Ge substrate reduces resistivity by optimizing the grain microstructure [5].

In this work, we study potential compositional inhomogeneities in epitaxial NiAl thin films. Epitaxial NiAl (100) layers were deposited by co-sputtering at 420°C onto 500 nm thick strain-relaxed chemical vapor deposition (CVD) Ge grown on 300 mm Si (100) wafers. The microstructure and compositional uniformity of the films were characterized using advanced techniques including atom probe tomography (APT), which enabled the assessment of the spatial distribution of the atomic composition. The spectrum obtained from a 5-nm-thick cylindrical region of interest (ROI) (Figure 1) indicates a stoichiometric composition within the sample. A ~2% Ge content observed within the ROI arises from interdiffusion at the NiAl/Ge interface.

Structural analysis, including X-ray diffraction (XRD) θ-2θ scans and reciprocal space mapping (RSM), confirms the high-quality epitaxial growth of NiAl. The out-of-plane orientation was determined to be NiAl (100) ‖ Ge (100) ‖ Si (100), with an in-plane relationship of NiAl (010) ‖ Ge (010) ‖ Si (010). RSM data for NiAl (202) (Figure 2) reveals lattice constants corresponding to less than 1% deviation from the bulk NiAl lattice parameter (a_0=2.86 Å), indicating a relaxed epitaxial structure.

Figure 3 presents the concentration profile along the length of the sub-cylinder, revealing an uniform distribution of Ni and Al. Furthermore, a compositional histogram (Figure 4), calculated using a 2nm radius around each reconstructed atom, demonstrates significantly reduced fluctuations compared to the uneven distribution observed in polycrystalline NiAl on SiO_2. The comparison with a random comparator (shuffled dataset) yields a similarly sharp peak, reinforcing the observation of a homogeneous chemical composition of the epitaxial NiAl.

This strain-free epitaxial configuration is identified as a primary factor contributing to the significant reduction in compositional fluctuations, highlighting the advantages of such strain-free epitaxial intermetallics for advanced interconnect applications.

References

1. D. Gall, J. Appl. Phys. **127**, 050901 (2020).
2. J-Ph. Soulié *et al.*, J. Appl. Phys. **136**, 171101 (2024).
3. L. Chen *et al.*, Appl. Phys. Lett. **113**, 183503 (2018).
4. C. Adelmann *et al.*, 2023 IEEE Intern. Interconnect Technol. Conf. (IITC), pp. 1-3 (2023).
5. J-Ph. Soulié *et al.*, 2022 IEEE Intern. Interconnect Technol. Conf. (IITC), pp. 73-75 (2022).

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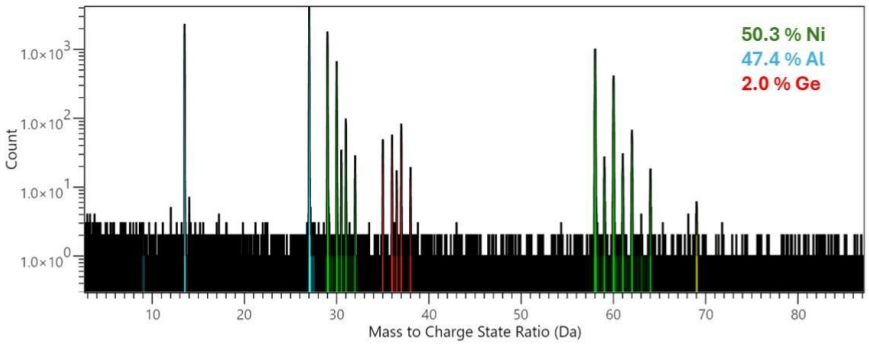

Figure 1: Mass to charge state ratio spectrum in the sub-cylindrical region.

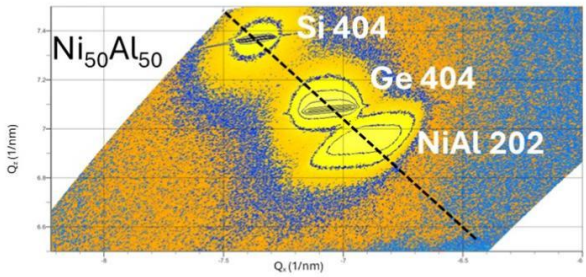

Figure 2: Reciprocal space mapping of Si (404), Ge (404) and NiAl (202).

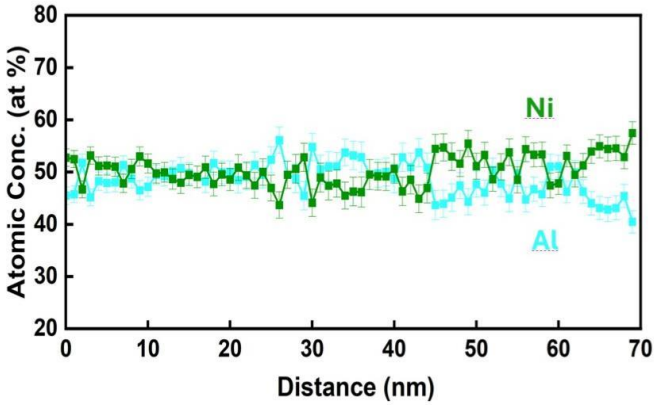

Figure 3: Atomic concentration distribution as a function of distance.

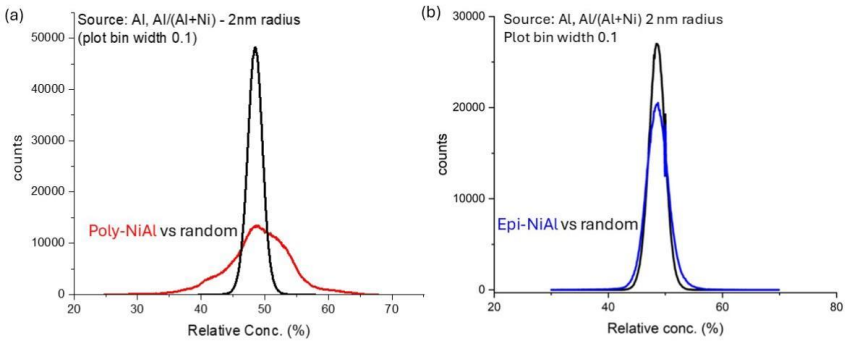

Figure 4: Measured relative concentration in the (a) polycrystalline and (b) epitaxial NiAl thin films compared with the randomly shuffled data.

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