



Technology Manufacturing Engineering

TME EMEA Collaboration Program

Making High Impact technologies happen

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Intel Confidential

Outlook

- **TME EMEA Program Milestones**
- **The collaboration model-key competence**
- **Intel technology Development Process**
- **Future Tech Areas of Interest**
- **Engagements**

Intel's global operations



The Intel EMEA TME Program milestones



- Launched at 1996 driven by an agreement with the Government of Israel to drive commercialization /development of Israeli goods and technology based services.
- Developed evaluation / collaboration practices and BKMs , strongly supported by the Israeli Intel Fabs / resources. (Beta projects, engineering support).
- Qualified >50 suppliers to Intel and supported >100 technology initiatives
- Intel Israel industry development program has reached its 10th year with total of > \$1.5B accumulated program driven sales

The EMEA TME program milestones cont..



- Europe based TME enabling activity started at September 2003. operates under tight alignment & interaction with the TME US
- EMEA - Intel Capital (venture capital arm) and TME operations joined forces for close collaboration to best support the European Semi industry needs.
- The collaboration framework with industry associations and Intel EMEA Fabs is in place, program operates as the TME front line, enabling force in Europe .

The Commercialization mission



The potential contribution of intellectual property and \$\$\$ invested in research

The commercialization efforts in the region will:

- Add value to inventors & universities thus stimulate further innovation
- Bring benefits to Intel and the market from new discoveries
- Support economic development in this region
- Foster entrepreneur spirit to encourage new companies formation

TME EMEA Collaboration Model A Commercialization Proven Method



The charter is to Enable new or improved **technologies** for Intel and the Semiconductor Industry by fusion of Intel leadership & resources with the EMEA technological innovation

The objective is to Identify and execute upon high-value Si related engagement opportunities with the potential to significantly impact Intel core business

Focus on OGA (one generation ahead)

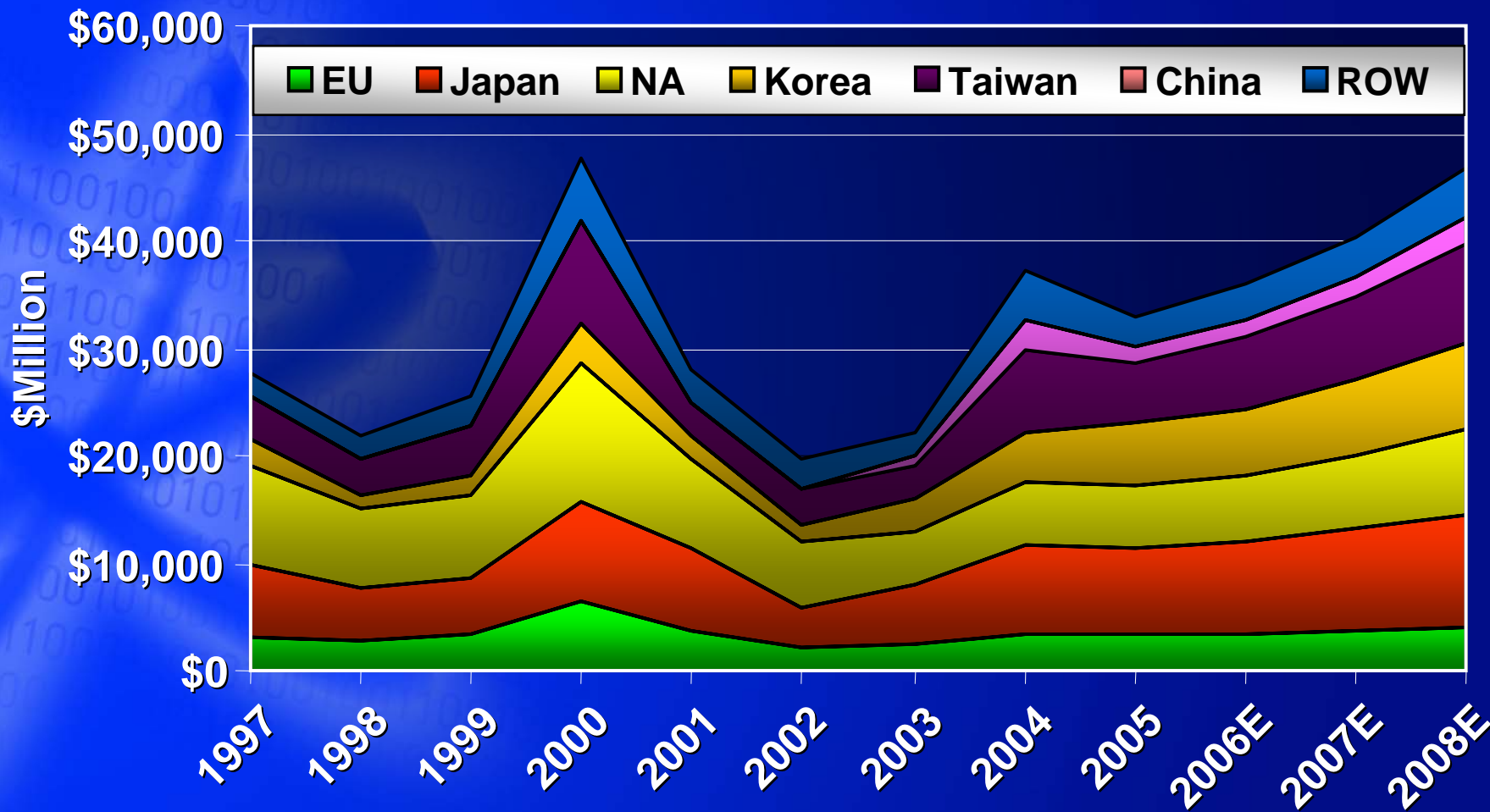
Focus on making high-impact technology collaboration happen



- **Pro-actively source & develop high-impact opportunities**
 - **Joint work by TME EMEA and Intel Investment Arm to support Intel's supply chain and supplier ecosystem**
 - **Engage with R&D institutes for spin-offs with unique, 'best-in-class' technology**
- **Shape engagement structures, build & facilitate syndicates to support production ramp , lead technology/application development and product improvement.**
 - **Engage with Corporate Collaboration Programs**
- **Support companies growth by making them investment ready**
 - **Pre-investment technology development activity**
- **Bring in the local, cultural perspective**

From Idea to Commercialization

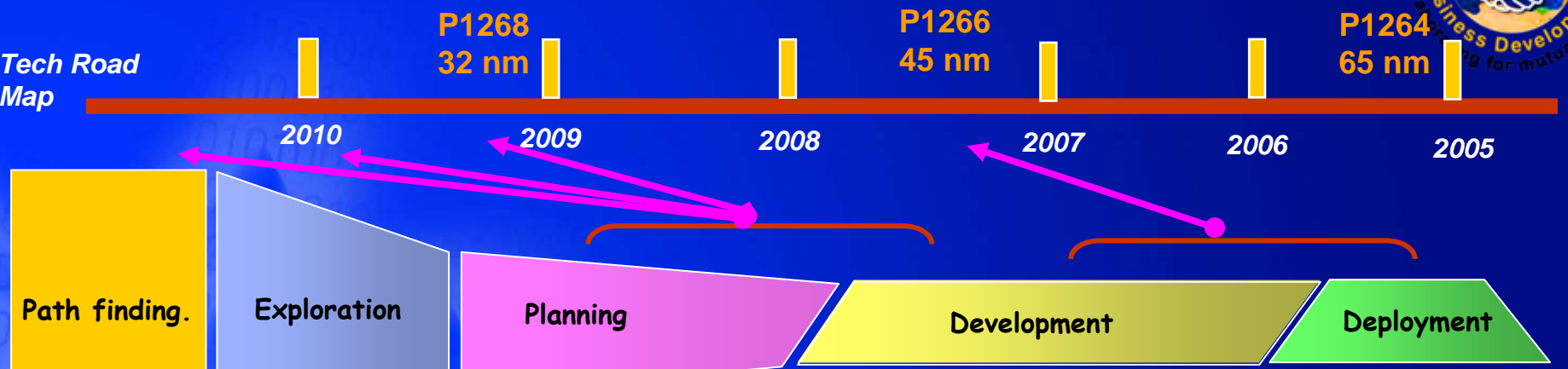
Semi Equipment Sales Forecast



Source: SEMI, 12/05



The Development Process methodology

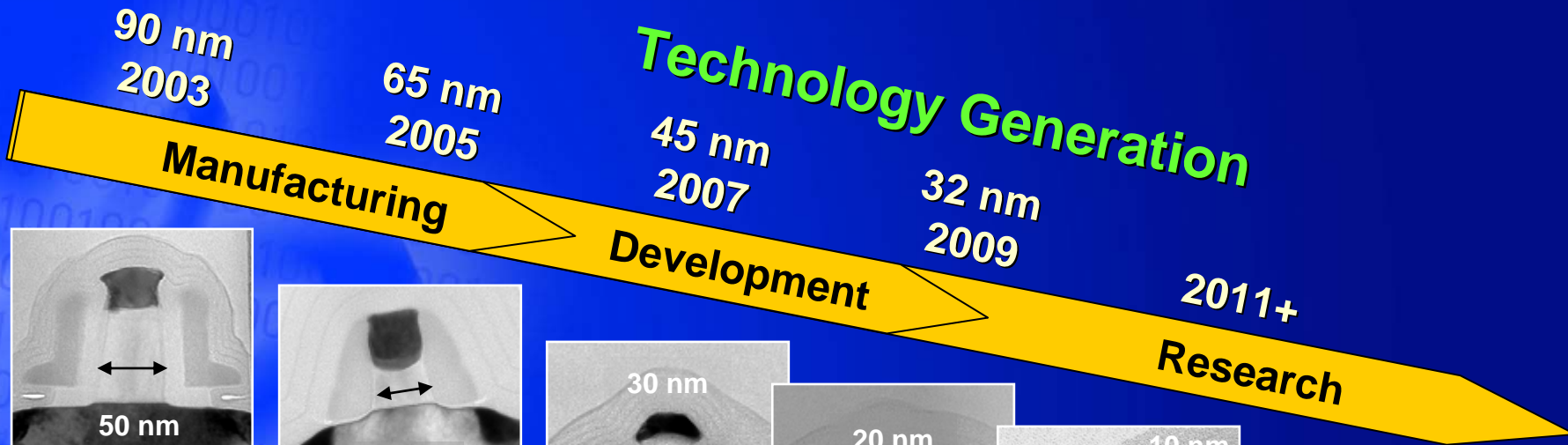


- ISTG Roadmap
- Mobility For Mfg Roadmap
- MOSCS Roadmap
- FSM Research Roadmap



Innovation Transistor Nanotechnology

Technology Generation



90 nm
2003

65 nm
2005

45 nm
2007

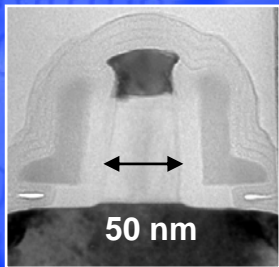
32 nm
2009

2011+

Manufacturing

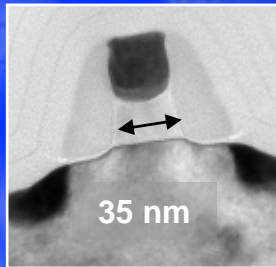
Development

Research



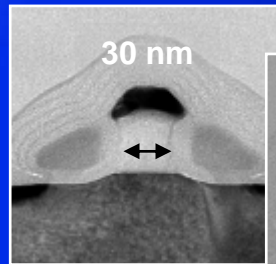
50 nm

SiGe S/D
Strained
Silicon



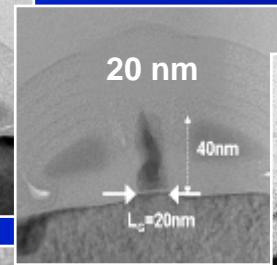
35 nm

SiGe S/D
Strained
Silicon



30 nm

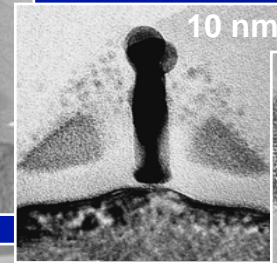
Metal Gate



20 nm

High-k

Si Substrate

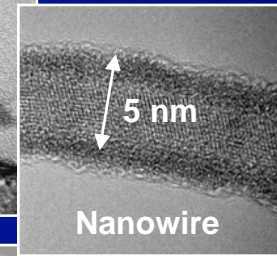


10 nm

Tri-Gate

S D S

G III-V



5 nm

Nanowire



Carbon
Nanotube FET

Future options subject to change

2006 OGA Areas of interest



Transistor

- ❖ Alternate High k
- ❖ Alternate Metal Gate
- ❖ Dual Orientation Substrates
- ❖ III/V on Si

Interconnect

- ❖ ALD Barrier/Alternative Seed
- ❖ Direct Plating on Barrier
- ❖ Electropolish/Advanced CMP
- ❖ Alternate barrier CMP
- ❖ Lower k ILD
- ❖ Optical Interconnect
- ❖ Metallic CNT

Litho / Etch / Cleans

- ❖ Photo Resists
- ❖ EUV Resist
- ❖ Develop
- ❖ ILD Cleans
- ❖ Mask technologies

Interface / Assembly

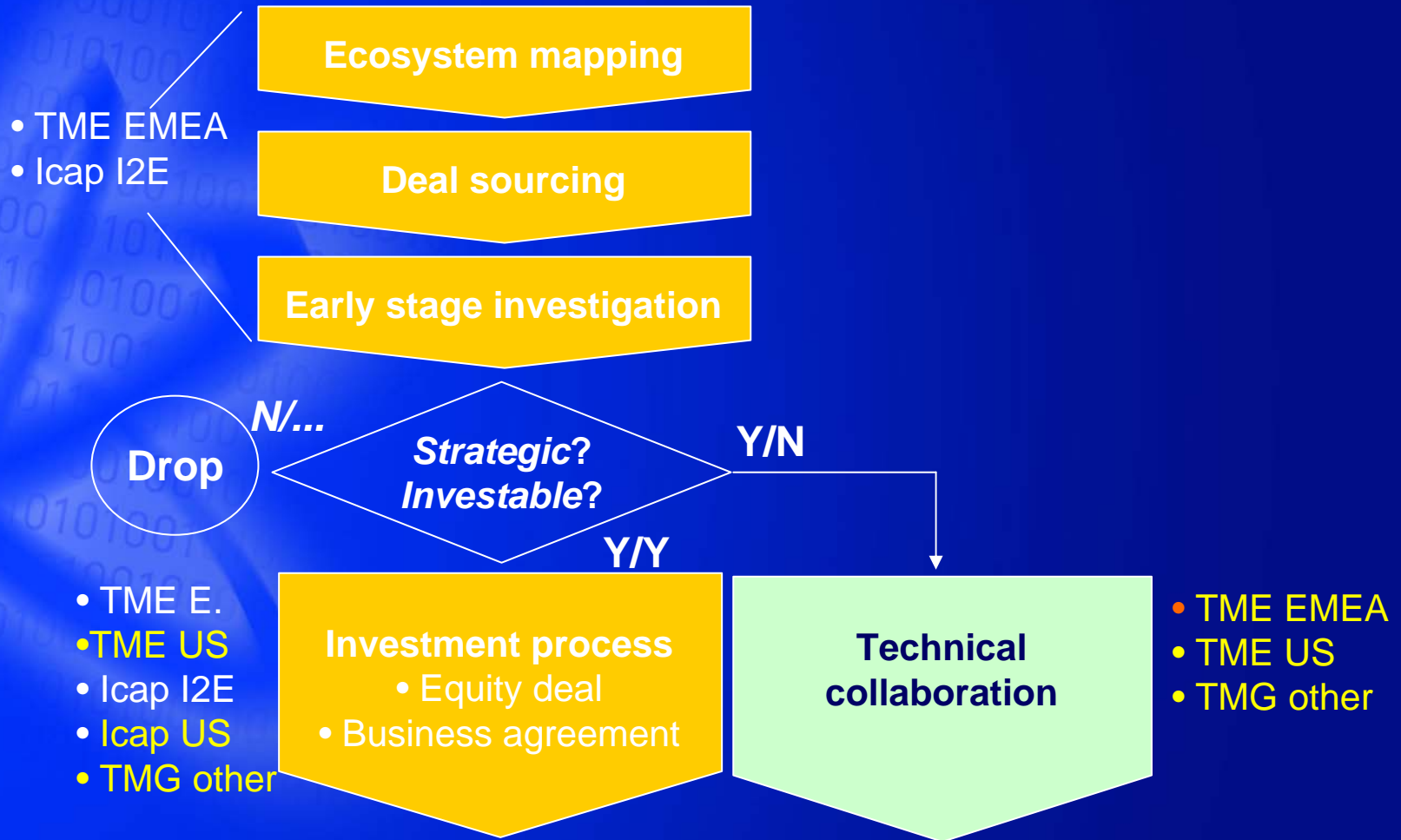
- ❖ 3D Interconnect

Metrology

- ❖ Fast e-beam defect inspection

New Materials
New Structures
New technologies

A structured enabling process by TME & Intel Capital in EMEA



A Structured approach by TME and ICap in EMEA & US

The proven way to develop next Gen. Technology

Intel TME

- Defining the Industry Long Term Barriers
- Technology early validation
- Collaboration ,Support development of specific application
- Ramp up support (Eng. &MFG)



Industry

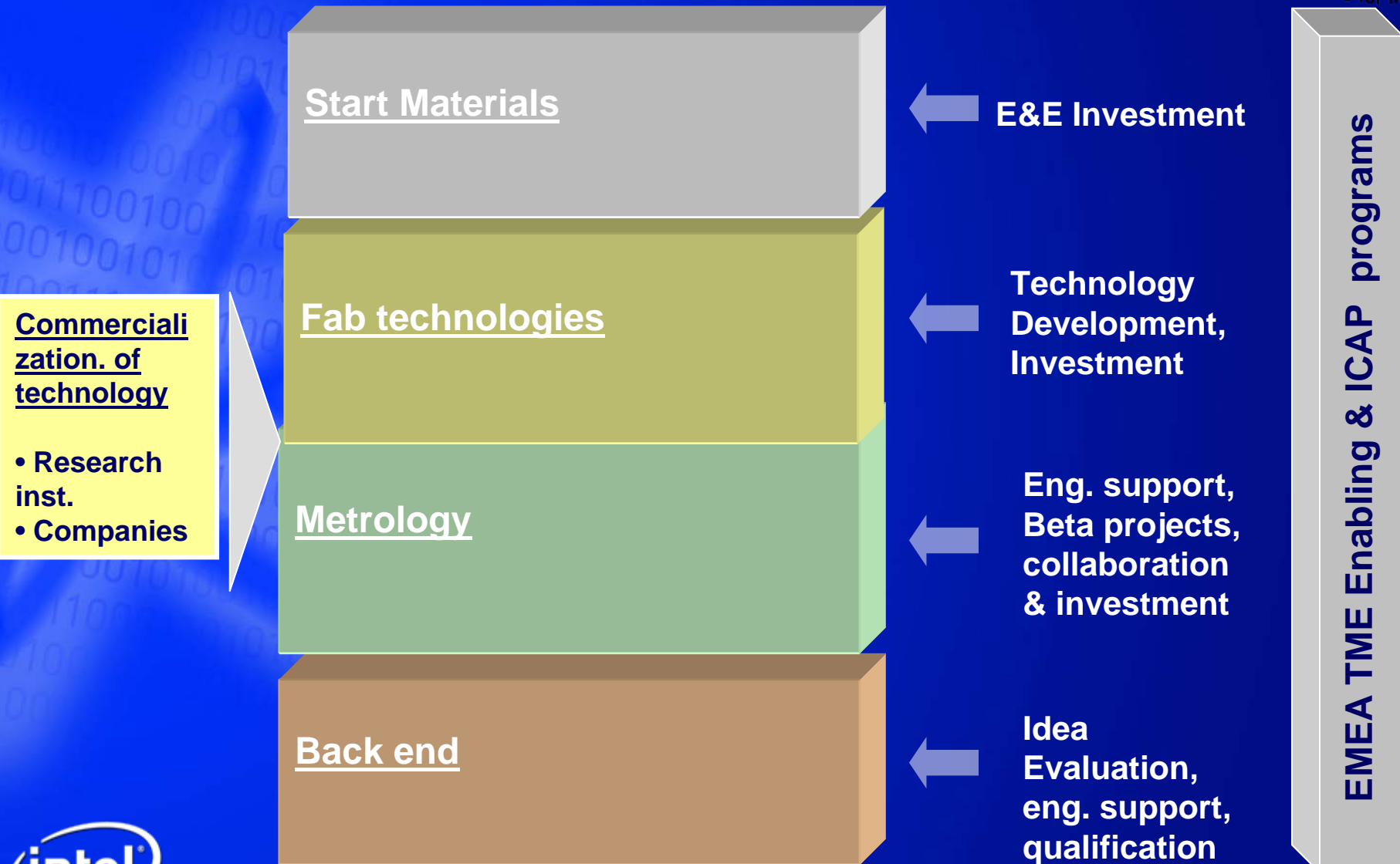
- Introduce novel ideas
- Develop innovative Technologies & Tools
- Collaboration ,focus on development of applications
- Product improvement processes
- Product affordability

The classic engagement model



<u>Engage with</u>	<u>Project Stage</u>	<u>Time to Market</u>
• Large/Med. Business	Final Product	5 months Ave.
• Large Business	After Prototype	9 months Ave.
• Medium Business	After Prototype	1.5 Yrs Ave.
• Medium Business	Before Prototype	2.5 Yrs Ave.
• Small business:	Start ups	3.5 Yrs. Ave.
• Early Stage business	Incubators	4.5 Yrs. Ave.
• Research	University	6-9 Yrs. Ave.

EMEA Portfolio impact along the Si value chain



EMEA program line-up of all TME resources Summary



The EMEA enabling arm of TME Corp. developed domain expertise in order to Keep Moore's Law going:

- We cover the entire Si chain ,support :
 - ❑ Roadmap gap fillers and OGA approach
 - ❑ Supply chain development (ecosystem)
 - ❖ Capacity & product availability
 - ❖ Intel supplier health
 - ❖ Cost reduction projects
 - ❑ Eyes & Ears
 - ❖ Adjacent & disruptive technologies.

Contact TME EMEA Team to discuss new ideas



- TME EMEA Web site
- TME EMEA program manager

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Thanks

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