Lithography Roadmap for CMOS manufacturing

S.Tedesco CEA-LETI

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Outline

- Introduction
  - Limits of optical lithography ?
- How to improve resolution?
  - k1 factor : OPC, OAI, Double Exposure
  - NA : immersion
  - λ : EUV
- Economics factor : CoO solutions
  - Maskless
  - Nanoimprint
- Conclusion
  - Roadmap

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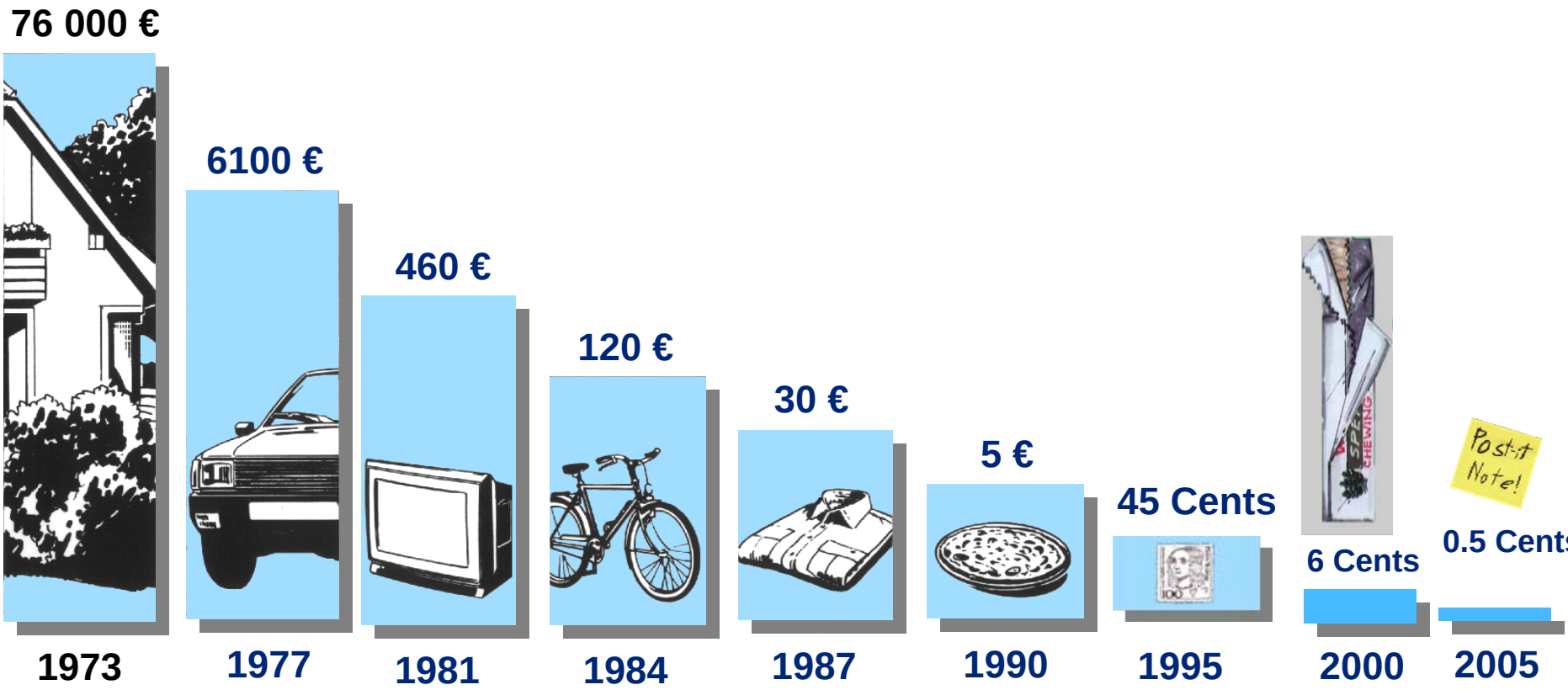
Lithography requirements : 2005 ITRS roadmap

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ pitch (nm) (contacted)	28	25	22	20	18	16	14
DRAM and Flash							
DRAM ½ pitch (nm)	28	25	22	20	18	16	14
Flash ½ pitch (nm) (un-contacted poly)	25	23	20	18	16	14	13
Contact in resist (nm)	31	28	25	22	20	18	16
Contact after etch (nm)	28	25	23	20	18	16	14
Overlay [A] (3 sigma) (nm)	5.1	4.5	4.0	3.6	3.2	2.8	2.5
CD control (3 sigma) (nm) [B]	3.0	2.6	2.3	2.1	1.9	1.7	1.5
MPU							
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	23	20	18	16	14
MPU gate in resist (nm)	19	17	15	13	12	11	9
MPU physical gate length (nm) *	11	10	9	8	7	6	6
Contact in resist (nm)	35	31	28	25	22	20	18
Contact after etch (nm)	32	28	25	23	20	18	16
Gate CD control (3 sigma) (nm) [B]	1.2	1.0	0.9	0.8	0.7	0.7	0.6
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	23	20	18	16	14
Chip size (mm^2)							
Maximum exposure field height (nm)	26	26	26	26	26	26	26
Maximum exposure field length (nm)	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858
Number of mask levels MPU	37	37	39	39	39	39	39
Number of mask levels DRAM	26	26	26	26	26	26	26
Wafer size (diameter, mm)	450	450	450	450	450	450	450

The microelectronics success story

A cost reduction unique in the industry history

PRIZE EVOLUTION OF 1 Million transistors



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Limits of optical lithography ?

- **Rayleigh criteria** :

$$R = k_1 \times \frac{\lambda}{NA} \quad with \quad NA = n \times \sin(\theta) < n$$

$$DOF = k_2 \frac{\lambda}{NA^2}$$

➔**To improve resolution we need to:**

➔**Decrease k1**
➔**Increase NA**
➔**Decrease λ**

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The K1 factor decrease

- **k_1 decrease is made through:**
  - Resist improvement
  - OPC and PSM masks
  - Off axis illumination or polarization
  - Double exposure/Double patterning

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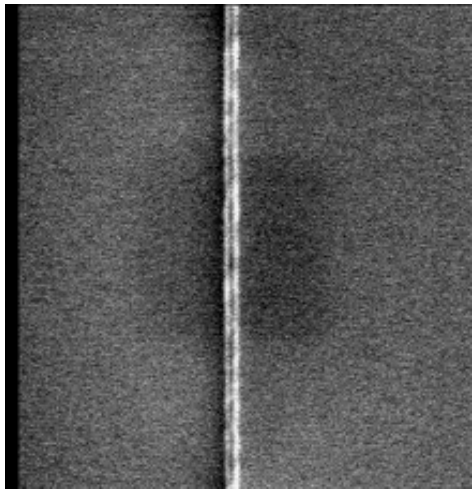
Chemically Amplified Resist

Positive resists :

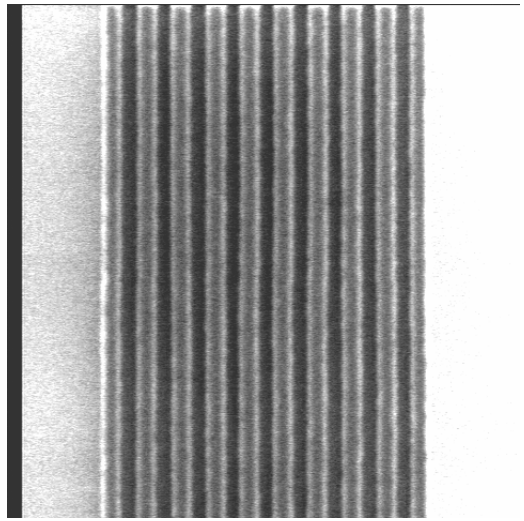
PAG $\xrightarrow{\text{exposure}}$ acid H^+ $\xrightarrow{\text{Bake}}$ PHS deprotection + H^+

Negative resists :

PAG $\xrightarrow{\text{exposure}}$ acid H^+ $\xrightarrow{\text{Bake}}$ reticulation PHS-CL + H^+



20 nm isolated line



40 nm lines and spaces

e-beam exposure at 100 kV.

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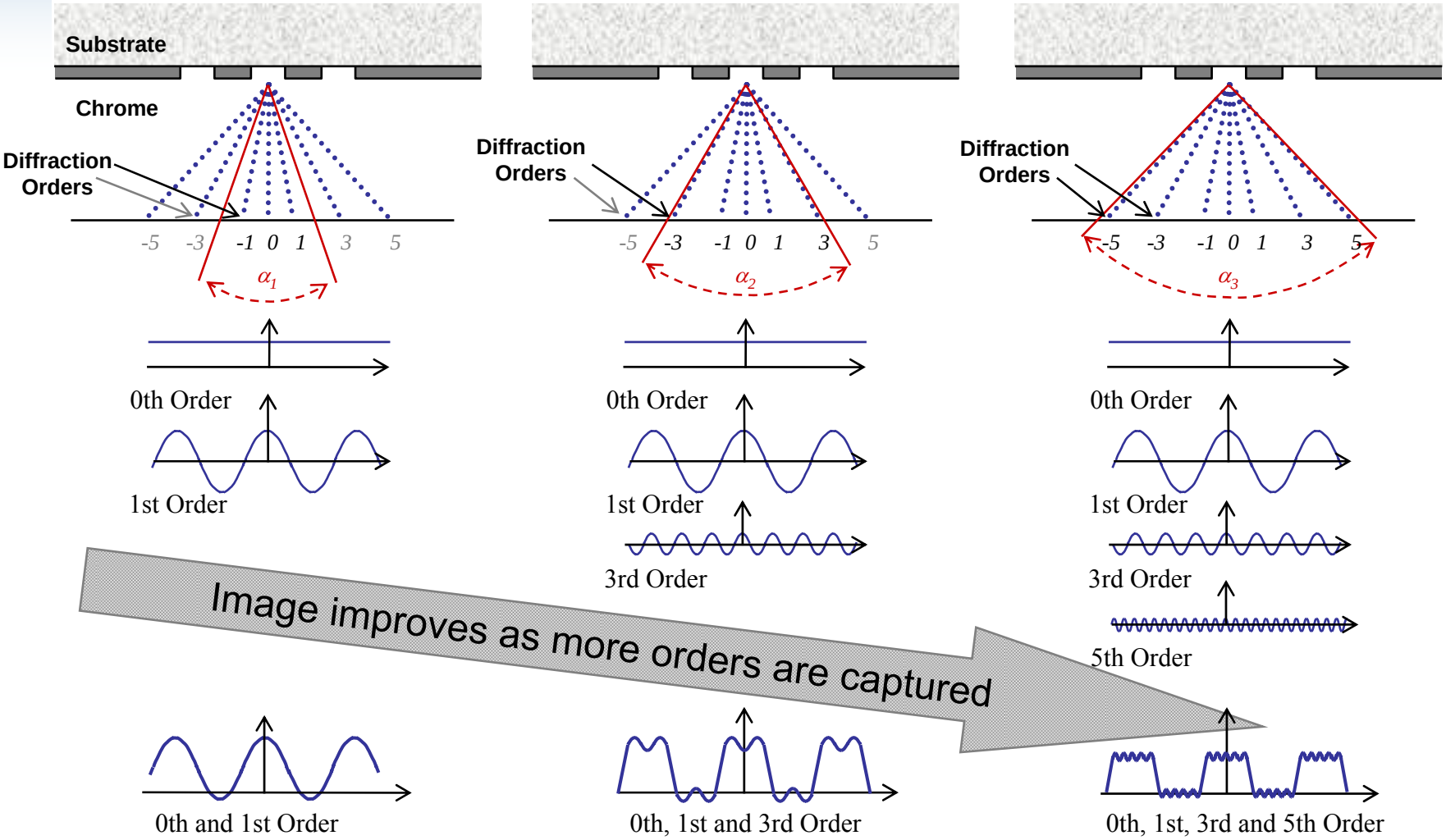
Image Capture



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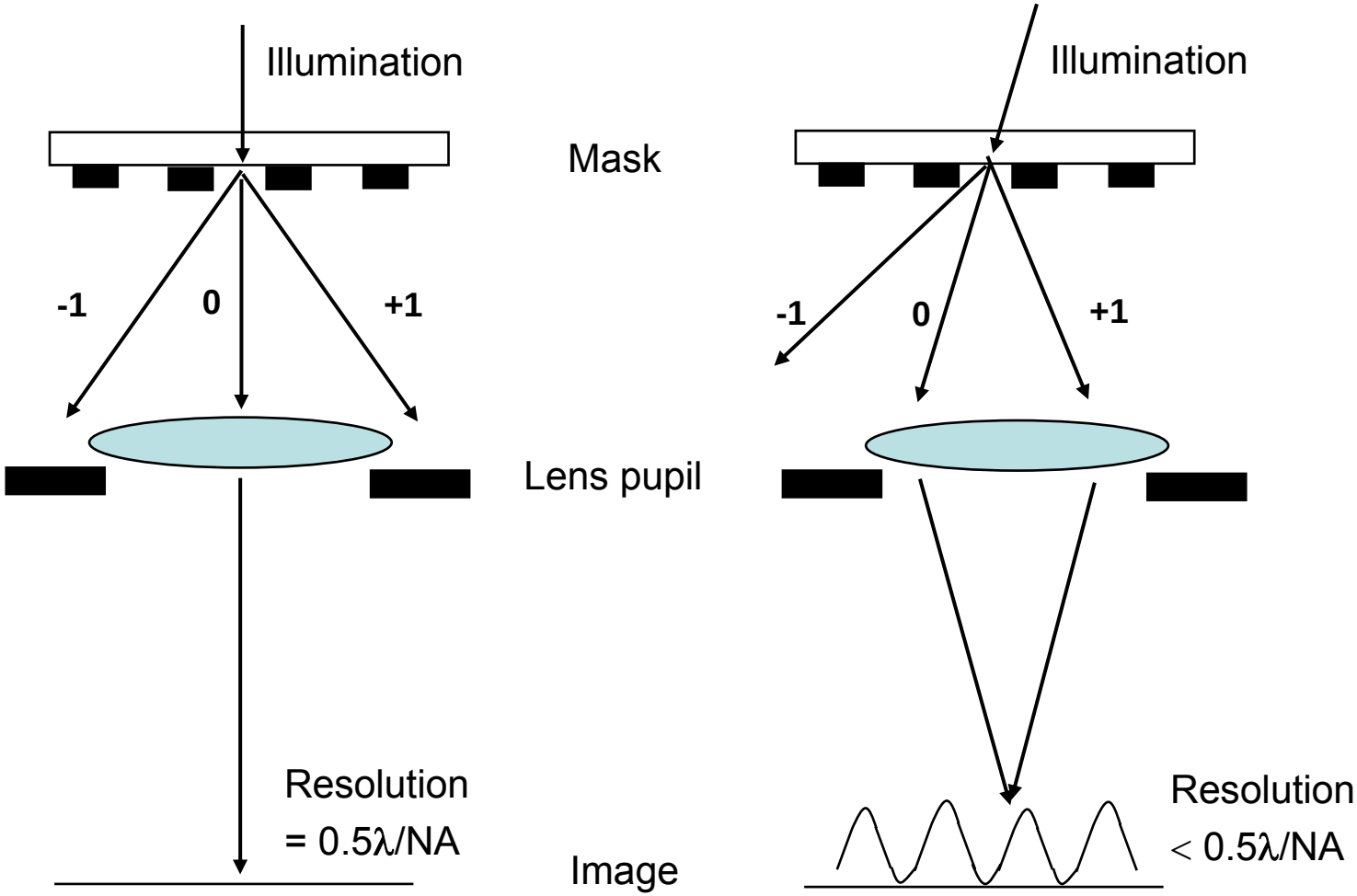
Off-Axis Illumination (OAI)

- Primarily used for improving resolution/DOF of dense features



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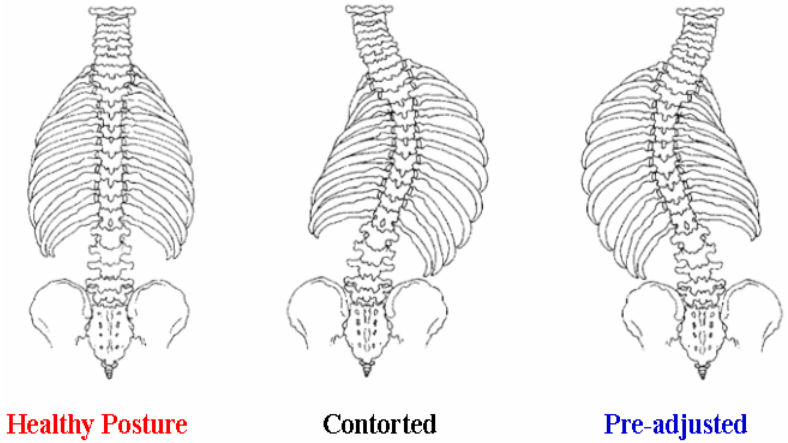
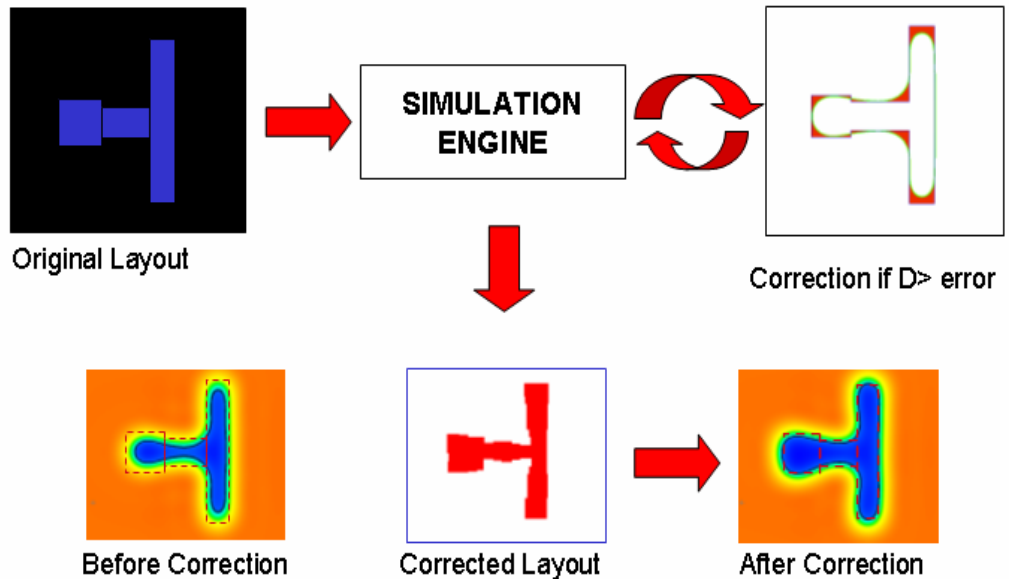
Optical Proximity Correction (OPC)

OPC : precorrect the mask to have the silicon result as close as possible to the original design





Courtesy of Y. Trouiller

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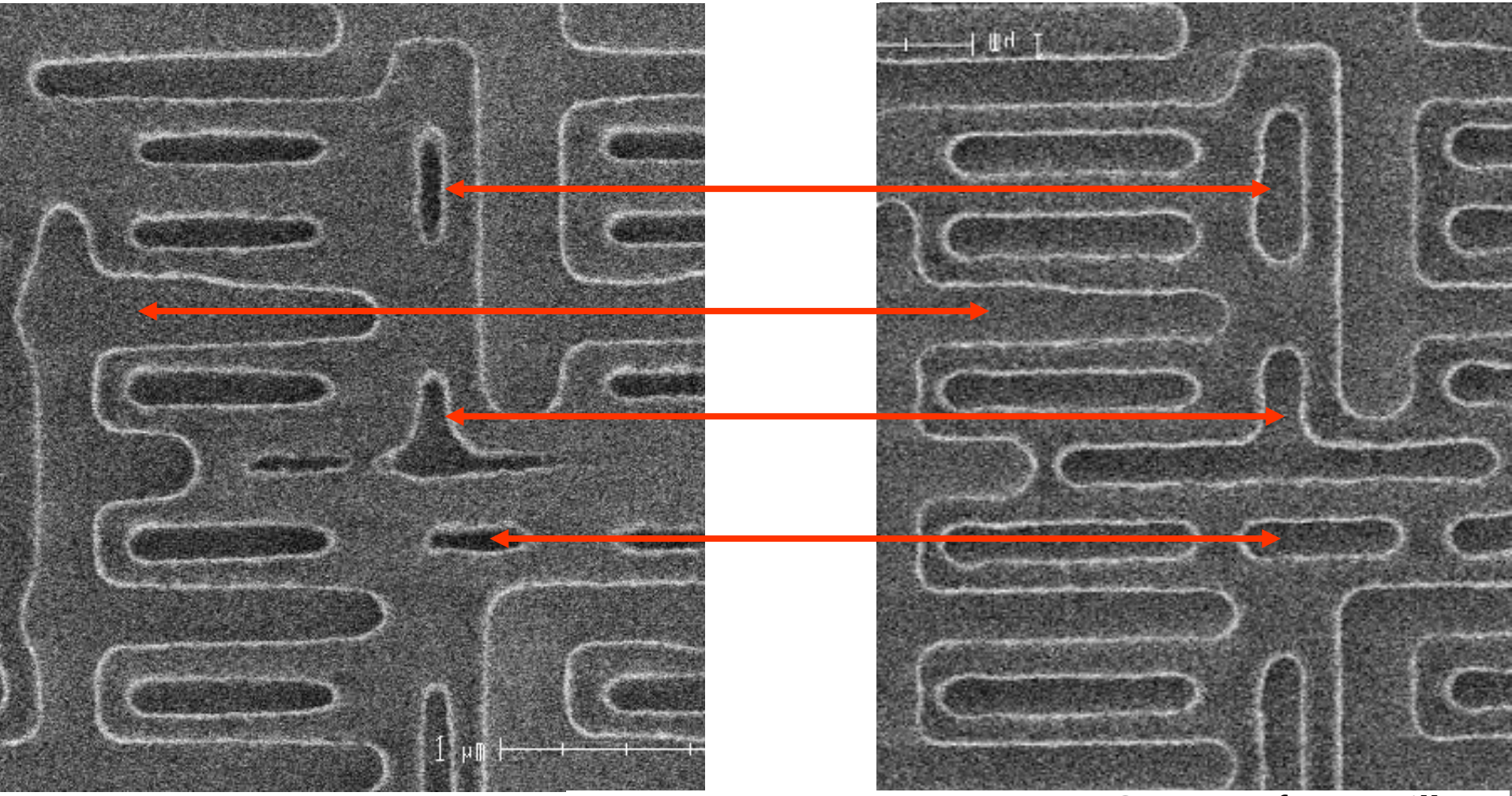
Optical Proximity Correction (OPC)

No OPC C065 Metal1 OPC



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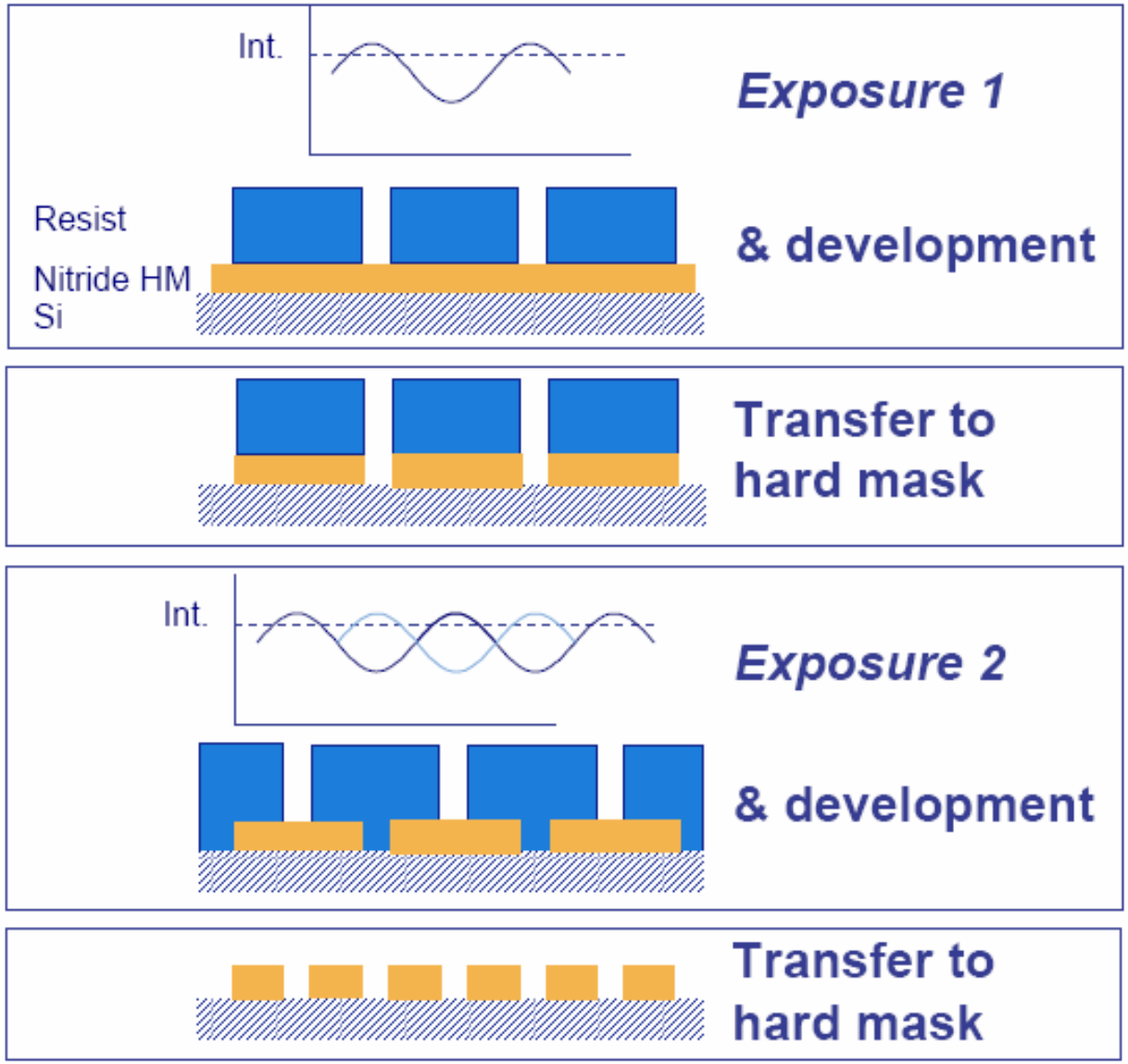
Double exposure/ Double patterning



Overlay bu
Process co
CoO (throu

ASML

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K1 factor decrease

- K1 factor was 0.6-0.7 in production environment
- Today most aggressive k1 in production is 0.3
  - Physical limit for single exposure is 0.25
- Using DE/DP k1 could be pushed down to 0.22

➔This will allow to print features less than ¼ of the exposure wavelength

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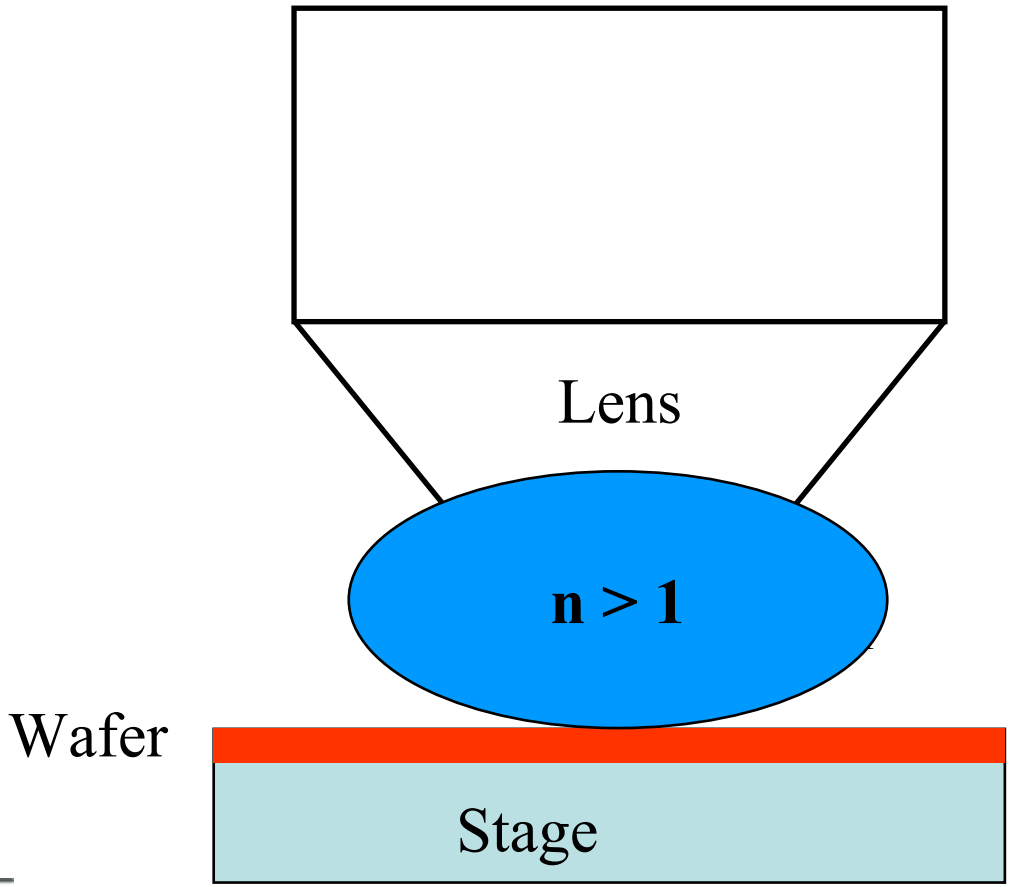
Numerical Aperture increase

- In air max achievable NA is 1
- Today state of the art dry system achieve NA =0.93

Introduction of immersion lithography allows to reach NA >1



$$NA = n \sin \theta$$

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Immersion lithography

- Today with water (n =1.44) NA=1.2~1.3 are achievable

  ➔ Still some defect issues to be resolved

- High index fluid are under development
  - n= 1.6 could allow NA =1.35~1.5
  - n=1.8~2 could allow NA=1.6~1.8

  ➔ Big challenge to develop high index fluid which are stable and with low absorption

  ➔ Going to n> 1.5 will request new lens material and new resist

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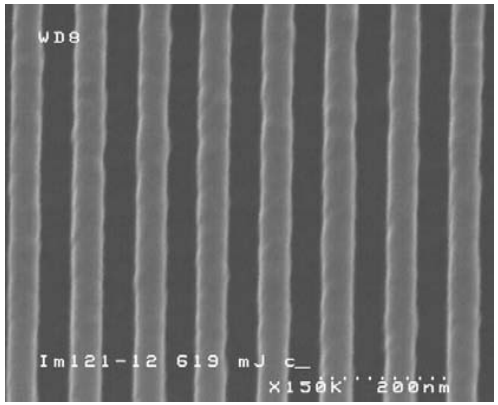
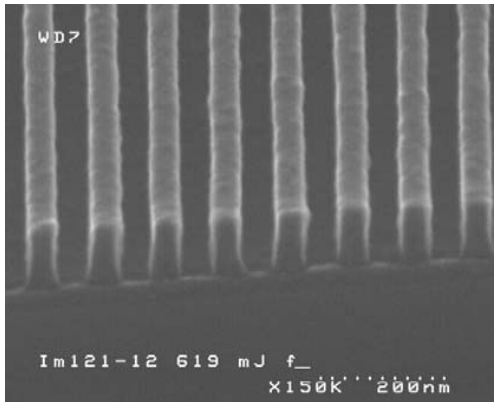
Immersion lithography with water

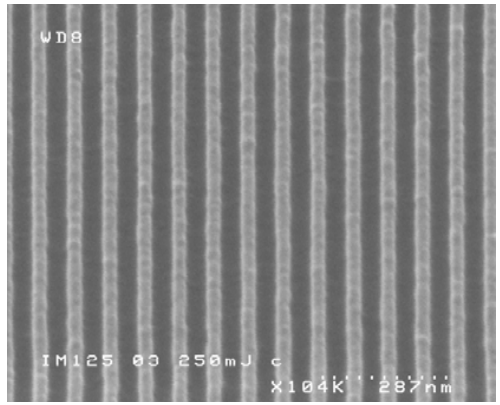
55 nm hp imaging NA=0.87

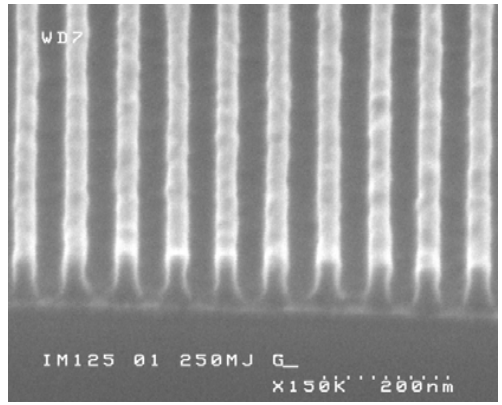




CD = 47 nm

40 nm hp imaging NA=1.2





CD = 39 nm

Obtained by interferometer lithography

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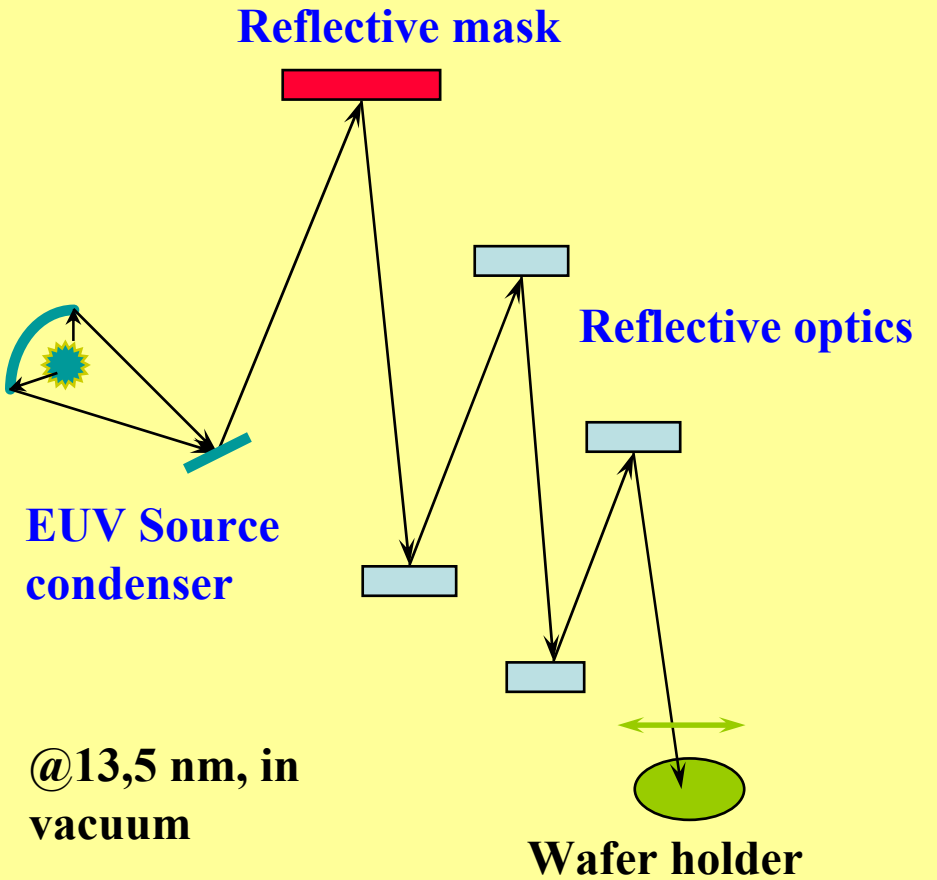
EUV Lithograpy: technological breakthrough

The big jump from DUV 193 nm to EUV 13.5 nm



Everything absorb EUV light

- ✓Vacuum
- ✓Reflective masks and optics

Sources: based on plasma (Xe,Sn,In) emitting in EUV (13.5 nm)

- ✓Laser Produce Plasma (LPP)
- ✓Discharge Produce Plasma (DPP)

Specifications very tight

- ✓ML mirrors: 70% reflectivity
- ✓Masks: defects < 10^{-3} defects/cm2
- ✓optics: < 0.1 nm roughness
- ✓sources: 180 W, no debris

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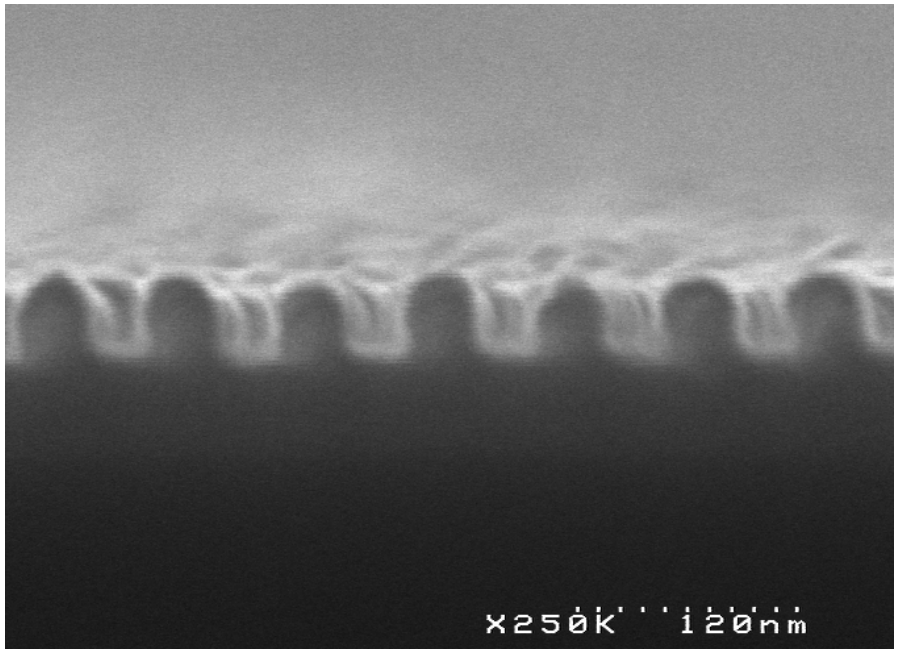
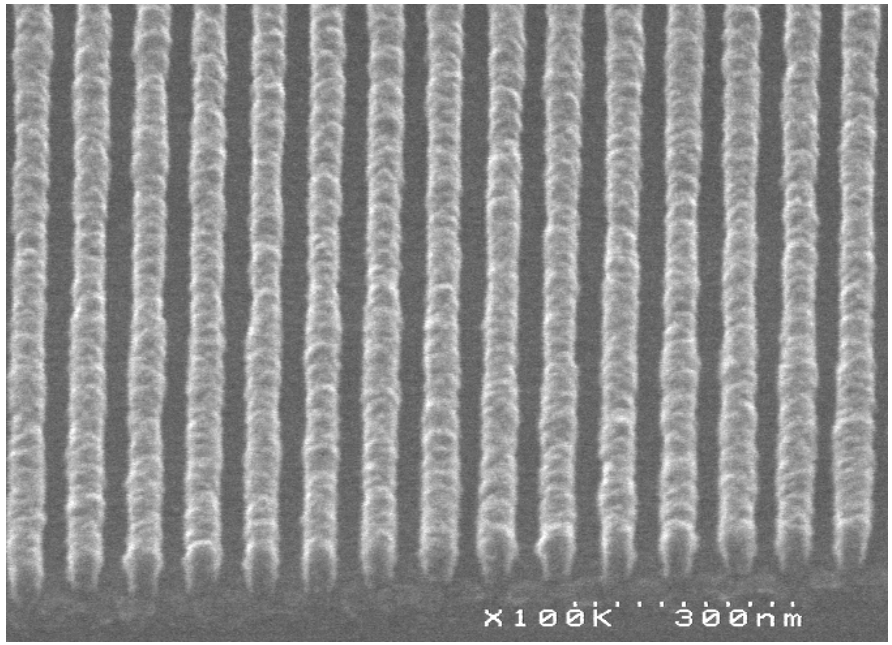
EUV lithography main achievements





32.5 nm L/S on CAR using IL-EUV at PSI

Today no CAR meet requirements for resolution, sensitivity and LER

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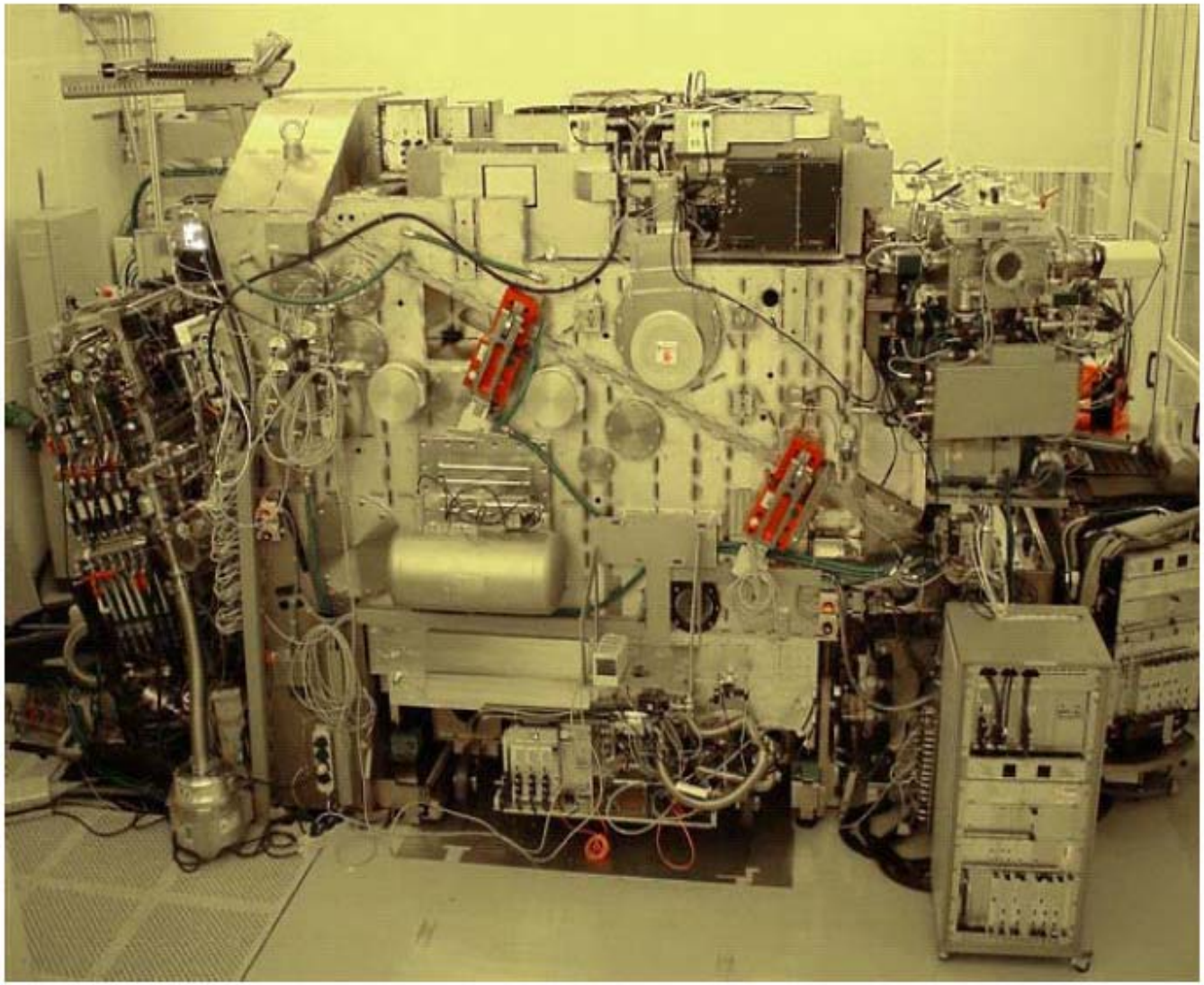
EUV lithography : ASML alpha tool



	AD-tool
λ	13.5 nm
NA range	0.15 – 0.25
Field size	26 x 33 mm²
Wafer size	300 mm
Magnification	4x
Flare	16%
Dense L/S	40 nm
Isolated lines	30 nm
Iso/dense contact	55 nm
Overlay	12-15 nm
Throughput	~6-10 wph

ASML

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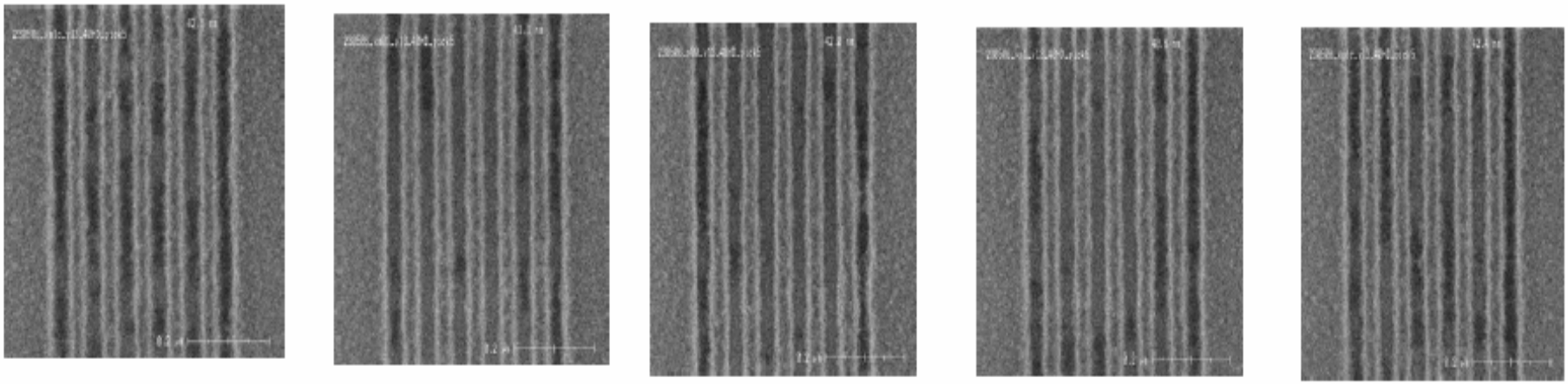
EUV lithography : ASML alpha tool

40nm scanning H-lines/spaces 'through slit' from AD-tool

(22-May-'06)



-10.6 mm | -6.36 mm | 0.0 mm | 6.36 mm | 10.6 mm

Resist: MET-2D, ~18 mJ/cm2
NA=0.25
σ= 0.5 (conventional illumination)

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EUV lithography main issues

Top issues

- Resist resolution, sensitivity and LER
- Collector lifetime
- Availability of defect free masks
- Source power

Remaining Critical Issues

- Reticle protection during storage, handling and use
- Projection and illuminator optics quality and lifetime

➔**Significant concern: Timing and cost**

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ASML technology roadmap scenarios

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Pitch relaxation or Double patterning

Low k_1 challenge

Fluid/ material challenge

Infrastructure challenge

likely

opportunity

ASML

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CoO issues

➔ **Resolution improvements are made to the detriment of severe cost increase for masks and tools.**

➔ **To overcome these economical issues introduction in the lithography roadmap of:**

- Maskless solutions foreseen with charged particles (E-beam) or optical (193 nm or EUV wavelength)
- Nanoimprint technology

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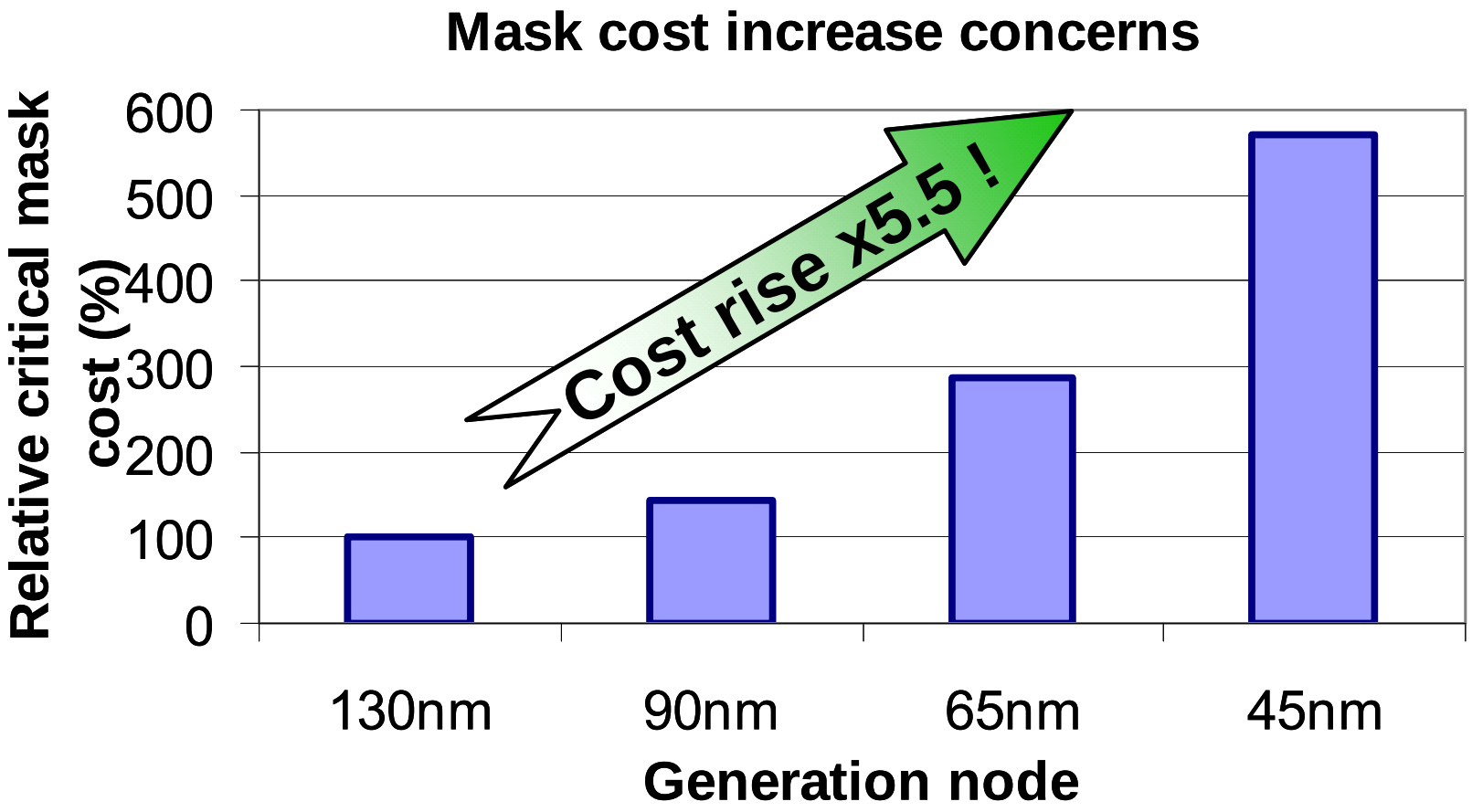
Mask cost



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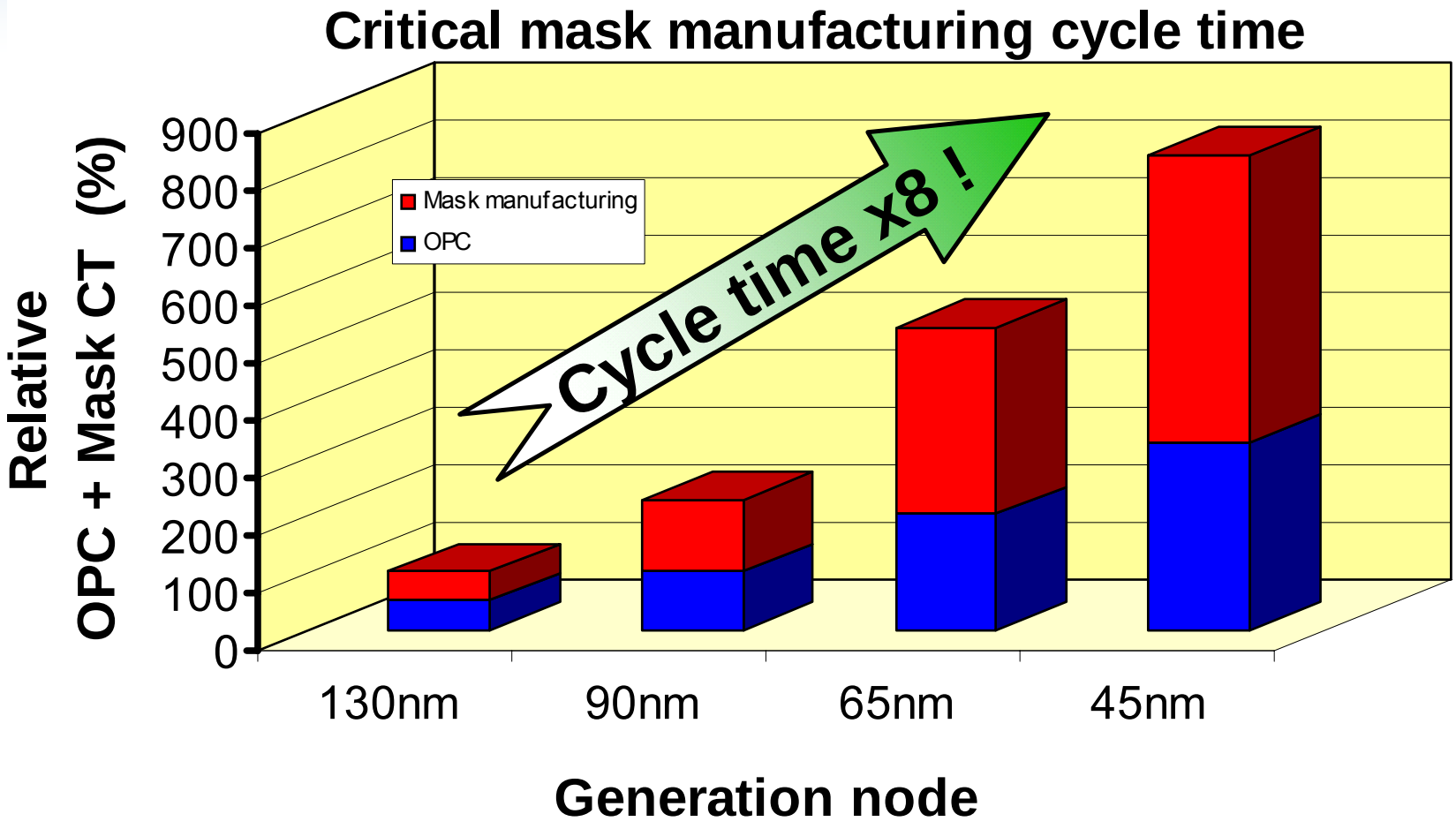
Mask cycle time



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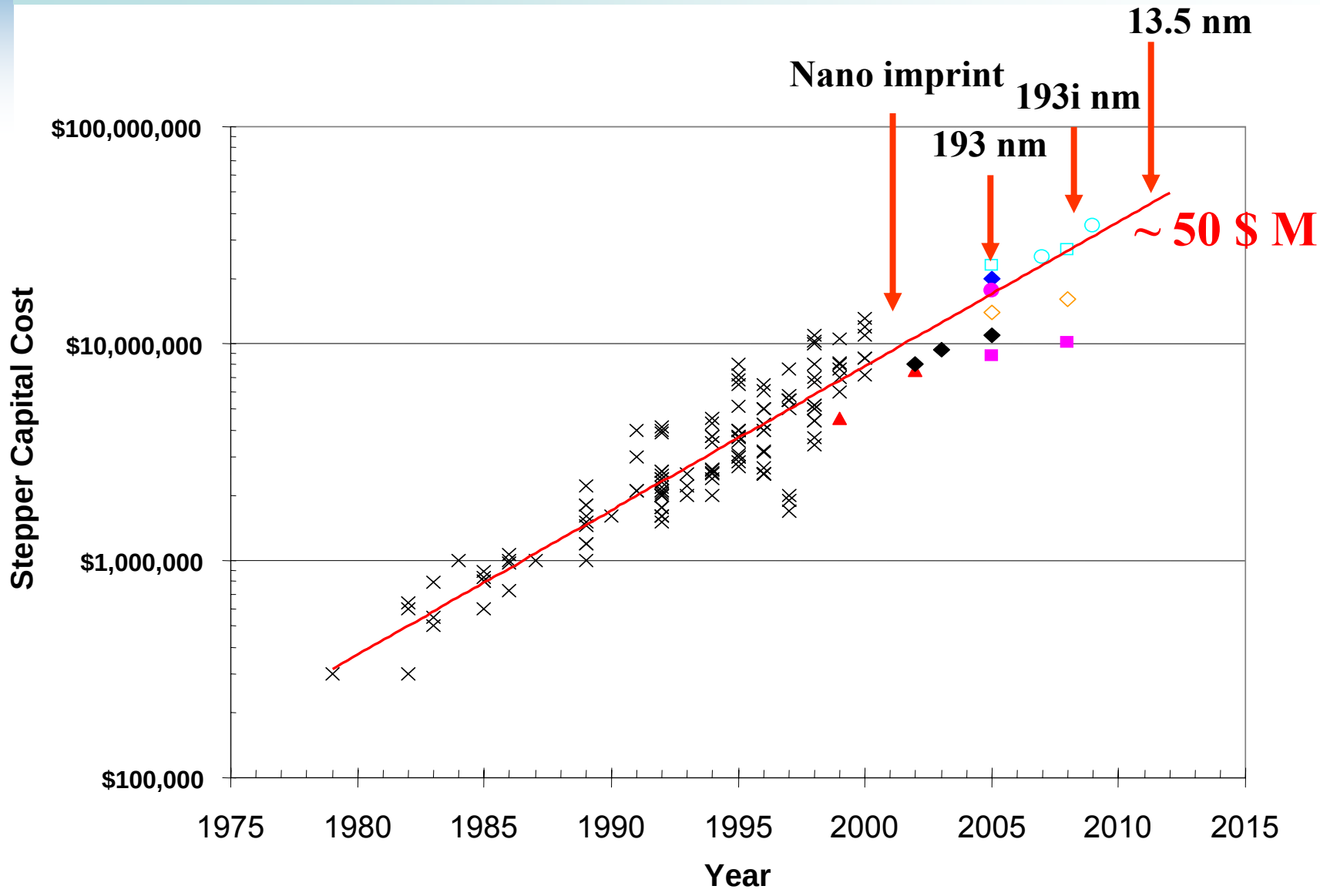
Equipment cost



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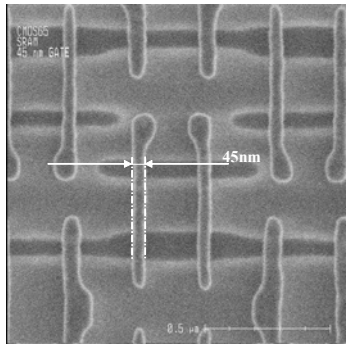
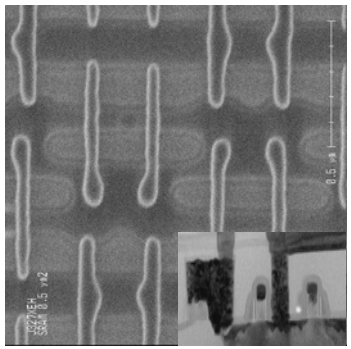
Crolles 2 Alliance EBDW Litho

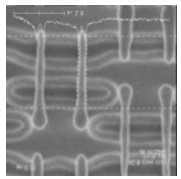
CMOS 65 | CMOS 45 | CMOS32

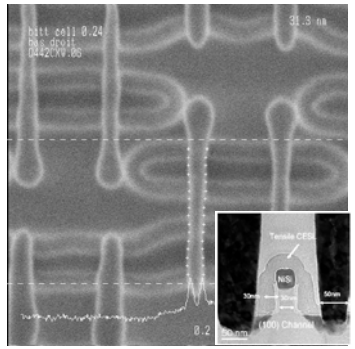
Q4/2002 | Q4/2003 | Q4/2004 | Q4/2005 1st studies



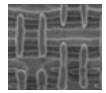


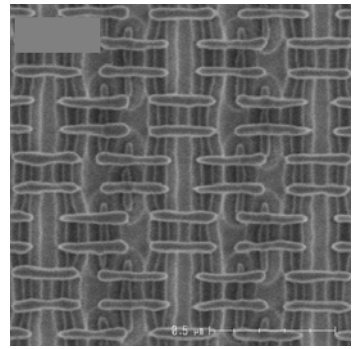
Scale reduction vs 0.5µm² SRAM cell





Scale reduction vs 0.5µm² SRAM cell





0.69µm² - 65nm | **0.5µm² - 65nm** | **0.248µm² - 45nm** | **32nm**

Courtesy of Laurent Pain

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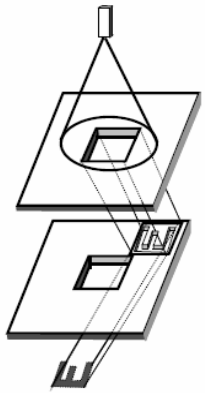
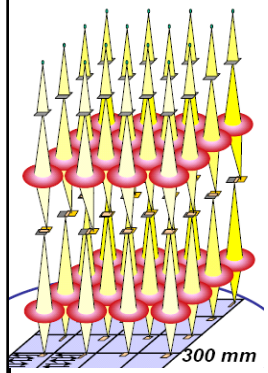
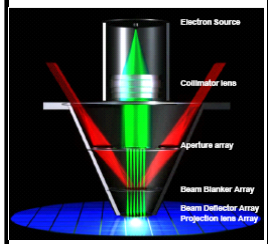
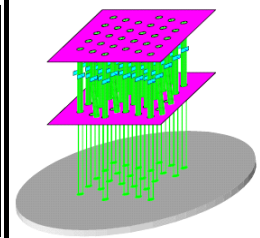
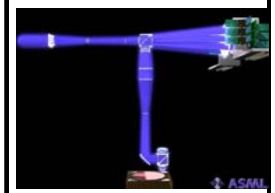
ML2 tools development

company name	EBEAM corp	ADVANTEST	MAPPER	VISTEC	ASML
principle	VSB+CP 400 characters	multi columns with shape beam & CP concept 100 characters	multi-beam	multi-beam	multi array
source	electron	electron	electron	electron	photon
Acc voltage	5kV	50kV	5kV	100kV	NA
demagnification number				400	400
beam number	1	16 columns	13000	10000	100Mpixel 26x32mm
spot size	VSB spot	VSB spot	35nm	25nm	40nm
throughput (wph)	1-5	1-10	10-30	5	5
technology node insertion	65hp	65hp	45 hp	45hp	65hp
					

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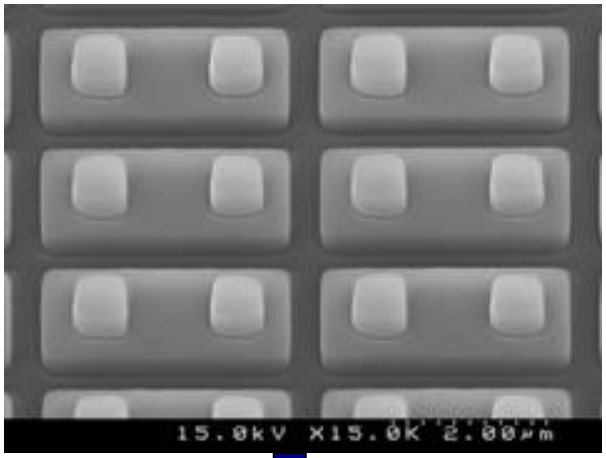
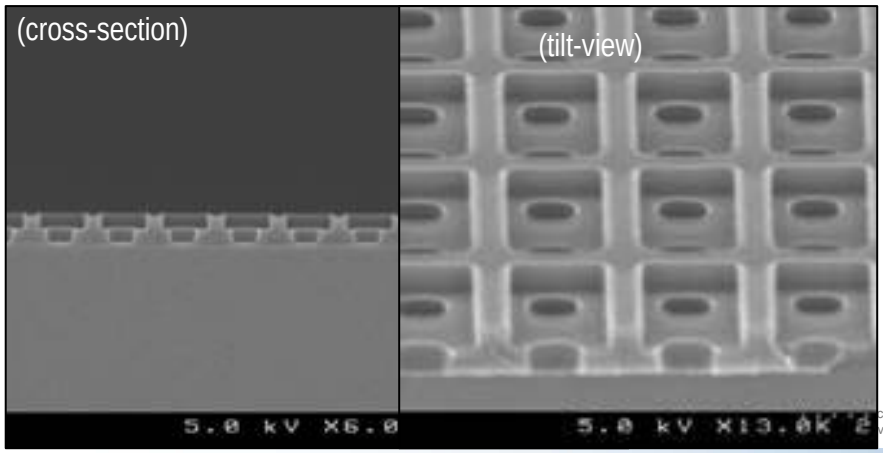
Nanoimprint as a NGL: Why?

3 Dimensional printing

Via chain structure (Via / Metal2)

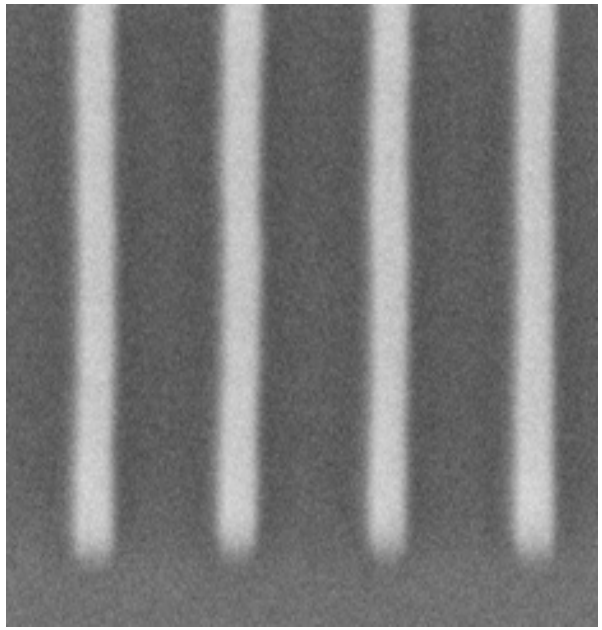


Imprint into dielectric



Courtesy of Univ. of Texas and DPI

Low LER



20nm Replication

Courtesy of MII

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Template requirements for IC manufacturing

Template :	*Specifications (32 nm node) :*
Magnification	**1X**
Mask nominal image size	**18 nm**
Image placement	**1 nm**
Linearity	**3.2 nm**
Defect impacting CD	**3 nm**
Trench width roughness	**1.4 nm**

The full infrastructure need to be put in place timely

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1X template fabrication key issues

➔ Compare to 4X requirements 1X roadmap need to fill significant technical gaps:

- E-beam lithography tools are needed with1X resolution, Image placement and the necessary throughput
- CAR resists needed with Low diffusion allowing 32 nm dense and 18 nm isolated lines with necessary CD control
- Etching process needed with 1X specifications for linearity, profile and depth control
- E-beam metrology and inspection on insulator
- Handling/storage: maintaining defect free template what will be the pellicle?

➔ 1X mask technology could have difficulties to be accepted by the IC industry

➔ Remember: 1X mask have been one of the showstopper for X-Ray lithography!

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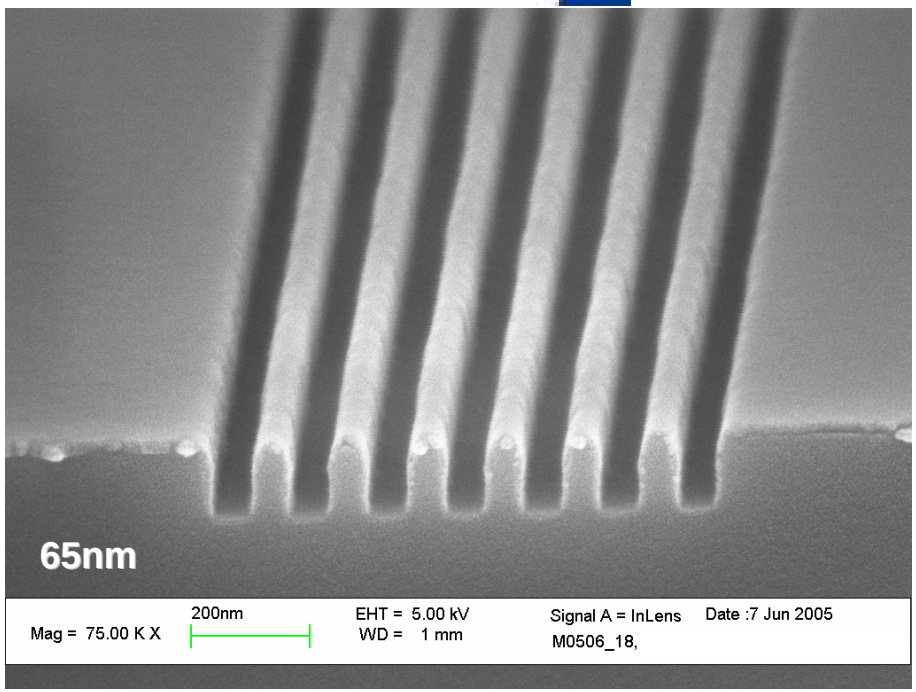
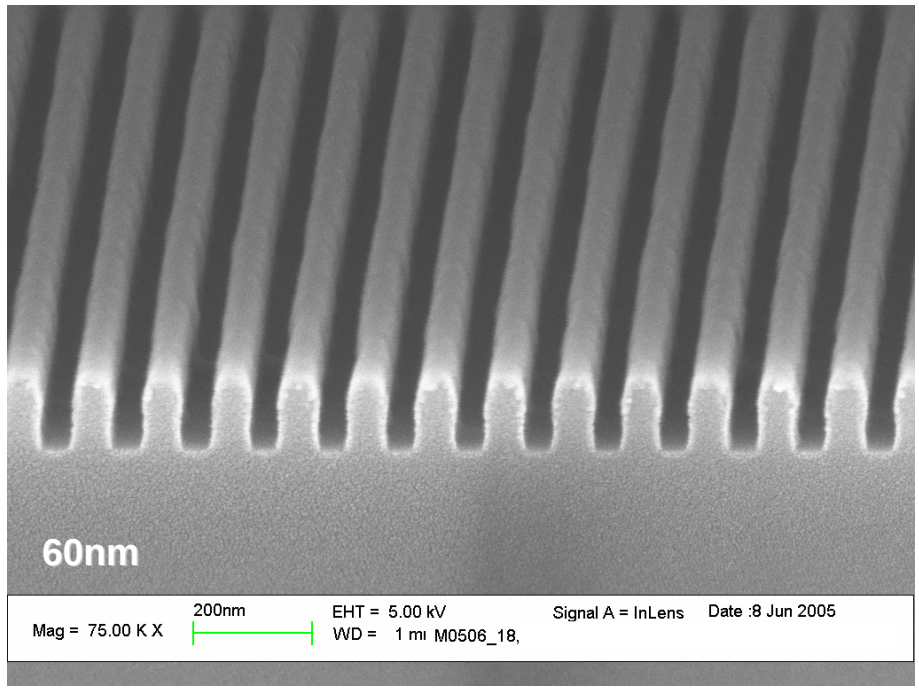
1X template fabrication: state of the art





65 and 60nm L/S structures etched in quartz

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Tool requirements for IC manufacturing

Tool/process :	*Specifications (32 nm node):*
Wafer min half pitch	**32 nm**
Wafer min line in resist	**18 nm**
Wafer min contact hole	**30 nm**
Overlay accuracy	**6 nm**
CD uniformity (3σ)	**3 nm**
Throughput (300 mm)	**50 wph**

But also:

- Magnification/Distortion corrections
- Mix and Match capability
- Defectivity control

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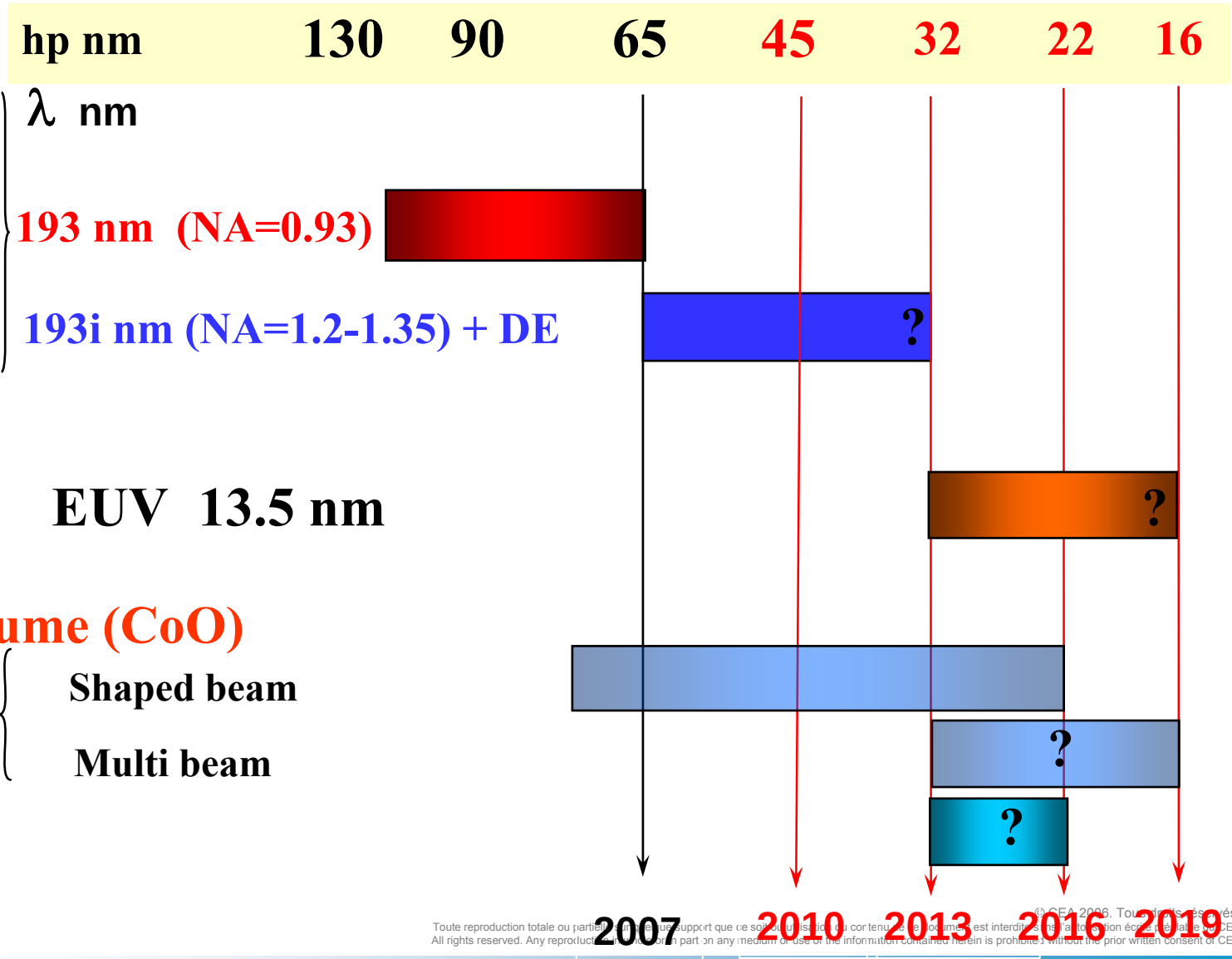
lithography roadmap (2006)



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Conclusion

- 193 i with DE/DP will be pushed down to the 32 nm hp
- Today there is no alternative to EUVL for the 22 nm hp
- Actual CAR doesn't met requirements (LER, resolution and sensitivity) :
  - ➔ **new resist platforms needed for 22 nm hp?**
- For low volume production a cost effective lithography solution is urgently needed :
  - ➔ **ML2 and nanoimprint could be an alternative**
- Can optical lithography be pushed down to the 10 nm range ?
  - ➔ **surface plasmon or evanescent wave could open a multitude of new possibilities for sub-wavelength lithography.**

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Conclusion

Be aware the “optical for ever” lobby will never give up!!

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