## The Impact Of Step And Flash<sup>tm</sup> Imprint Lithography For Nano-Manufacturing In Emerging Market Applications

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Step and Flash Imprint Lithography  $(S-FIL^{TM})$  process is a nano-replication technique based on UV curable, low viscosity liquids. Investigation by this group and others has shown that the resolution of replication by imprint lithography is limited only be the size of the structures that can be created on the template (mold). A typical S-FIL process uses field-to-field drop dispensing of the UV curable liquids for step and repeat patterning. Similarly, a non-step and repeat variation of S-FIL is possible, where a thin whole-wafer template replicates patterns in a single imprint step, enabling patterning over non-flat surfaces. These approaches allow for nano-manufacturing of devices with widely varying pattern densities and complicated structures.

There are numerous market applications for imprint lithography including advanced CMOS patterning, fine pitch gratings for the manufacture of wire grid polarizers, photonic crystal and quasi crystal patterns for LED light extraction and the fabrication of 3D structures such as micro-lenses to channel light into image sensors or aid in the extraction of light from LEDs. These applications and the underlying process requirements will be described. Images will be shown of distortion free sub-100 nm contacts and gratings that are replicated by S-FIL processing. Imprinted micro-lens device structures will also be shown.

To-date, the imprint lithography systems manufactured by Molecular Imprints have demonstrated:

- Full wafer coverage with lithographically useful patterning by S-FIL and whole-wafer imprinting.
- Full wafer residual thickness control to enable practical etching (thickness variation < 10 nm, 3 sigma.
- Field-to-field CD uniformity measured on an analytical SEM < 2 nm, 3 sigma with no process adjustments.
- Etch pattern transfer including break-through etch of residual material, followed by a bilayer etch through thick planarization layers.
- Process life showing no degradation of sub-100 nm dense features for over a thousand imprints without requiring change of template or template surface treatment.
- Overlay results down to < 50 nm 3 sigma on CMOS substrates.

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