Nanoimprint Lithography Fabrication Of Photonic Crystal Devices

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We present a nanoimprint lithography (NIL) process for fabrication of topology optimized photonic crystal (PhC) devices [1] (and other nanoscale applications) in silicon. High resolution and high aspect ratio of the transferred pattern is obtained by exploiting a high-resolution negative electron beam resist for silicon stamp fabrication in combination with NIL in a thermoplastic resist with high etching resistance. The optical performance of the PhC devices is highly sensitive to the nanometer features of the components. The pattern transfer quality is assessed by benchmarking the optical performance of NIL fabricated PhC devices against nominally identical devices, defined by direct electron beam writing.

Silicon stamps were fabricated by utilizing 100 kV electron beam lithography (EBL) (JEOL JBX9300FS) in a 50 nm thick film of TEBN-1 [2] negative resist on a silicon substrate. The exposure dose was 9 mC/cm^2. The written structures were developed in methyl isobutyl ketone (MIBK) for 20 s, rinsed in isopropyl alcohol (IPA) and subsequently transferred 100 nm into the silicon substrate by a highly anisotropic reactive ion etch [3]. After etching the silicon, any remaining resist was removed in a oxygen plasma prior to deposition of an anti sticking layer from a C4F8 plasma and imprinting.

An 80 nm thick film of mr-I T85 (4 wt%) imprint polymer was spincoated onto a silicon-on-insulator (SOI) substrate at a spin-speed of 3000 rpm and baked at 150°C for 5 min on a hot plate. The stamp was imprinted using a parallel plate imprint tool (EVG 520HE) under vacuum (0.01 mbar). The optimum imprint parameters for replication of the PhC structures were found to be: temperature 140°C, time 10 min, and pressure 13 bar. The stamp and substrate were separated at a temperature of 60°C. The imprint parameters resulted in a *complete* filling situation of the stamp in the PhC structured areas and yielded 100 nm deep holes in the mr-I T85 resist. The nanoimprinted patterns were transferred into the top 320 nm thick silicon layer of a SOI substrate by using an optimized SF6-based inductively coupled plasma (ICP) etch. The etch selectivity of silicon over mr-I T85 is 9:1 (silicon:mr-I T85) [4], which allows for pattern transfer of the imprinted holes through the device silicon layer of the SOI substrate.

The lithographic result of our imprint process is compared to devices fabricated by direct electron beam writing of the etch mask. For direct writing, the positive resist ZEP520a was exposed at 100 kV, using the same EBL tool as used for stamp fabrication. The ZEP520a resist has a selectivity of ~5 compared to silicon in the ICP etch, hence, a layer of 100-150 nm is necessary to transfer the pattern into the silicon layer. The results are shown in Figure 1, where scanning electron microscope (SEM) pictures of 2D photonic crystal waveguides (PhCWs) fabricated by EBL (left) and with NIL (right) are compared. In the lower panel of the figure, we show the corresponding measured transmission spectra for TE-polarized light. The steepness of the cut-off at longer wavelengths caused by the photonic bandgap effect is comparable, and signal suppression above the cut-off wavelength is comparable within the device-to-device variation in a fabrication batch.

LITHO2006 26 -30 June, 2006 Marseille, France

References:

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Figures:

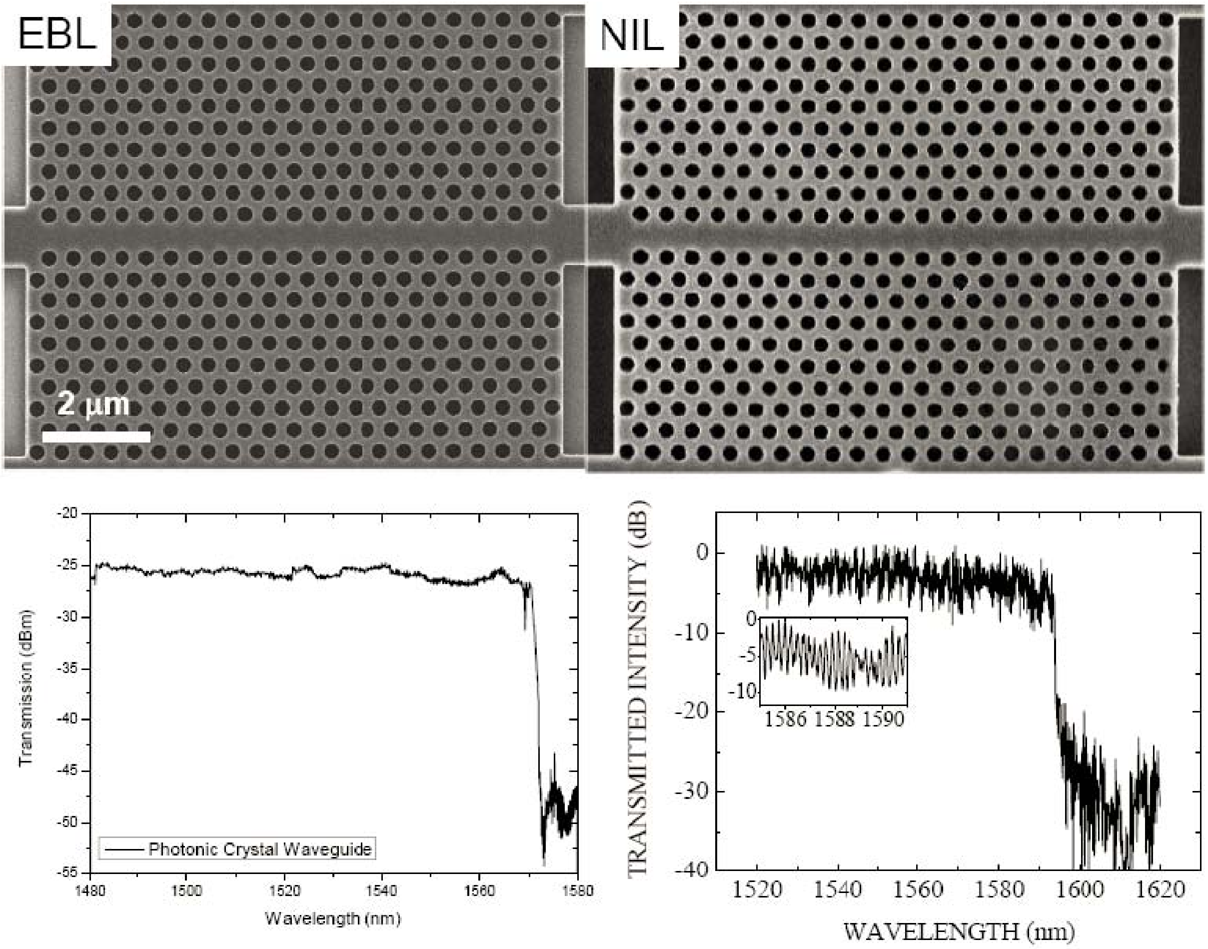

Fig. 1. Top panel: SEM pictures of a 10 µm long PhCW fabricated by (left) EBL and (right) NIL . Bottom panel: comparison of the corresponding measured transmission spectra for TE-polarized light.