

Continued Scaling In Integrated Circuits - Trends And Requirements In Lithography

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Over the past two years, 193nm immersion lithography has clearly emerged on the company roadmaps as the primary technology for the 65nm and 45nm half-pitch nodes. For the 32nm half-pitch node EUV is the primary candidate today. On the other hand, >1.6 NA 193nm immersion lithography using a single exposure and 193nm dry or immersion with double exposure are still considered as alternative candidates for this technology generation.ⁱ

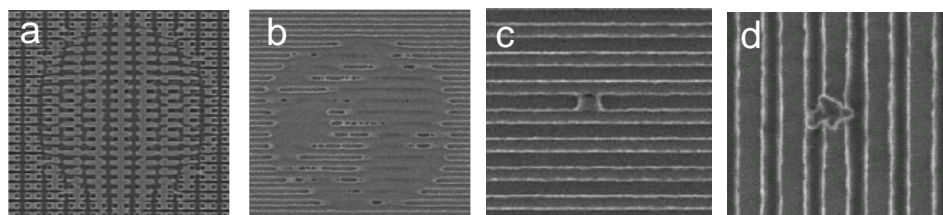


Figure 1 Defect types that were originally encountered in immersion lithography: micro-bubbles (a), water marks (b), micro-bridging (c) and particles (d)

IMEC, in collaboration with our partners – leading-edge chipmakers, equipment and material suppliers – has an active program on 193nm immersion lithography from the very beginning and is now starting a new program on EUV lithography. In this presentation, the progress, challenges and outlook of immersion lithography will be reviewed. A lot of the work at IMEC has focused on reducing the number of defects that were originally seen in immersion lithography (Figure 1). Great progress has been made over the past two years, resulting in complete removal of some defect classes (such as micro-bubbles) and significant reduction of the others (Figure 2).

Immersion - Daily Patterned Wafer Defect Monitor

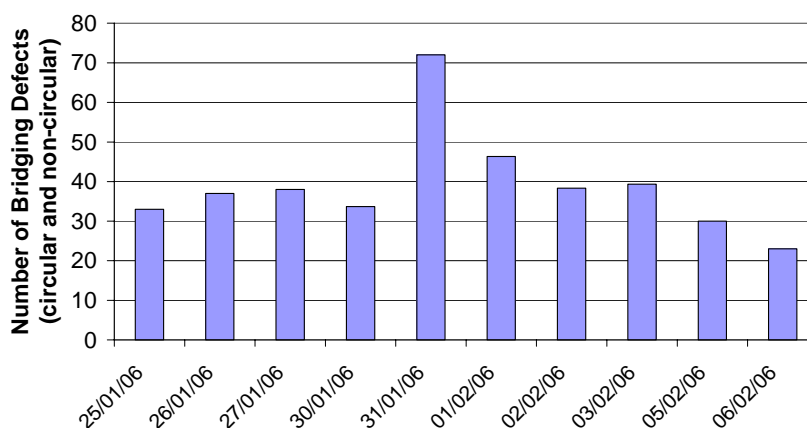


Figure 2 Monitoring data of the number of bridging defects per wafer using PAR-IM850 without topcoat on the XT:1250Di, 10x10mm field size. The data gives a proof of concept that a stable and low defect level can be maintained in immersion lithography.

Double patterning enables patterns to be printed at k_1 factors <0.25 (Figure 3). In this way 193nm lithography can be extended to the 32nm half pitch node. The most important concern for this technology is in the almost doubled cost per layer. Additionally, the overlay requirements for this technique are much more stringent.

KEYNOTES

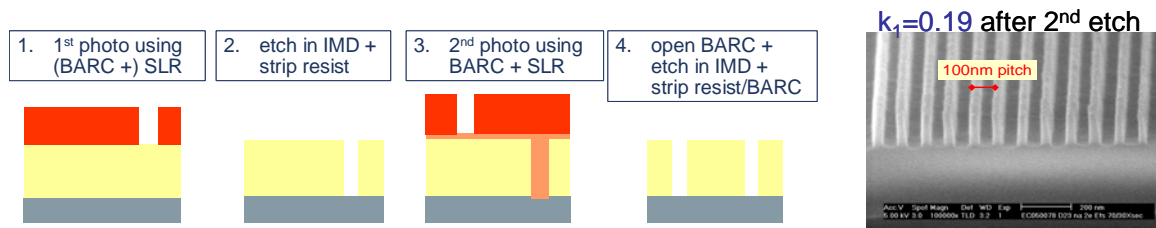


Figure 3 Double patterning scheme used to print 100nm pitch trenches at NA=0.75 ($k_1=0.19$)

In this presentation, also, a close look will be taken at where EUV can be expected to come in and what the issues are. Owing to its very short imaging wavelength (13.5nm) EUV has great potential for extendibility to the 32nm and 22nm half pitch node (Figure 4). However, some technical challenges remain, especially in the areas of EUV resists, collector lifetime and defect free masks.

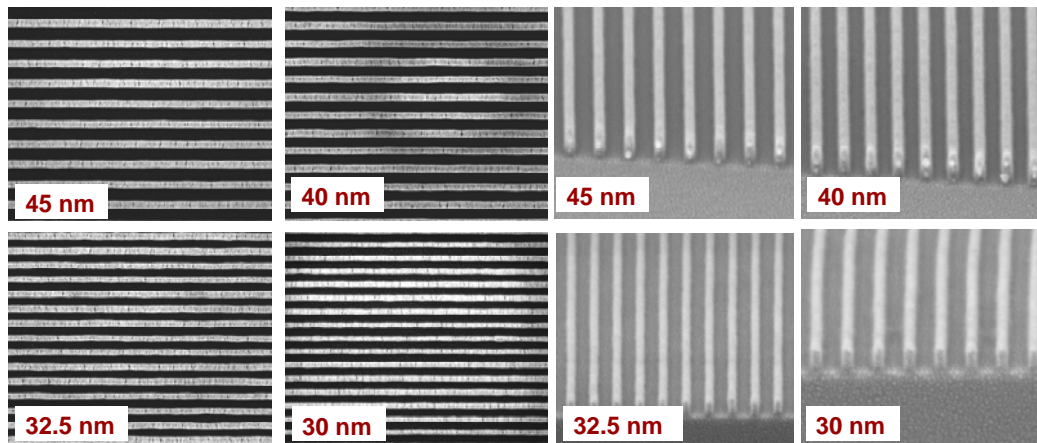


Figure 4 Top-down and cross-sectional images of lines/spaces patterned in PMMA using EUV interference lithography (in collaboration with Paul Scherrer Institut, Switzerland)