Statistical study of graphene field effect transistors (GFETs) performance

Sana Mzali[1], Alberto Montanaro[1], Odile Bezencenet[1], Jean-Paul Mazellier[1], Bruno Dlubak, Marie-Blandine Martin, Pierre Seneor, Pierre Legagneux[1]

[1]Thales Research & Technology, 1 Avenue Augustin Fresnel, 91767 Palaiseau, France
sana.mzali@polytechnique.edu

Abstract

Graphene has gained increasing attention over the last decade, due to its outstanding properties closely linked to its 2D material nature [1]. In particular, the potential of graphene for optoelectronic applications is currently being extensively explored because of its ultra-high carrier mobility and absorption from the far infrared to the ultraviolet [2,3]. However, to construct high-quality optoelectronic devices, it is necessary to accurately control graphene doping and to operate highly stable devices.

For that purpose, a statistical study was performed on more than 500 unsorted graphene field effect transistors (GFETs). The graphene films were grown on copper by chemical vapor deposition (CVD) and transferred on 300 nm SiO_2/Si substrates. The fabrication process includes, as a first step, the deposition of a protection layer (thin oxidized aluminum layer) after graphene transfer. Then, after device fabrication, we have deposited metal oxides layers, namely passivation layers, by atomic layer deposition, to passivate our CVD graphene based transistors.
We have statistically demonstrated the impact of each layer on our GFETs performance by comparing 3 different fabrication processes: without any protection/passivation layers, with only the protection layer and with both protection/passivation layers (Fig. 1). While we do not observe any conductance minimum with unprotected and unpassivated devices, 75% of the protected/passivated GFETs and 58% of only protected devices exhibit a conductance minimum for a gate voltage (V_{min}) below 50 V (Fig. 2).
Even more remarkable, we found out that 40% of protected and passivated devices exhibit a Vmin below 10 V. However, only 3% of protected devices display a conductance minimum in this small window. We also achieved successful hysteresis free DC characteristics on about one-quarter of our protected/passivated GFETs.

The analysis of all these statistical results highlights the importance of the use of both protection and passivation layers to fabricate low-doped graphene devices with minimum hysteresis and long-term stability.
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References

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Figures

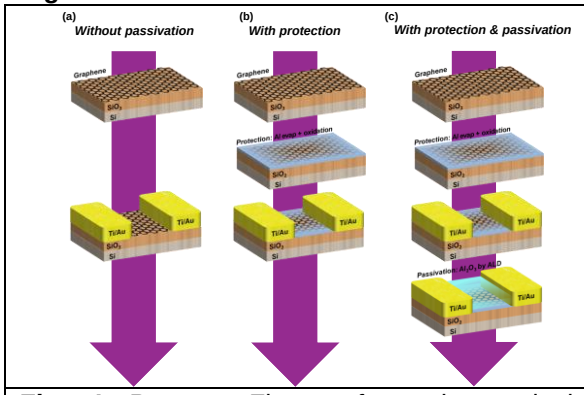

Fig. 1 Process Flows of graphene devices fabrication on 300 nm SiO_2/Si substrates without any protection/passivation layers (a), with protection process (b) and with protection/passivation process (c).

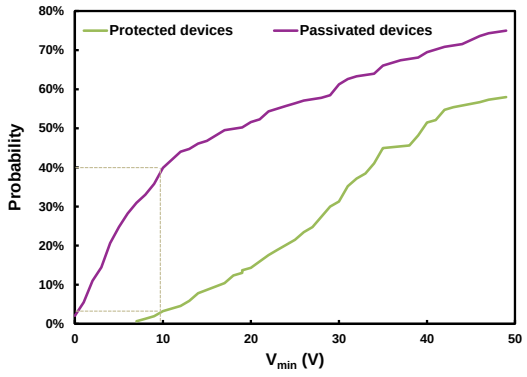

Fig. 2 Cumulative distribution curves of working GFETs with protection layer (green curve) and with protection/passivation layers (purple curve) as a function of V_{min} (gate voltage at minimum conductance).