Selective Nano- Structured Material Growth in Nanoelectronic Device

H. L. Chang[1, 2] and C. T. Chang[2]
Department of Material Science and Engineering of National Chiao Tung University
Research and Technology Development Department, 2PJT, Samsung Electronics South Korea

Abstract

Catalytic-assisted CNTs are integrated into trenches and holes under CH_4/H_2 gases by microwave plasma chemical vapor deposition, the trench and hole are used to fabricate for gate electrodes and interconnections, respectively. Results indicate the orientation of grown CNTs is dominated by pattern geometry. The growth models of Fe and $CoSi_2$ and application for nanoelectronics are purposed.

The integration of CNTs into Si-based metal-oxide-semiconductor field effect transistor (MOSFET) or new nanoelectronicos remains a challenge in the fields of transistors and interconnections. CNTs are accepted as candidates for use in molecular electronics to overcome the physical limitation of current Si transistors and Cu interconnections [1-2]. The feasibility of realizing this vision depends on direct approaches to selective depositions in the trenches or holes of Si wafers. Bundles of CNTs in the trenches and holes can provide sufficient current density in the form of channels and conductors, respectively. This work systematically elucidates the synthesis of CNTs by microwave plasma CVD (MPCVD). In this investigation, Fe catalyst and $CoSi_2$ film employed frequently as gate electrodes and a contact material in Si microelectronics are applied. The selective growth of CNTs in trench/hole approaches is also examined. The morphology and nanostructures of CNTs are characterized. The field emission characteristics of CNTs deposited in the trenches and holes are investigated to determine electronic performance. CNTs were synthesized on patterned Si wafers with trench arrays and holes by MPCVD system with CH_4+H_2 source gases. Two catalytic films were prepared on patterned Si wafers before CNTs synthesis: (1) an Fe film (20 Å) and (2) a Co film (75 Å). Then two-step rapid thermal annealing (RTP) was conducted at 600 ℃ for 60s and at 760 ℃for 20s, under N_2 ambient. Si wafer with patterned $CoSi_2$ holes with a $CoSi_2$ catalyst film was formed by rapid thermal processing (RTP) and the self-alignment process. Figure 1 presents the AES depth profiles Co film on Si substrate with rapid thermal annealing (RTP) indicating the chemical composition of $CoSi_2$.The oxide film was prepared by plasma-enhanced chemical deposition (PECVD), and plasma dry etching and a wet stripping were adopted to remove the un-reacted metal film. The schematic diagrams of CNTs formation on trench and hole are shown in Fig. 2.

References

[1] G. S. Duesberg, A. P. Graham, F. Kreupl, M. Liebau, R. Seidel, E. Unger, and W. Hoenlein, Dia. Relat. Mar. **13**, 354 (2004)

[2] B. Q. Wei, R. Vajtai, P. M . Ajayan, Appl. Phys. Lett. **79**, 1172 (2001).

Figures

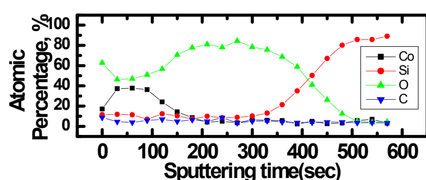

Fig. 1 AES depth profile Co film/Si substrate after RTP

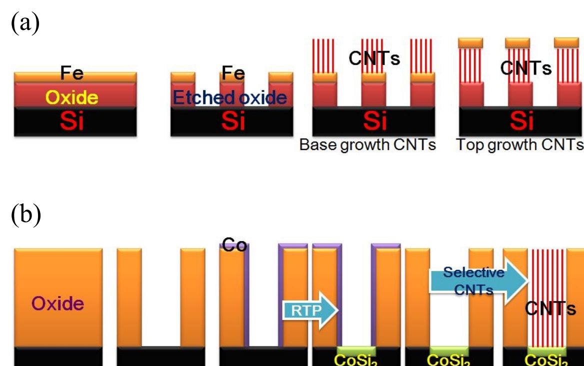

Fig. 2 Process flows of forming CNTs on (a) Fe trench arrays, oxide film deposition ->Fe film deposition ->drying etching ->CNTs growth (b) $CoSi_2$ holes, oxide film deposition ->drying etching ->Co film deposition ->RTP ($CoSi_2$ formation)-> unreacted metal removal -> CNTs growth