Study of SB-MOSFETs on SOI substrates

J.L. Padilla[1] and F. Gámiz[1]

[1]Departamento de Electrónica y Tecnología de los Computadores
Universidad de Granada, Facultad de Ciencias. Avda Fuentenueva s/n, Spain, EU
Email: jluispt@ugr.es, fgamiz@ugr.es

1. Abstract

This work constitutes a first approach to the study of SB-MOSFETs on SOI performing several simulations that take into account the different carrier transport mechanisms that may be found in these sort of devices. Some comparisons are made depending on the mechanism considered as well as for several Schottky barrier heights and different drain and gate bias.

2. Introduction

In SB-MOSFETs we replace conventional doped semiconductor regions by metallic materials that create rectifying metal-semiconductor junctions (*Schottky barriers*). These junctions having very similar electrical characteristics to doped *pn* junctions, present two most important scaling benefits: (*i*) Low source/drain resistivity (in usual MOSFETs as junctions depths are scaled to below 50nm, source and drain series resistances become increasingly significant), (*ii*) Abruptness of metal-semiconductor junctions allow very short physical channel lengths to be defined.

Schottky barriers are essentially unipolar current devices in which the carrier transport may be seen as formed by three different components: thermionic emission of carriers over the barrier, thermionic field emission of high energy carriers through the upper part of the barrier and field emission of carriers through the barrier at the Fermi level. Thus depending on the bias conditions at the junctions, one or more of these contributions will dominate carrier transport.

A first approximation to barrier height is given by [1] where

$$\phi_{bn} = \phi_m - \chi_s$$

$$\phi_{bp} = \frac{1}{q}E_g - (\phi_m - \chi_s)$$

In our case, we will deal with a p-channel SB-MOSFET as shown in Fig.2 therefore only holes transport will be considered. At high gate voltages, tunneling becomes determinant for current flow and consequently the higher the voltage, the narrower the barrier and field emission and thermionic field emission contributions appear. In Fig.1 it can be seen how for a gate bias of order of -3*V* the drain current can be nearly two orders of magnitude higher when we allow field emission mechanisms

3. Simulations

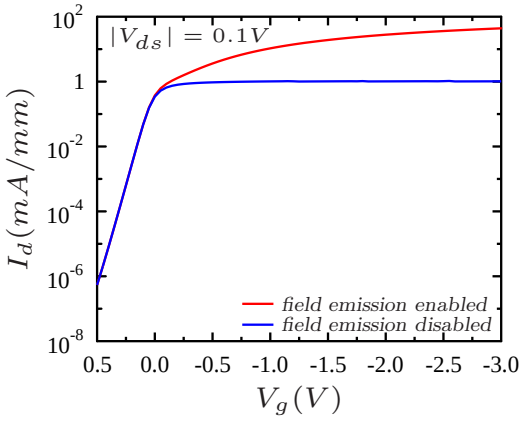

Fig.1: *Field emission enabled vs. field emission disabled for different gate bias with low drain bias.*

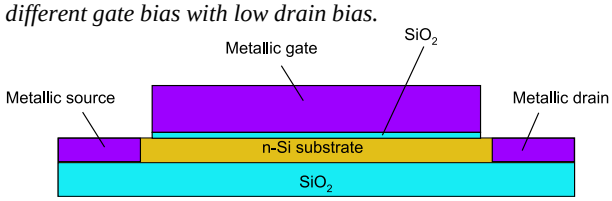

Fig.2: *p-channel SB-MOSFET with 10nm thick Si substrate. The channel length is 85nm.*

We performed our simulations using Silvaco ATLAS software [2]. Due to the abrupt variation in electrostatic potential between metal and semiconductor in Schottky contacts, the choice of an appropriate grid is essential and thus the mesh for the simulation must be carefully designed. We choose a quite fine grid at the source-to-channel and drain-to-channel interfaces to accurately calculate the current contribution caused by field emission at the expense of greater simulation time.

The voltages applied alter the shape and height of the barriers. Increasing gate bias gives rise to higher electric fields and height of barriers is reduced due to image force lowering and dipole lowering. These two effects can be estimated using the expressions described in [3]

$$\Delta\phi_{b,ifl} = \sqrt{\frac{qE_{applied}}{4\pi\varepsilon_s}}$$

$$\Delta\phi_{b,dl} = \alpha E_m$$

However, the Silvaco ATLAS simulator does not

account for barrier lowering mechanisms applied to field emission but only to thermionic emission. Therefore the barrier heights used in our simulations must be regarded as zero-bias values. This approximation has negligible impact for low gate and drain biases but obviously will not accurately represent the physical processes at work for high voltages. Nevertheless, as a first approach to the behaviour of these devices, we could use these simulations and compare them to experimental data for low drain and gate bias in order to guess the most likely zero-bias barrier height.

Drain current results for a low drain bias and different zero-bias barrier heights can be seen in Fig.3. Large differences up to nearly a decade in drain current are evident at V_{gs}=-3V between the cases of 0.10 and 0.35 eV. This emphasizes the significant impact that barrier height variations have on the ON state of a SB-MOSFET.

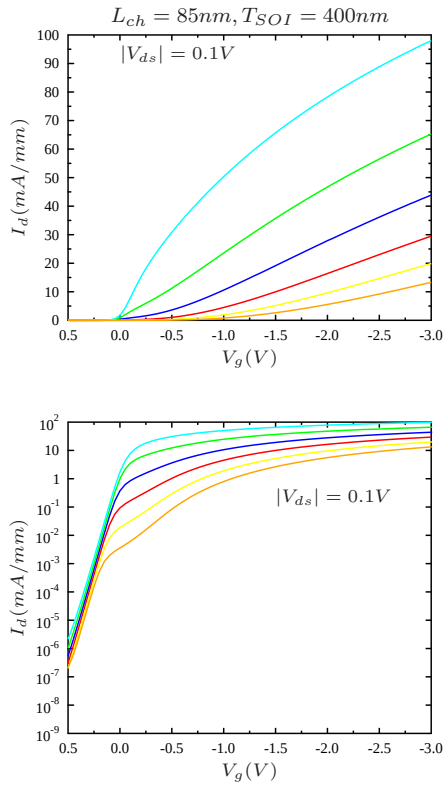

Fig.3: *Simulated drain currents for V_{ds}=0.1V for Schottky barrier heights from 0.10 eV (cyan line) to 0.35 eV (orange line).*

Conversely, we can infer very small impact of barrier height on the subthreshold current. Therefore, if one considered these different zero-bias barrier heights (from 0.35 eV to 0.10 eV) as the result of a gradual barrier lowering process these results would be in agreement with the fact that barrier lowering has little effect for low gate and drain bias.

The corresponding high drain voltage transfer characteristics are shown in Fig.4 in linear and logarithmic scales. In this case, as we are considering high drain bias, appreciable differences can be observed even on the subthreshold current. This again indicates that if the different barrier heights of the simulations were the effect of any barrier lowering mechanism, this mechanism becomes prominent under high drain and gate bias as expected.

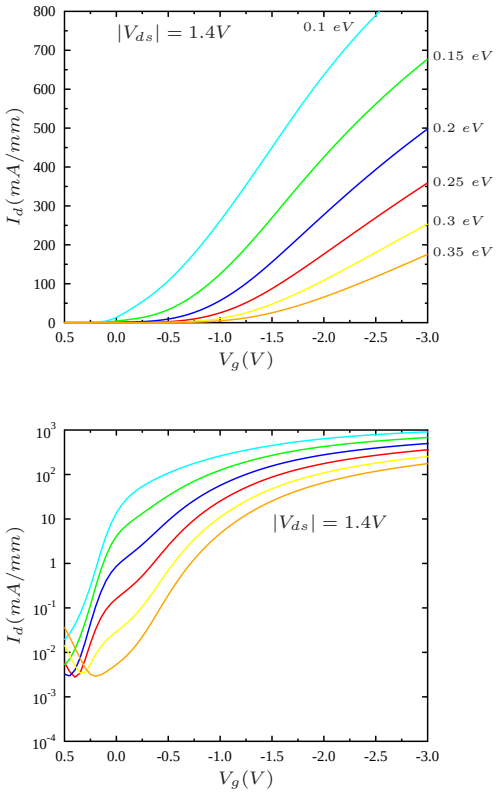

Fig.4: *Simulated drain currents for V_{ds}=1.4V for Schottky barrier heights from 0.10 eV to 0.35 eV..*

4. Conclusions

We have made a first study of the behaviour of p-channel SB-MOSFETs under low and high drain/gate bias without barrier lowering effects applied to field emission calculations. Nevertheless, a convenient interpretation of the obtained results regarding the different zero-bias barrier heights introduced by hand as the result of some barrier lowering mechanism leads us to confirm the expected dramatic influence that these lowering effects have in the current of these devices.

Next step will be to develop some kind of procedure as done in [4] that allows the inclusion of these effects as well as include implementation of quantum effects.

References

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