Negative Differential Resistance in Top-Gated Chemical Vapor Deposition Grown Graphene Transistors

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Abstract

Negative differential resistance (NDR) is a phenomenon in which an increase in voltage across the device's terminals results in a decrease in electric current through it. This is in contrast to a resistor in which an increase of applied voltage causes an increase in current due to Ohm's law. This unique phenomena can be exploited in numerous interesting applications, including high frequency oscillators, amplifiers, logic, memories and analog-to-digital converters. The NDR behavior can be realized with graphene transistors at high fields, thanks to its field-dependent carrier density and carrier-dependent saturation velocity, and has been demonstrated experimentally by few groups. [1]–[3]

In this work, we report the observation of NDR in the output characteristics of graphene transistors fabricated using monolayer graphene grown by large-scale chemical vapor deposition process. The NDR here was demonstrated for various channel lengths ranging from 200 nm to 5 µm by employing wide channels, small un-gated regions, dual gating and thin top-gate dielectric. [4]

Figure 1 shows the schematic view of the fabricated graphene transistor. Figure 2 shows the transfer characteristics of graphene transistor for 500 nm long and 30 µm wide channel having an equivalent oxide thickness of 2.5 nm. [4] Figure 3 shows the output characteristics for the same device. At the bias $V_{BG} = -40$ V, we see the decrease in the drain current (I_{SD}) as drain voltage (V_{SD}) is increased beyond V_{SD}> 1.5 V, resulting in NDR. This effect is also reflected in the corresponding differential conductance ($g_{DS} = \frac{dI_{SD}}{dV_{SD}}$) showing negative values between V_{SD} = 1.5 V and V_{SD} = 1.98 V.

We have proposed a novel explanation for the mechanism behind this unusual feature of graphene, relating NDR with the interplay between the field dependent carrier modulation and the drift velocity in graphene transistors. [4] In addition, we have also shown that the NDR phenomenon in graphene can be realized in transistors with relatively thicker oxide, however, the NDR in this case is achieved at relatively higher gate voltages and has a lower maximum negative differential conductance value. [4] Our demonstration of NDR using graphene grown by production-worthy CVD process opens up a new route for graphene's application in oscillators, amplifiers, switches, memories *etc*.

References

[1] Y. Wu, D. B. Farmer, W. Zhu, S.-J. Han, C. D. Dimitrakopoulos, A. A. Bol, P. Avouris, and Y.-M. Lin, *ACS Nano*, vol. 6, no. 3, pp. 2610–2616, 2012. [2] G. Liu, S. Ahsan, A. G. Khitun, R. K. Lake, and A. A. Balandin, *J. Appl. Phys.*, vol. 114, no. 15, p. 154310, 2013. [3] S.-J. Han, D. Reddy, G. D. Carpenter, A. D. Franklin, and K. A. Jenkins, *ACS Nano*, vol. 6, no. 6, pp. 5220–5226, 2012. [4] P. Sharma, L. S. Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, *ACS Nano*, Article ASAP, http://dx.doi.org/10.1021/nn5059437

Figures

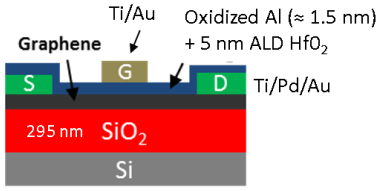

Figure 1 Schematic view of graphene transistor on Si/SiO_2 substrate.

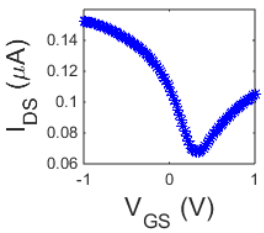

Figure 2 Transfer characteristics of 500 nm long and 30 µm wide channel at V_{BG} = 0 and V_{DS} = 0.01 V.

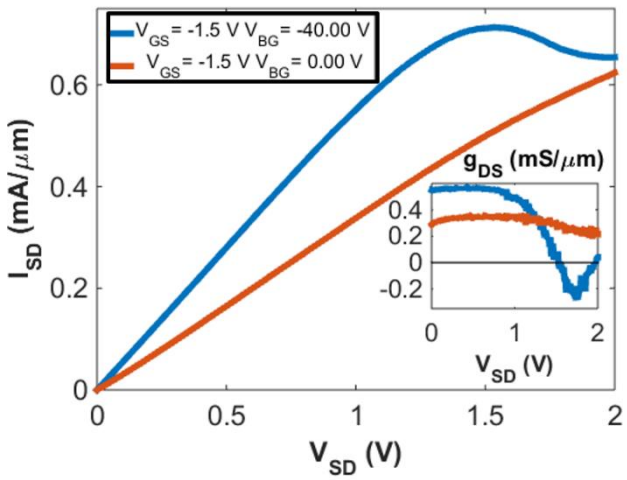

Figure 3 Drain current as a function of source-drain voltage for the same transistor as in Figure 2. Inset shows the corresponding differential conductance (g_{DS}) as a function of source-drain voltage. NDR was not observed for V_{BG} = 0 V because of higher series resistance as compared to the V_{BG} = −40 V.