

# Graphene Distributed Amplifiers: Generating Desirable Gain for Graphene Field-Effect Transistors

Hongming Lyu, **Huaqiang Wu\***, Yilin Huang, Jinyu Zhang, Xiaoming Wu, Zhiping Yu and He Qian

Institute of Microelectronics, Tsinghua University, Beijing, China 100084  
wuhq@tsinghua.edu.cn

## Abstract

The gapless energy band-structure in graphene results in good transport properties of carriers such as high mobility and high Fermi velocity. These physical properties are of great interests for electronic applications and have motivated many research groups to develop radio frequency (RF) and microwave graphene field effect transistors (GFET). However, due to the lack of saturation regions, GFETs have generally been regarded as being hard to provide substantial gain.

In this paper, the distributed amplification scheme, which has been in existence for decades<sup>1-4</sup>, is applied to graphene, creating a new approach to realizing graphene wideband amplifiers. Inductors are built between GFET stages. With the intrinsic capacitances of the GFET, gate and drain artificial transmission lines are formed. In this way, while the capacitances of the GFET stages are separated, the transconductance of each stage,  $g_m$ , may be combined in an additive manner. If the GFETs are phase synchronized, the combined gain can be increased almost without limit. The topology exactly overcomes the GFETs' difficulty in amplification. In conventional semiconductor amplifiers, engineers cannot increase the gain-bandwidth product by parallelizing field-effect transistors, because the resulting increase in transconductance  $g_m$  is compensated for the corresponding increase in the input and output capacitances. The distributed amplification topology, however, solves this problem by adding the individual  $g_m$  of the transistors without adding their input and output capacitances. The schematic diagram of GDA is illustrated in Figure 1, hypothetically realized in our inverted processing technology. Inductors lie in the first metal layer and capacitors form between both layers. GFETs sit at the top, so that contaminations from BEOL processes are eliminated.

Circuit evaluation starts with appropriate compact device models. The corresponding complete equivalent circuit is shown in Figure 2. The resulting I-V characteristics are shown in Figures 3 and 4. The S-parameters are shown in Figure 5. At a comparable bias ( $V_{ds} = 1V$ ,  $V_{gs}$  being the same respect to the Dirac point), the GFET compact model produces similar performance, as shown in Figure 5(b). The structure of a graphene distributed amplifier is shown in Figure 6.

Simulated performance of 2-, 4-, 6-, 8-stage GDAs optimized at 1GHz are shown in Figure 7. All circuits operate at 0.45V and 1.0V gate and drain bias, respectively. At this biasing condition, the GFET features  $f_T=8.3GHz$  and  $f_{max}=9.9GHz$ , as shown in Figure 7(a), with the inset showing the S-parameters. Figures 7(b) through (d) represent 2-, 4-, 6- and 8-stage GDAs, respectively. Optimization of the 4-stage DA results in  $C_g = 2.9pF$ ,  $C_d = 3.0pF$ ,  $L_g = 23.9 nH$ ,  $L_d = 22.4 nH$ . (Higher design frequency will lead to lower values)  $C_g$  and  $C_d$  being an order of quantity larger than the GFET's gate capacitance, identical propagation velocities of the gate and drain line are satisfied. 2-stage GDA shows 8dB Gain at 0.9GHz. Both the bandwidth and the gain are increased with the number of stages. Reflected power at the input and output from 50Ω load, represented by S11 and S22 respectively, are practically below -10dB over the bandwidth in all the designs. Gain of the 8-stage GDA exceeds 15dB at 1GHz. Figure 7(f) plots 2-, 4-, 6- and 8-stage GDAs' gain in one chart.

The distributed amplification's ability to add transconductances of transistors while separating their capacitive parasitics makes it possible to achieve wide bandwidths. Another set of designs was optimized for wideband applications. Optimization results in an order lower  $C_g$ ,  $L_g$ ,  $C_d$  and  $L_d$  values, consistent with larger transmission line bandwidth. An 8-stage GDA design achieves 9dB gain with flatness  $\pm 1dB$  over 0-4.5GHz is shown in Figure 8(a). A 16-stage GDA features 13dB gain and a unity-gain bandwidth of 8GHz, as shown in Figure 8(b).

In summary, a graphene distributed amplification scheme is proposed. Against graphene's long-existing problem of weak amplification capability, this topology substantially expands graphene amplifier's gain-bandwidth product by separating capacitance while adding (in stead of multiplying) the transconductance. In order to perform the simulation, a compact model is first studied. Simulation results show that even modest-performance GFET can achieves wide-band amplification with gain over 10dB.

## References

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- [3] Majidi-Ahy, R., et al. IEEE Trans. MTT, 38(1990) 1986-1993.
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# Figures

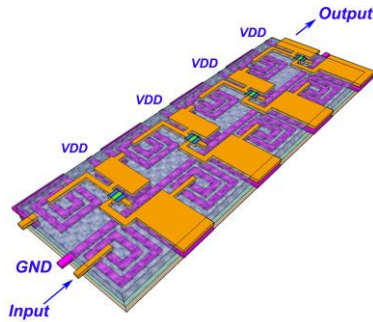


Figure 1. Schematic of a graphene distributed amplifier realized by an inverted processing technology.

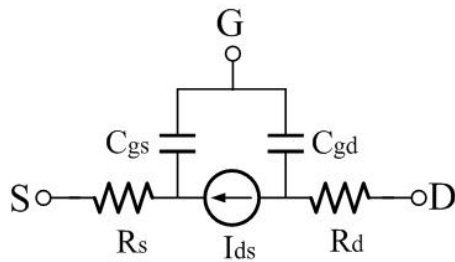


Figure 2. Equivalent circuit of the GFET compact model.

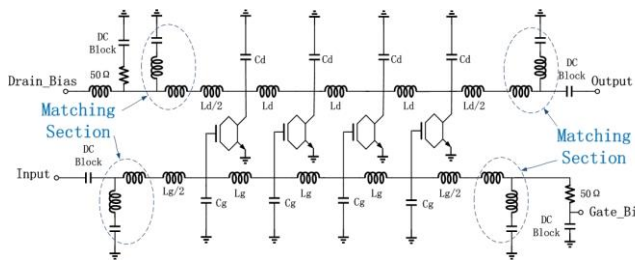


Figure 6. The structure of a graphene distributed amplifier.

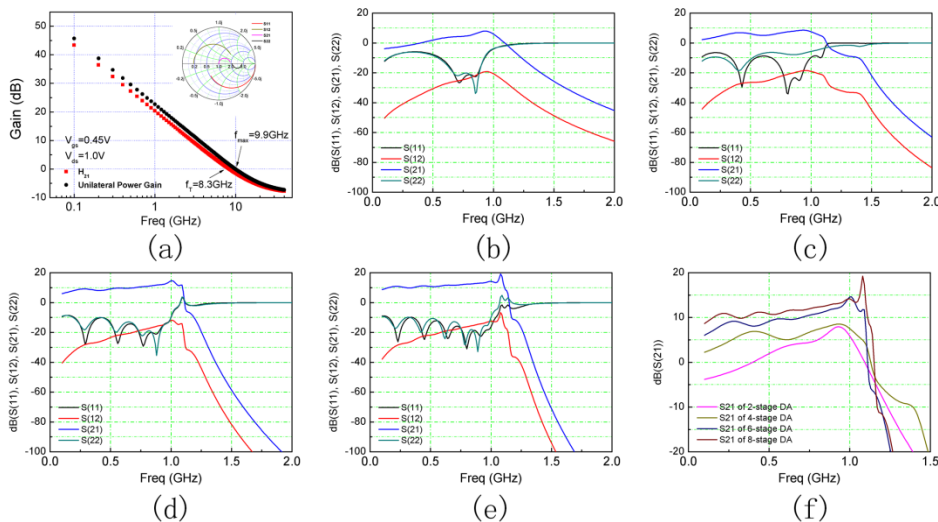


Figure 7. (a) The GFET model's performance at working condition of 0.45V gate bias and 1.0V drain bias. (b)-(e) Simulated performance of 2-, 4-, 6-, 8-stage GDAs optimized at 1GHz. (f) S21 comparison among the 2-, 4-, 6-, 8-stage GDAs.

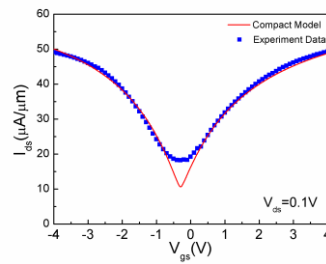


Figure 3. Transfer characteristics of the model with comparison to measurement.

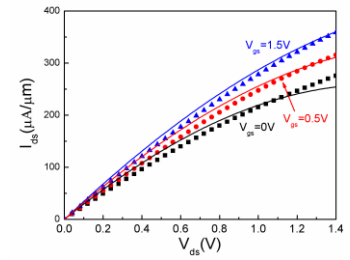


Figure 4. Output characteristics. Symbols represent experiment data and solid lines the compact model results.

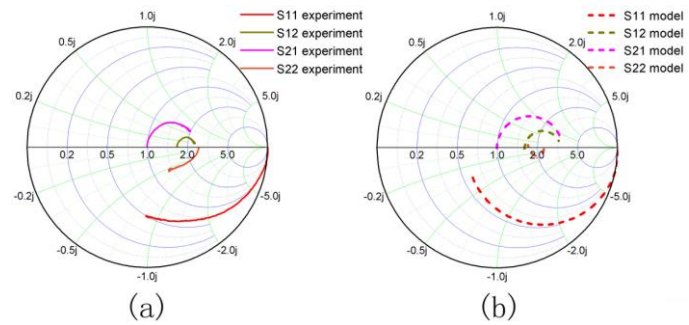


Figure 5. (a) S-parameters of a fabricated 500nm-gate-length GFET with modest-performance. (b) S-parameter prediction of the 500nm-gate-length GFET compact model with comparable bias.

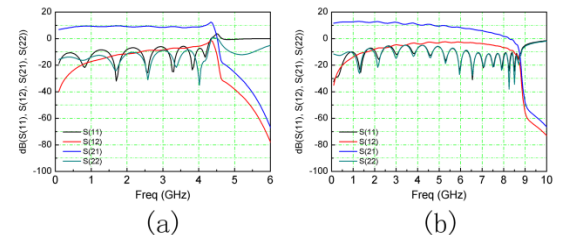


Figure 8. (a) An 8-stage GDA that achieves 9dB gain with flatness  $\pm 1$ dB over 0-4.5GHz. (b) A 16-stage GDA with gain 13dB and unity-gain bandwidth 8GHz.