Graphene field-effect transistor with a solution-processed gate dielectrics and UV-ozone-treated graphene/metal electrodes

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Theoretically, graphene has extremely high mobilities around 200,000 cm^2/Vs, which is more than 100 times higher than that of silicon. Thus, graphene-based field-effect transistors (GFETs) have been intensively investigated in recent years aiming at replacing silicon-based MOSFETs. The scaling down strategy of Si-MOSFETs is expected to reach physical, technical, and cost limits in the near future. There are however several challenges remaining in GFETs that impede their development. Among them are the carrier mobility degradation by gate dielectrics and the high contact resistance between graphene and metal electrodes. These two factors severely screen the excellent properties of pristine graphene in GFETs. In this work, we propose a solution process to form a qualified gate dielectrics. This novel method, together with a UV-ozone treatment to realize lower metal/graphene contact resistance, brings about substantial betterment of GFET performance.

A CVD graphene layer was transferred onto a Si substrate covered with a 90 nm-thick SiO_2 layer. To define the source/drain region, image reversal photolithography was conducted using AZ5214E. After a UV-ozone treatment to remove the photoresist residue, Ni was e-beam evaporated to form contact electrodes. Gate formation consists of three steps. First, an Al ultrathin layer (2 nm) was directly deposited onto graphene by e-beam evaporation, which turns into an ultrathin Al_2O_3 natural oxide layer in the atmospheric ambient. This first layer can be omitted, but it suppresses the unwanted doping to graphene. Second, an Al_2O_3 precursor solution was spin-coated onto this substrate, which was exposed to an oxygen plasma at room temperature and annealed in air at 250ºC for 2 hours. Finally, gate electrode of Al (150 nm) was deposited by e-beam evaporation. Doping, strain, and defects in graphene have been evaluated by Raman scattering measurements. Figure 1 shows the drain current as a function of the gate voltage. The Dirac point, i.e., the minimum conductivity point, is rarely shifted within ~0.1V, indicating that the graphene underneath the gate dielectrics is almost in its charge neutral states. To evaluate the intrinsic carrier mobility μ and the contact resistance R_c of the GFET, the total resistance R_T as a function of the gate voltage has been fitted with the following formula [1] (figure 2):

$$R_T = 2R_C + \frac{L}{We\mu\sqrt{n_0^2+n^2}} \quad . \quad (1)$$

Here n_0 is the residual carrier concentration, n is gate-induced carrier density, and L and W are the channel length and width, respectively. By this fitting, we extract values of n_0 =2.2 × $10^{11}cm^{-2}$, μ=8600 cm^2/Vs and R_c=900 Ω·um. These high μ and low R_c values are one of the best to the authors knowledge.

To summarize, we have successfully developed GFETs with solution-processed gate dielectric and UV-ozone treated contacts. As we confirm very high mobility and low contact resistance in the devices, the present combination of solution-processed gate dielectrics and UV-ozone treated contacts is quite promising for realizing high performance graphene FETs.

References

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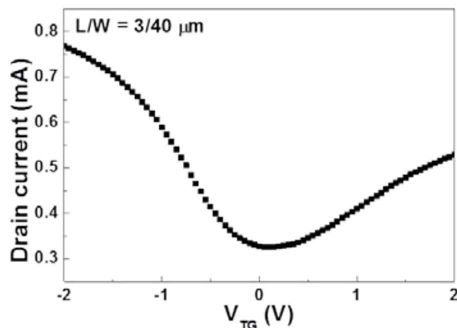

Fig. 1 Drain current as a function of the gate voltage.

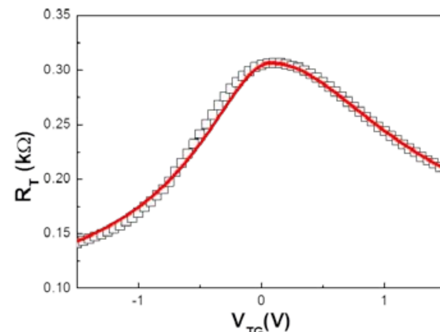

Fig. 2 Measured R_T (open squares) versus V_{TG} fitted with equation (1) (solid line).