A Theoretical Study of the Electrostatics and Electronic Transport of the Graphene Barristor

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Abstract

Although transistors based on silicon technology have continued improving their speed and integration density over the years, their extreme reduction of the channel length causes inevitable leakage currents, being increasingly difficult to follow Moore's law. To overcome the problems related with scalability, a variety of technologies and active materials have been proposed over the past years. Among them, the graphene-based transistor came up as a potential candidate because its appealing physical properties such as a very large mobility and saturation velocity. However, because graphene has no band gap, only a small on/off current ratio can be obtained on conventional graphene transistors [1]. To circumvent the problem, Samsung researchers introduced a class of three-terminal devices based on a graphene-silicon hybrid device that exhibits a large current ratio I_{on}/I_{off} (~10^5) [2]. They have named this barrier variable device as "barristor" (GB) (Fig.1a). The key GB function takes place at the electrostatically gated graphene/silicon interface where a tunable Schottky barrier controls charge transport across a vertically stacked structure (Fig. 1b). In order to gain a deeper insight into the GB operation, we present a theoretical study of GB electrostatics, so the relation between the applied biases and both the graphene shift Fermi level (ΔE) and the Schottky barrier height (ϕ_b) could be properly understood, even in the presence of a chemical doping in the graphene. Other important aspect we have looked into is to what extent the transport theory of the conventional metal-silicon Schottky junction, where the metal is a bulk (3D) material, is appropriate in describing the GB characteristics. In this regard, we have explored the fundamentally different case of graphene-silicon Schottky junction, where graphene is a flat (2D) material.

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[1] Frank Schwierz, "Graphene transistors", Nature Nanotechnology 5, 487 (2010).

[2] Heejun Yang *et al.,* "Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier", *Science* 336, 1140 (2012).

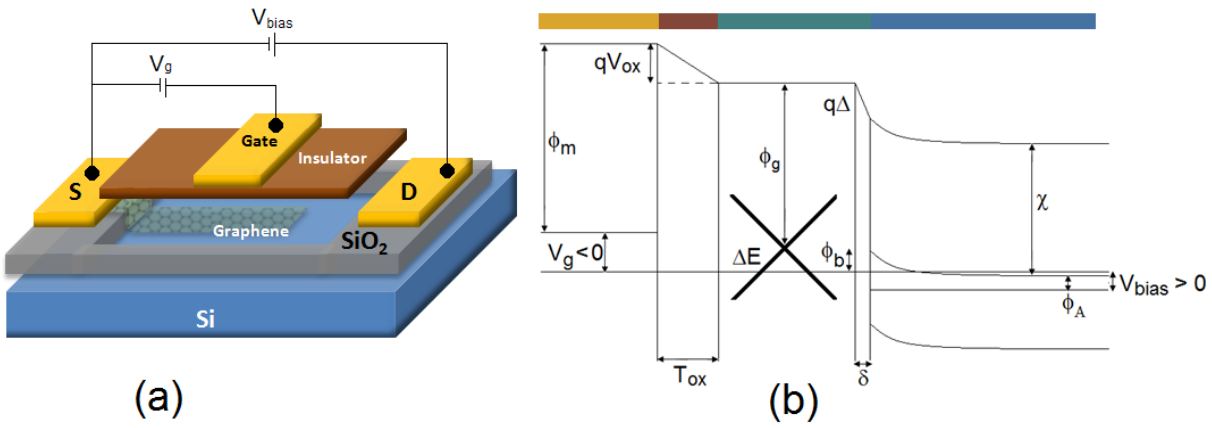

Figure 1.(a) Scheme of the Graphene Barristor proposed by Samsung in Ref. [2]; (b) Band diagram along a vertical cut along the gate stack.