

Graphene Synthesis, Transfer, FETs and Scaling

Kenneth Teo*, Nalin Rupesinghe, Andy Newham, Paul Greenwood, Matthew Cole
AIXTRON, Cambridge, United Kingdom

Li Tao, Jongho Lee, Deji Akinwande
University of Texas at Austin, USA

Kemal Celebi, Hyung Gyu Park
ETH Zurich, Zurich, Switzerland

Jie Sun
Chalmers University of Technology, Sweden

Tim Booth, Peter Boggild
Technical University of Denmark, Denmark

*Presenting author: k.teo@aixtron.com

Growth and characterization of graphene grown using copper foils as well as copper films on silicon dioxide on silicon substrates were performed. Kinetics of growth and effective activation energy for the graphene synthesis will be discussed for the surface catalytic synthesis of graphene. Conditions for large-scale synthesis of monolayer graphene will be addressed in this talk. Wafer-scale graphene transfer and electrical results will be presented. Based on our preliminary results from capped 100-mm wafer scale graphene transistors, we expect a mobility of 4-6 k cm²/Vs with symmetry hole/electron transport. In addition, important circuit blocks such as frequency multipliers and amplifiers with gain of about five have been achieved. Integrating the CVD graphene with Si VLSI chips affords interconnects and gas sensors that utilize the resistance modulation of graphene. Likewise, graphene integrated onto flexible sheets yield 25GHz cutoff frequency and robust performance down to 0.7mm bending radius which represents the state of the art for graphene nanoelectronics on soft substrates. Key considerations and challenges for scaling are discussed and results for graphene growth on the 300mm wafer scale will be discussed.