Graphene-based Integrated Circuits: From an Inverter Towards a Ring Oscillator

Daniel Schall, Daniel Neumaier, Heinrich Kurz

AMO GmbH, Otto-Blumenthal-Strasse 25, 52074 Aachen, Germany
schall@amo.de

Abstract

High frequency transistors, the core of modern information and communication systems, have been recognized from the very beginning as one of the most promising fields of applications for graphene having the potential to significant outperform transistors based on Silicon and III/V semiconductors in terms of speed. This large expectation has mainly been fuelled by graphene's outstanding charge carrier mobility, the large saturation velocity and the 2D nature giving prospects for ultimately scaled devices. Although single graphene transistors have already proven these expectations by delivering high cut-off frequencies up to 420GHz [1], the realization of integrated circuits based on graphene transistors is still in its embryonic stage. To date the most complex integrated circuit based on GFETs are a mixer with one GFET and passive components operating at GHz frequencies [2] and an inverter operating at kHz frequency and consisting of one p and one n type GFET [3]. The realization of more complex circuits containing several GFETs was so far limited by the process technology, which did not allow the highly reproducible fabrication of GFETs with designed properties.

Here we demonstrate the realization of integrated inverters consisting of one n and one p type GFET with record voltage gain A_V = 20. The GFETs are based on CVD grown graphene and ambivalent operation was achieved by biasing as previously shown in [3]. High voltage gain has been achieved using a local back-gate geometry (see figure 1c). This unique geometry allows the fabrication of high quality Al_2O_3 with an EOT of 3 nm, avoiding the rather complex deposition of dielectric layers on-top of the graphene. Input-output matching of the operation voltages in single inverters was realized by proper control of the individual process steps and the thereto related unintentional doping.

Based on such inverters as major building blocks and a highly reproducible process technology, we realized the first graphene based integrated ring oscillator. The ring oscillator consists of 6 n-type and 6 p-type transistors, so that 5 inverters from a loop, while one inverter is needed to decouple the loop from the measurement equipment. An optical micrograph (false color) and a corresponding circuit diagram are shown in figure 1a and 1b, respectively. The fundamental oscillation frequency f_{OSC} of the ring oscillator is ranging from 20 to 30 MHz depending on the supply voltage (figure 2b). This is consistent with the intrinsic parameters of the circuit. The delay time of one inverter is given by $\tau = 1/2nf_{Osc}$ = 3 ns at V_{DD} = -3 V. Taking into account the large parasitic capacitance, which are in our design mainly related to the large overlap between the gate electrode and source and drain, we get an intrinsic delay time of a single inverter of 0.3 ns.

This work was financially supported by the German Science Foundation DFG under the project Ultragraphen (BA3788/2-1) and by the European Commission under the project GRAFOL (285275).

References

[1] R. Chen et al., PNAS doi: 10.1073/pnas.1205696109 (2012).
[2] Y.-M. Lin et al., Science 332, 1294 (2011).
[3] L.G. Rizzi et al., NanoLetters 12, 3948 (2012).

Figures

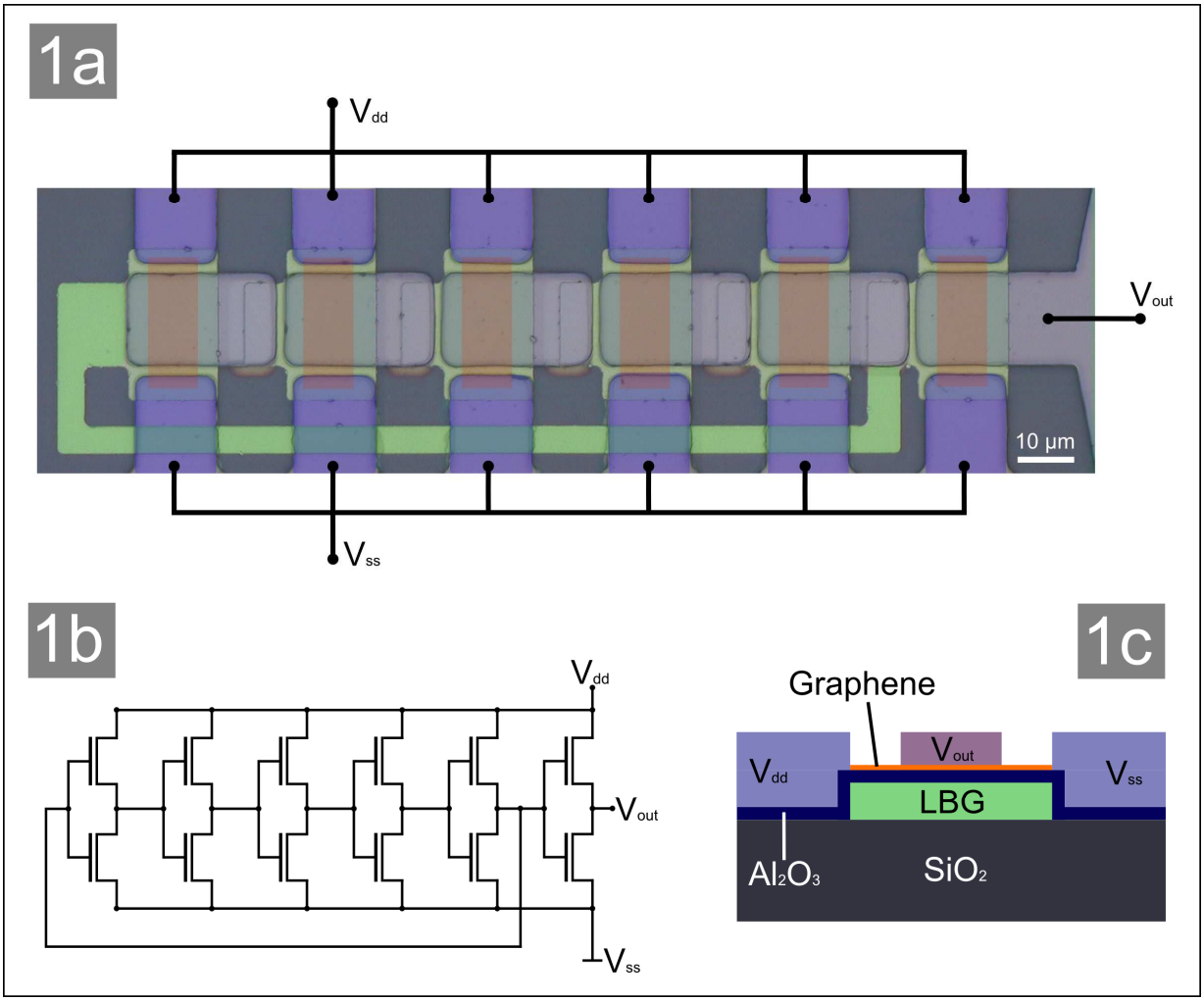

Fig.1. a) Optical micrograph of an integrated ring oscillator (false color). b) Circuit diagram of the ring oscillator. c) Schematic of a single inverter stage.

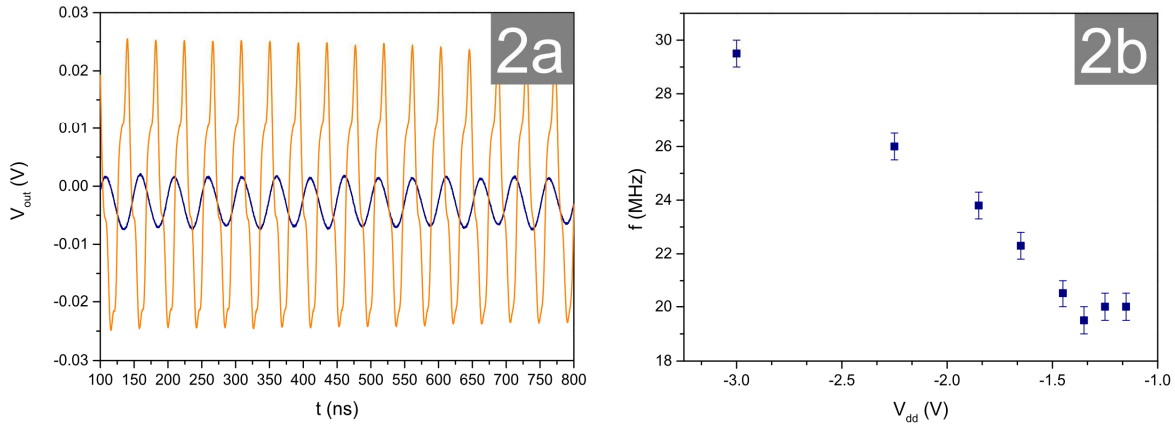

Fig.2. a) Time transient of the output voltage of the ring oscillator. b) Fundamental oscillation frequency of the ring oscillator as a function of the supply voltage.