Graphene-Organosilane Memory Cell Based on Charge Transfer Hysteresis

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Abstract

One of the most striking features of graphene is that the electrons/holes are confined to a plane of atomic thickness, making graphene devices sensitive to the surrounding environment. In this study, a prototype memory cell based on charge transfer between graphene and organosilane self-assembled monolayer (SAM) has been demonstrated. 3-Aminpropyltriethoxysilane (NH_2-silane) has been used to modify SiO_2 substrates, which has been proven to enhance graphene transfer integrity due to stronger Van der Waal's force[1]. To apply this organosilane, substrates with 90 nm thermally grown SiO_2 were immersed in 2 wt % NH_2-silane ethonal solution. During the process, silane groups reacted with hydroxyl groups and are chemically bonded to SiO_2 surface[2], as shown in Fig.1(a). Graphene in this study was synthesized by APCVD method and transferred by electrochemical bubbling technique [3]. Raman spectrum of graphene on NH_2-silane SAM is shown in Fig. 2. The absence of D-band proves high quality of the graphene without defects, and high peak intensity ratio of G-band to 2D-band indicates charge carrier doping induced by proximity effect of NH_2-silane molecules [2]. Bottom gate graphene field effect transistors (GFET) with channel dimension of 300μm*250μm were fabricated on those treated substrates, as illustrated in Fig. 1(b). Source/Drain electrodes, Ti/Au (5nm/45nm), were evaporated through shadow mask and graphene channel was patterned by conventional photolithography followed by oxygen plasma etching. This type of device patterning is easily applicable and contaminations from photoresist residues are reduced. Electrical characterization of these bottom gate GFETs shows significant and reproducible hysteresis in conductance. Fig. 3 compares transfer curves of GFETs with and without NH_2-silane interface engineering. With gate voltage sweeping speed of 2.1V/s, the hysteresis window in NH_2-silane case is 36V in -50V-to-50V range, which is 8 times larger than the counterpart on untreated SiO_2. Hysteresis phenomenon is explained by electron transfer between graphene and trapping sites in dielectric underneath. Significant enhancement of hysteresis in NH_2-silane case is attributed to the charge trapping/detrapping properties of electron lone pairs of nitrogen atoms[4]. At zero bottom gate voltage, a 4X change in graphene channel resistance is observed. Reproducibility of transfer curve is further studied by comparing its minor shifts under ambient atmosphere and in vacuum. Fig. 4(a) shows that transfer curves shift in positive direction under ambient atmosphere, which is unfavorable from memory window point of view. In vacuum, however, transfer curves are very stable, with Dirac points slightly heading zero and electron/hole branches getting more symmetric, as shown in Fig. 4(b). These results indicate that absorbates from the air cause non-negligible p-doping for the exposed graphene device, while electro-cleaning effect in vaccum produces favorable stabilized memory characteristics. For better memory performance, air absorbates are to be avoided via packaging in future memory cell fabrication. Even under ambient atmosphere, memory window remains above 1.6X over 100 sweeping cycles, as shown in Fig. 5. Pulse program/erase was applied to those devices. A stable 2X memory window is observed. Those memory effects are more sensitive to pulse height rather than width, as shown in Fig. 6. Memory cell functionality was further examined through retention test. Fig. 7 shows that the resistance difference between high and low values decays slowly with time. In summary, we demonstrated graphene device with nonvolatile memory effects which show significant promise as a prototype for flexible and transparent memory applications. Further device optimization, trapping layer design and packaging would greatly improve the memory performances.

References

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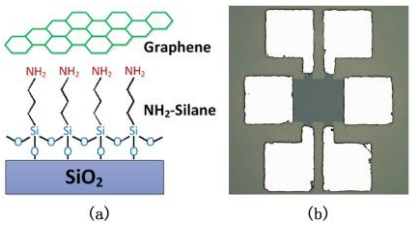

Fig. 1. (a) Schematic of graphene transfer with NH_2-silane interface engineering. (b) Optical image of the as-fabricated device.

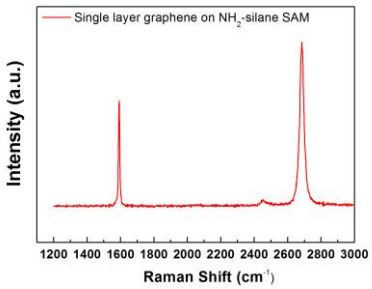

Fig. 2. (a) Raman spectrum of graphene/NH_2-silane SAM.

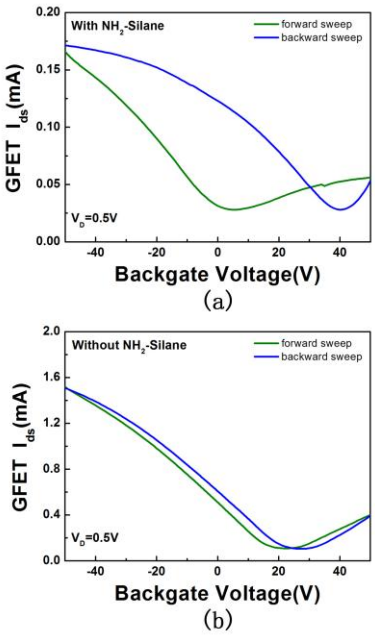

Fig. 3. Transfer curve of GFETs with (a) and without (b) NH_2-silane interface engineer.

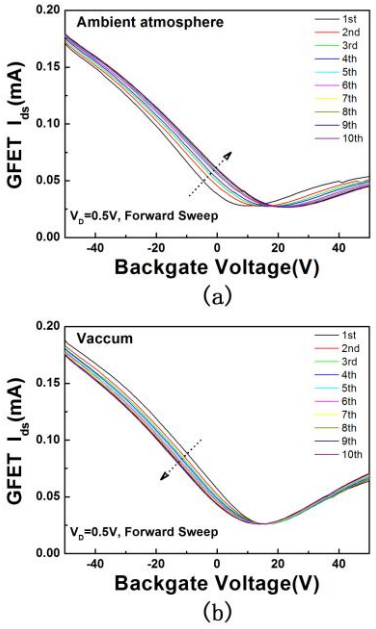

Fig. 4. GFET transfer curve shifts under ambient atmosphere (a) and in vaccum (b).

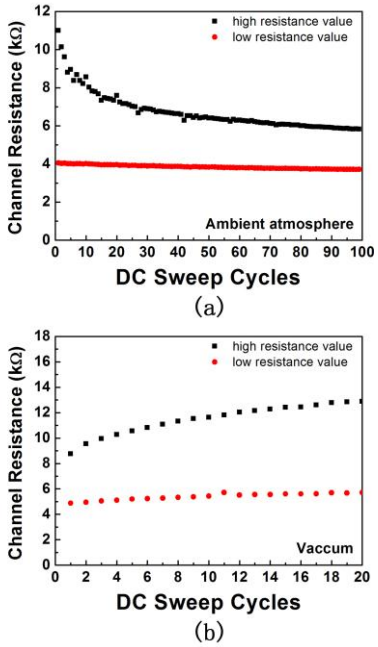

Fig. 5. DC sweep cycling endurance under ambient atmosphere (a) and in vaccum (b).

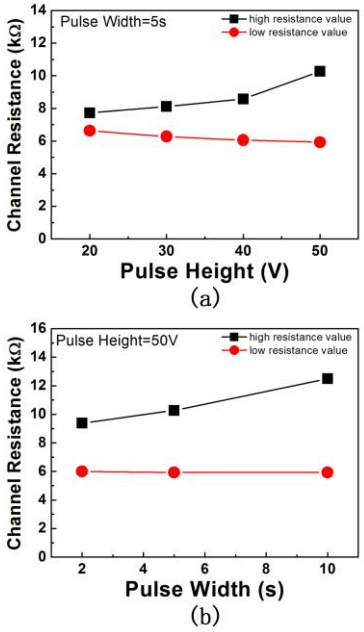

Fig. 6. Channel resistance change in pulse program/erase mode. Pulse width and height is kept constant in (a) and (b), respectively.

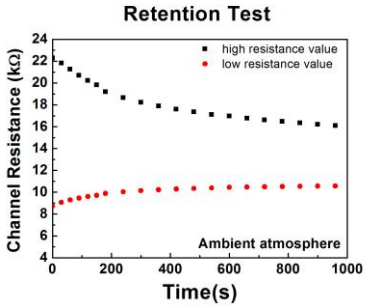

Fig. 7. Channel resistance versus time for two different charge states. The resistance difference decays slowly with time as the stored charge decays.