Preparation and characterization of reduced graphene oxide deposited on Si/SiO_2 wafer by rod coating technique

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Abstract

Conducting and transparent large area graphene films can find many application such as touch screens, antennas, circuits, or as resistivity heaters. Here we present easy, fast and scalable method of producing graphene oxide films by rod coating method.

Graphene oxide films were deposited on Si 2" wafer with thermally grown 200nm thick SiO_2 layer. The graphene oxide layers were reduced in the RTP oven in an Ar/H_2 atmosphere at temperatures of 700, 800, 900 and 1000°C. The annealing time was 3 min. The reduction process was followed by lithography and isolation etching in oxygen plasma. Finally the pattern of electrical contacts was defined in subsequent photolithography step followed by Ti/Au metallization evaporation and lift-off.

The TLM structures were measured across 2" wafer and the basic statistics out of 100 measured devices for each reduction process were calculated. All devices exhibited excellent linear I-V characteristics. In table I one can see evolution of layer resistivity with increase of reduction temperature.

Tab. 1
Resistivity of reduced GO layers

Temperature of reduction	Sheet resistivity kΩ/sqr	remarks
700	125	
800	44.8	
900	19	First symptoms of delamination
1000	46	Delamination and peeling

The thickness of layer was measured with mechanical surface profiler. Its value does not depend on reduction temperature and equals 6-8 nm.

The Raman spectra were measured for each reduction process and two strong peaks D and G were observed along with small 2D peak. The FWHM of the D modes is reduced as temperature increases while G band FWHM stays at the same level. This trend is continuous and exhibits no saturation. We attribute D band width evolution to the defect annealing (i.e. oxygen reduction). 2D band is single mode graphene like for 800°C reduction process and becomes wide - graphite like for higher temperatures. This trend we attribute to interaction of carbon layers in a stack which is preferred when reduction degree of GO increases.

Further carrier transport test are planned to explore RGO feasibility for fabrication of cheap devices on liberally chosen substrates.