Tailoring the graphene/silicon carbide interface for monolithic wafer-scale electronics

Stefan Hertel[1], Daniel Waldmann[1], Johannes Jobst[1], Andreas Albert[1], Matthäus Albrecht[1], Alexander Glas[1], Sergey Reshanov[2], Sascha Preu[1], Adolf Schöner[2], Michael Krieger[1] & Heiko B. Weber[1]

[1] Chair for Applied Physics, Friedrich-Alexander University Erlangen-Nuremberg, Staudtstr. 7, 91058 Erlangen, Germany
[2] ACREO AB, Electrum 236, Isafjordsgatan 22, 16440 Kista, Sweden
Stefan.Hertel@FAU.de

Graphene has many favorable properties for future electronics, e.g. extremely high current stability[2], high thermal conductivity and temperature stability[3] and excellent charge carrier mobility[4]. The latter should result in fast transistors, which have already been demonstrated[5]. However, due to the missing gap in graphene's band structure it is fairly hard to design an efficient switch for logic applications[6].

As epitaxial graphene grown by thermal decomposition of silicon carbide (SiC) (0001) [7] is intimately connected to the SiC we consider the bare graphene layer together with the substrate and their common interface as one material system, in which SiC provides a wide-bandgap semiconductor[8], and graphene acts as a metal. There, the graphene physics come into play: due to its atomically thin shape, the interface tunes its Fermi level, which is not possible for other metals. We are able to tailor that interface to form ohmic and Schottky-like contacts by means of hydrogen intercalation[9].

We developed a scheme to fabricate both interface types side by side on the same chip leading to a monolithic epitaxial graphene transistor with ON/OFF ratios exceeding 10^4 under ambient conditions (Fig. 1). We proof the concept's capability for logics by presenting an integrated inverter (Fig. 2) as well as NAND and NOR gates without any additional components. Using a Schottky diode built within the same fabrication scheme, and connected to two suitable antennae, we are able to realize a fast and efficient THz detector.

References

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Figures

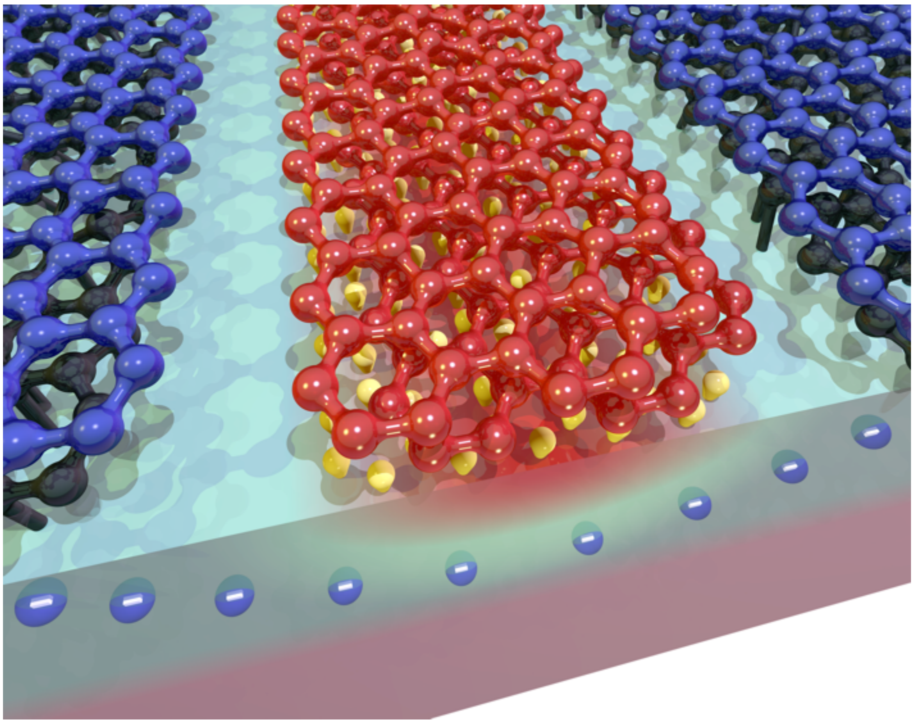

Figure 1 Artist's impression of a monolithic epitaxial graphene transistor. Current flows from as-grown monolayer graphene (blue) through an ohmic interface into the silicon carbide (SiC) channel (cyan). The quasi-freestanding bilayer graphene (red) provides a Schottky-like contact to the conducting SiC layer, which can be pinched of by the corresponding space charge region.

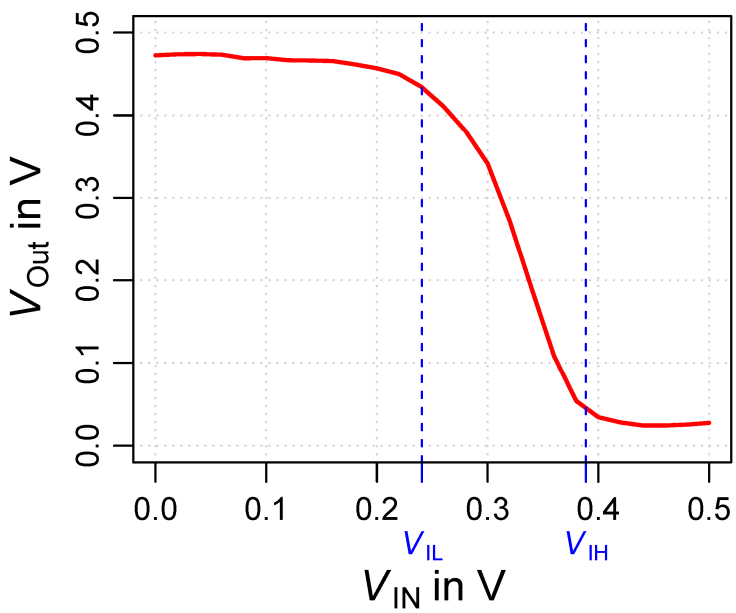

Figure 2 Voltage transfer characteristic of an inverter. V_{IL} and V_{IH} indicate noise margins for the input signal.