Making large area graphene field-effect transistors (FETs) without polymer resists

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The conventional way to produce field-effect transistors (FETs) is by lithographic techniques using polymer resists as a patterning mask. This technique has also been successfully used to make graphene FETs out of small flakes of exfoliated graphene [1] and large area graphene such as graphene grown using chemical vapour deposition [2]. However, the polymer resists usually leave residues reducing the electronic performance of the FET [3]. Here we report a simple and reliable process to fabricate large area graphene FETs (1 mm^2) without using polymer resist. Our procedure can be used as a tool to quickly map the electronic properties of large area graphene on insulating substrates.

The recipe is schematically depicted in figure 1. We use two reactive ion etching steps to pattern a sheet of graphene into the desired shape. Subsequently, we deposit source and drain contacts using shadow-mask e-gun evaporation in vacuum. We applied our recipe to a 1 cm^2 graphene sheet on silicon/silicon dioxide wafer [4] resulting in 12 FETs of 1mmx1mm without employing any polymer resist. The electrical characterization of the prepared graphene FETs is carried out after annealing the devices at 130^0C overnight in a vacuum of 10^{-5} mbar. After annealing, the charge neutrality point is observed to be close to 0 volts applied to the back gate electrode (figure 2), indicating that thermal annealing has successfully removed dopants.

References

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[4] Samples were obtained from Graphene Supermarket Inc. The graphene was grown using chemical vapour deposition on copper and subsequently transferred to a Si/SiO_2 wafer.

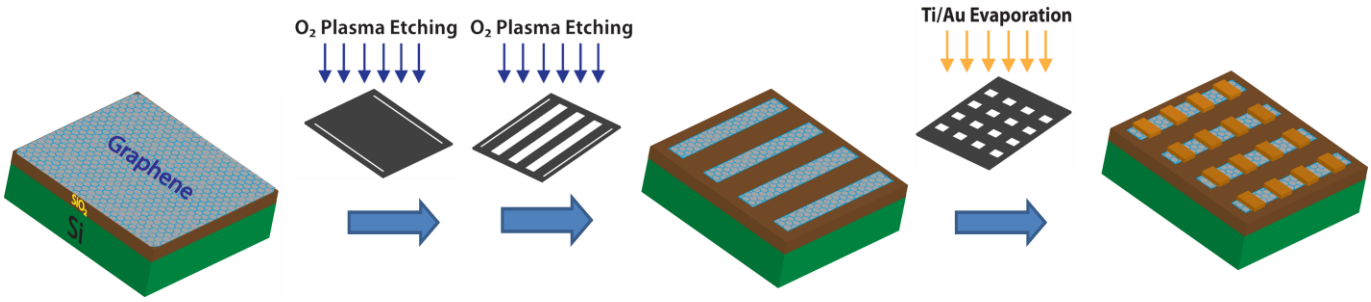

Figure 1: Schematics of the preparation of large area graphene (1 mm^2) field-effect transistors using shadow-mask etching and evaporation.

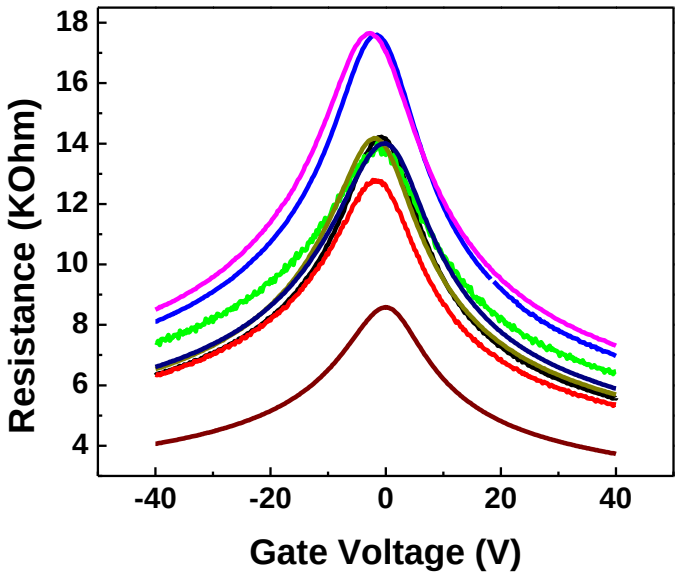

Figure 2: Gate spectroscopy traces of eight large area graphene (1 mm^2) FETs fabricated using shadow-mask etching/evaporation without using polymer resist. The traces were recorded after annealing overnight at 130^0C in vacuum. The variation in resistance of the FETs is attributed to macroscopic deformations such as cracks in the CVD-graphene.