Graphene Materials, Devices and Integration: Challenges and Opportunities

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Abstract

There has been significant progress in graphene research since its isolation. The future of graphene for the electronics industry will depend on our ability to grow it or form it from graphite sources with the desired characteristics that meet the requirements of the specific application. The semiconductor industry is still pursuing devices that meet beyond complementary metal oxide semiconductor (CMOS) device requirements. The current transistor approaches that use FinFET, III-Vs compounds or SiGe for channel materials are expected to meet the device requirements that will bring the transistor to the CMOS limit.[1] In order to meet the beyond CMOS device requirements, such as low voltage, <<1V, operation and continue on the current Moore's law trends, it will be necessary to introduce devices that will be based perhaps on new physics. Graphene-based devices are being explored to meet these requirements and are being studied by many groups, but none of the devices have been demonstrated to meet the requirements yet. Some of the devices studied are (1) graphene tunnel field effect transistor (TFET) [2-4], (2) bilayer pseudospin FET (BisFET)[5], (3) Veselago lens based device [6, 7], and most recently (4) the lateral tunnel FET (LTFET) [8, 9]. However, there are many materials and integration challenges for any of these approaches that are being addressed in order to fabricate of them. But there are still many challenges. For example it is likely that single crystal or very large single crystal graphene will be needed in order to decrease the effects grain boundaries but more importantly it will be necessary to grow films on substrates that have a much lower thermal coefficient of expansion difference with respect to graphene in order to minimize wrinkles, and substrates that lower surface roughness than metals, just to name a few. Dielectrics having a range of dielectric constants, bandgap and band offsets may be necessary depending upon the device structure. The metal contact resistance problem is still to be solved although progress is being made. The objective of this presentation is to review the status of graphene growth, and its integration with dielectrics and metal contacts, and present the status and challenges of fabricating the various proposed devices.

References

[1] *International Technology Roadmap for Semiconductors*. http://www.itrs.net/Links/2011ITRS/Home2011.htm, 2011, p.^pp. Pages.

[2] G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, "Lateral Graphene-hBCN Heterostructures as a Platform for Fully Two-Dimensional Transistors," *ACS Nano,* vol. 6, pp. 2642-2648, Mar 2012.

[3] Q. Zhang, T. Fang, H. L. Xing, A. Seabaugh, and D. Jena, "Graphene Nanoribbon Tunnel Transistors," *IEEE Electron Device Letters,* vol. 29, pp. 1344-1346, Dec 2008.

[4] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE,* vol. 98, pp. 2095-2110, Dec 2010.

[5] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer PseudoSpin Field-Effect Transistor (BiSFET): A Proposed New Logic Device," *IEEE Electron Device Letters,* vol. 30, pp. 158-160, Feb 2009.

[6] S. Chun-Yung and L. Ji Ung, "The ultimate switch," *Spectrum, IEEE,* vol. 49, pp. 32-59, 2012.

[7] V. V. Cheianov, V. Fal'ko, and B. L. Altshuler, "The focusing of electron flow and a Veselago lens in graphene p-n junctions," *Science,* vol. 315, pp. 1252-1255, Mar 2007.

[8] G. Fiori and G. Iannaccone, "Ultralow-Voltage Bilayer Graphene Tunnel FET," *IEEE Electron Device Letters,* vol. 30, pp. 1096-1098, Oct 2009.

[9] M. P. Levendorf, C. J. Kim, L. Brown, P. Y. Huang, R. W. Havener, D. A. Muller, and J. Park, "Graphene and boron nitride lateral heterostructures for atomically thin circuitry," *Nature,* vol. 488, pp. 627-632, Aug 2012.