Application of graphene toward digital electronic device and system

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Abstract

In this talk, applications of graphene for digital electronic devices are presented in three different ways; a channel material of FET, an gate electrode of FET, and an electromagnetic interference (EMI) shielding material.

(1) Graphene, which presents remarkably high electron mobility, has come to the forefront as an alternative channel material for the post-silicon era. However, the natural lack of an energy bandgap hinders the practical use of graphene field effect transistor (FET) devices, especially for digital logic applications. Extensive efforts have accordingly been made to open up the energy bandgap of graphene. However, the bandgap and carrier mobility are in a trade-off relationship in most materials. Once the energy bandgap is opened in graphene, its original physical properties are altered and carrier mobility degradation is unavoidable. It is also unrealistic to attain a bandgap of larger than 0.4 eV, which is the minimum practical requirement for digital circuit applications. Here, we propose a new device structure that does not require opening the bandgap of graphene and therefore can fully utilize the original unique properties of graphene. The new device employs a physical gap along the channel instead of opening graphene's energy bandgap as shown in Fig. 1, and is designed with consideration of producibility and compatibility to conventional complementary-MOS (CMOS) process technology [1]. The physical-gap-channel graphene transistor is implemented on a silicon-on-insulator (SOI) substrate. The device simulation results of the newly proposed device structure reveal successfully suppressed off-state current of ~10^{-9} A/μm, an on/off current ratio of more than seven orders of magnitude, and a subthreshold slope of 2.23 mV/decade, constituting more than a 20-fold reduction relative to the theoretical limitation of conventional metal-oxide-semiconductor (MOS) devices. The proposed device structure demonstrates the feasibility of bringing graphene into the mainstream of semiconductor device technology with minimal changes to current MOS device technology but with substantial improvement in device performance.

(2) Reliability of high-K gate dielectric is one of the most serious concerns in deep scaled CMOS devices for both digital logic and memory device applications. We demonstrate that the high-k gate dielectric reliability is dramatically improved by replacing metal gate electrode with graphene gate electrode. The atomic-scale thickness and flexible nature of graphene completely eliminate mechanical stress in the high-k gate dielectric, resulting in significant reduction of trap generation in the high-k film. Almost all the electrical properties related to reliability of MOSFET such as the positive-bias temperature instability (PBTI), time-dependent dielectric breakdown (TDDB) (Fig. 2), leakage current, etc are significantly improved [2]. Data retention and program/erase properties of charge trap Flash memory are also greatly improved when graphene is used as a gate electrode of the charge trap Flash memory device [3]. As the graphene gate electrode does not require stringent control of defects in graphene, the graphene gate electrode can easily be adopted to the CMOS front-end line, by using variety of graphene synthesis methods including solution-based process and so on. Therefore, the result in this work pioneers the way for the adoption of the new nano-material to conventional CMOS devices to overcome the limitation of the performance and reliability of the current devices in production.

(3) We report the first experimental results on the EMI shielding effectiveness (SE) of wafer-scale monolayer graphene [4]. The prepared monolayer CVD graphene has an average SE value of 2.27 dB, corresponding with ~ 40% shielding of incident waves. CVD graphene shows more than 7 times (in terms of dB) greater SE than gold film. The dominant mechanism is absorption rather than reflection, and the portion of absorption decreases with an increase of the number of graphene layers. Our modeling work shows that plane-wave theory for metal shielding is also applicable to graphene. The model predicts that ideal monolayer graphene can shield as much as 97.8% of EMI. This suggests the feasibility of manufacturing an ultrathin, transparent, and flexible EMI shield by single or few-layer

graphene. As the graphene is found to be an excellent EMI shielding material, it is also successfully applied to 3D IC with mixed signal system as a shielding material.

Figures

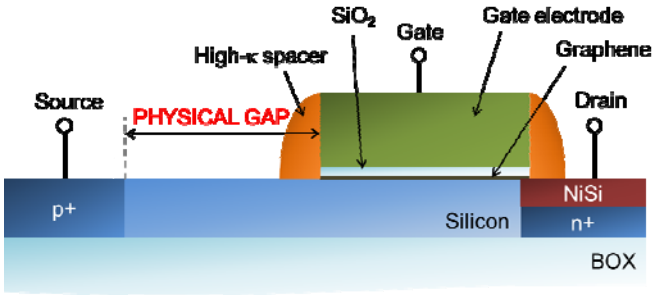

Fig. 1. Schematic drawing of the physical-gap-channel graphene transistor. The graphene channel under the gate is physically separated from the source edge. The source is p+ doped, while the drain is n+ doped. The silicon body is almost intrinsic. A high-κ spacer is used to induce a fringing electric field to the silicon surface.

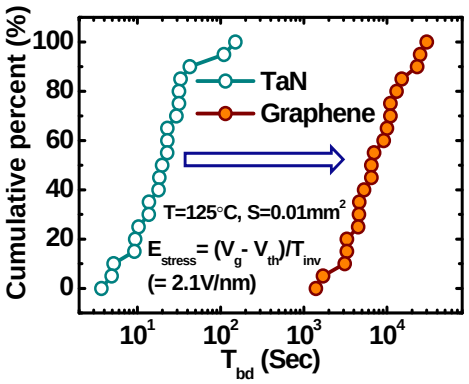

Fig. 2. Time dependent dielectric breakdown (TDDB) property of the devices with two different gate electrodes. Time-to-breakdown of graphene gate device is more than two orders of magnitude higher.

References

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