

## Graphene-enabled Wireless Networks-on-Chip

Sergi Abadal, Ignacio Llatser, Josep Solé-Pareta, Albert Cabellos-Aparicio, Eduard Alarcón

NaNoNetworking Center in Catalunya (N3Cat)

Universitat Politècnica de Catalunya

Barcelona, Spain

{abadal,llatser,pareta,acabello}@ac.upc.edu and eduard.alarcon@upc.edu

### Abstract

A remarkably promising application of graphene is that of *Graphene-enabled Wireless Communications* (GWC) [1]. GWC advocate for the use of graphene-based plasmonic antennas – *graphennas*. A graphenna is composed of a finite-size graphene patch with a length and width between 1 and 10 micrometers mounted over a metallic flat surface (the ground plane), with a dielectric material layer in between, and an ohmic contact (see Fig. 1) [2,3]. Such disposition could be integrated with a CMOS process since graphene technology is compatible with CMOS circuitry, especially in the back-end-of-the-line, i.e. silicon CMOS chips after the completion of all silicon CMOS processes and metallization/interconnect formation.

Right at the interface between the graphene patch and the dielectric material layer, Surface Plasmon Polariton (SPP) waves are excited. SPP waves are confined EM waves that result from the coupling between surface electric charges at the interface between a metal and a dielectric, and an incident EM wave. The fundamental properties of the SPP wave depend strongly on the conductivity of the graphene layer. In particular, SPP waves on graphene have been observed at frequencies as low as in the terahertz band (0.1-10 THz) and can be tuned by material doping [3]. By exploiting the SPP waves in graphene, plasmonic antennas can be developed. The main difference between a metallic antenna and a plasmonic antenna is that the electrical length of the plasmonic antenna is much smaller than that of a metallic antenna resonating at the same frequency, due to the much lower speed of SPP waves in the plasmonic antenna compared to free-space EM waves. These unique properties of graphene allow graphennas to be much more compact than its metallic counterparts, while keeping the same radiation frequency.

Thanks to both the reduced size and unique radiation capabilities of graphennas, GWC may represent a breakthrough in the research areas of wireless off-chip communications, which consider communication among different chips in a given system, as well as wireless on-chip communications, i.e., among the different processors or cores of a Chip Multiprocessor (CMP) and of these cores with the CMP memory system. Particularly, the latter field is currently attracting the attention of the research community since the performance bottleneck in multiprocessor systems is foreseen to migrate from the computation to the communication. As the number of cores in a multiprocessor grows, inter-core and core-to-memory communication rises exponentially both in quantity and cost in terms of energy. In this context, it remains unclear whether current on-chip network alternatives will be able to provide scalable solutions for on-chip communication.

In this context, the application of graphennas and GWC to the on-chip communication scenario arises as a way to respond to this need for scalable, flexible and efficient means to interconnect the different cores of a multiprocessor. The advantages of the resulting *Graphene-enabled Wireless Networks on-Chip* (GWNoC, illustrated in Fig. 2) [5] are manifold but can be summarized in two points. On the one hand, **the potential of GWC to radiate in the terahertz band provides a huge transmission bandwidth**, allowing not only the transmission of information at extremely high speeds but also the design of ultra-low-power and low-complexity schemes. On the other hand, **the reduced size of graphennas, being commensurate with that of current and future cores, will allow the integration of one or a plurality of graphennas within the core architecture**. Such size compatibility with cores of current and future multiprocessors will allow the implementation of core-level wireless communication.

Upon these physical layer advantages, the concept of GWNoC represents a clear opportunity from the multicore architecture perspective, i.e., on how processors interact between them and with memory. Since information is radiated and can be potentially received by any receiver within the transmission range, GWNoC natively implements broadcast and multicast communications. Such approach also allows simultaneous transmissions and the creation reconfigurable communication schemes. Deployed over a state-of-the-art on-chip interconnection network [6], a GWNoC will therefore enable not just the alleviation of the latency or power bottlenecks of traditional on-chip networks, but also the devising of novel multiprocessor architectures. As a result, the cost of operations such as data coherency,

consistency or synchronization, which represent the main limiting factor in multiprocessors, could be significantly reduced and, in a few cases, eliminated [5].

In light of the potential residing within the conjunction of GWC and on-chip communication field, we are currently carrying a research project financed by the SAMSUNG Global Research Outreach program [4]. This project is mainly devoted to **1) developing a complete terahertz channel model for GWNOC**, and **2) inspecting the modulation/codification design space**. The channel model is based on Finite Element Method (FEM) simulations and we take into account the two main peculiarities of the scenario: within-package and terahertz communication. The former affects to aspects such as the static multipath effects due to the reflection of the EM waves on the different metallic surfaces, while the latter affects to important parameters such as the path loss or the ambient noise, and therefore, the communication range and the channel capacity. Investigation on modulations focuses on the design of simple, efficient and high-data rate modulations. We take into account the results given by the channel model in order to determine the need for multipath or collision-resistant schemes.

In conclusion, GWNOC will enable the future generation of computer architectures that will emerge from the cross-fertilization of the following fields (i) antennas & propagation (ii) novel nano-materials and (iii) wireless communications. By means of this convergence, computer architectures will be able to implement very high bandwidth wireless communications among the different modules and components of a computer, enabling point-to-point, broadcast, multicast and in general, all-to-all communications. To the best of our knowledge, graphene is the only material able to provide such benefits at such high-frequencies. The SAMSUNG Global Research Outreach project on GWNOC will establish the scientific and technical foundations of this new technology, pioneering this ground-breaking field both in terms of industrial and scientific impact.

## References

- [1] I. F. Akyildiz, J. M. Jornet, I. Llatser, S. Abadal, A. Cabellos-Aparicio, E. Alarcón, J. Solé-Pareta, M. C. Lemme, M. Nemirovsky, D. N. Chigrin and U. Pfeiffer, submitted to Proceedings of the IEEE (2012).
- [2] J. M. Jornet and I. F. Akyildiz, in Proc. of 4th European Conference on Antennas and Propagation (2010).
- [3] I. Llatser, C. Kremers, A. Cabellos-Aparicio, J. M. Jornet, E. Alarcón, and D. N. Chigrin, *Photonics and Nanostructures - Fundamentals and Applications*, **10** (2012), pp. 353-358.
- [4] [http://www.sait.samsung.co.kr/saithome/01\\_about/gro\\_overview.jsp](http://www.sait.samsung.co.kr/saithome/01_about/gro_overview.jsp)
- [5] S. Abadal, A. Cabellos-Aparicio, E. Alarcón, M. C. Lemme and M. Nemirovsky, accepted for publication in *IEEE Communications Magazine* (2012).
- [6] S. Abadal, A. Cabellos-Aparicio, J. A. Lázaro, E. Alarcón and J. Solé-Pareta, in Proc. of the International Conference in Transparent Optical Networks (2012).

## Figures

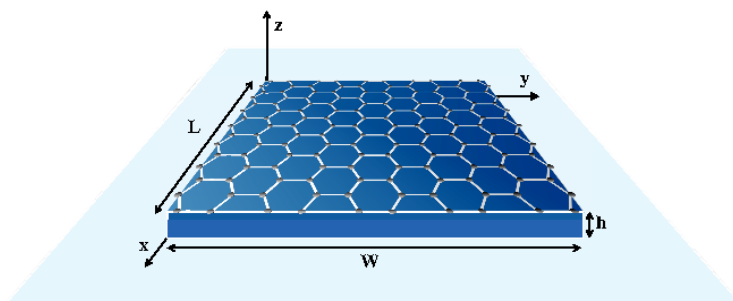


Fig. 1. Conceptual diagram of a graphene-based plasmonic nano-patch antenna (graphenna).

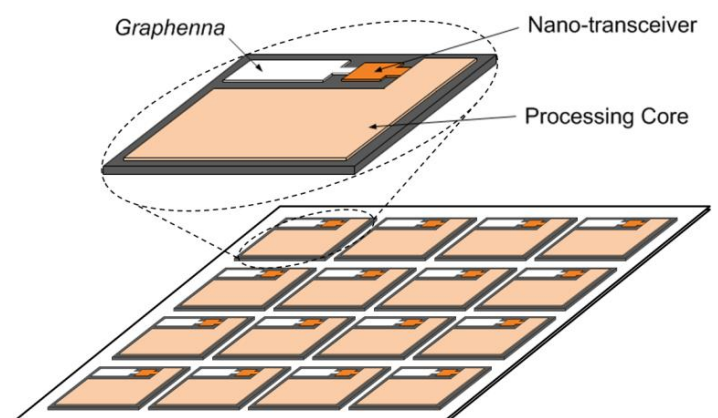


Fig. 2. Schematic representation of a 16-core Graphene-enabled Wireless Network-on-Chip (GWNOC).