Single dopant and single electron effects in CMOS devices

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For the first time a state-of-the-art CMOS foundry (CEA-LETI-MINATEC) has been used to design silicon nanostructures with single or multiple gates dedicated to the study of single electron effects. The nanofabrication uses two e-beam lithography steps to define an active region formed by silicon-on-insulator (SOI) nanowires of cross section down to 20 nm×10 nm and polysilicon gates of lengths down to 20 nm. The pitch at the gate level (distance between centers of the successive gates) is as small as 70 nm. Several technological splits (SOI thickness, channel doping, LDD doping, nitride spacer's length, trimming of active layer) have been made to compare devices differing only by one crucial parameter. Several dozen of designs have been introduced in the e-beam database to analyse the impact of key geometrical parameters. As a whole few 10,000 samples have been fabricated and several hundreds of them have been studied electrically, mostly at low temperature. Some of them are described in this contribution which focuses i) on ultra scaled Ultra-thin SOI nanowire MOSFET ii) on controlled MOS-SET.

Single dopant effects in UT SOI MOSFET [1, 6]

We have fabricated nanoscale n-type SOI MOSFET with an effective gate length down to 10 nm (see figure 1, right panel). For that dimension current below the threshold can be dominated by transport through a single isolated dopant orbital, which has diffused from source and drain [1]. In that case we show that up to room temperature transport below the threshold is dominated by thermally broadened resonant tunneling via this single dopant coupled to a source and a drain.
We show that the ionization of such a single isolated dopant is strongly affected by its dielectric environment [6], namely the proximity of the BOX of our SOI wafer. This "so-called dielectric confinement" effect was predicted a few years ago [4] and can be a source of large dispersion of dopants ionization energies. This dispersion induces a large sub-threshold variability for ultra scaled FETs. Performing low temperature transport spectroscopy, we are able to detect the filling of the first dopant (see figure 1, left panel). The gate voltage where this occurs is a direct measure of the ionization energy of this dopant. Compared to the bulk case (54meV) we find a strongly enhanced value (up to 108 meV) for a dopant close to the buried oxide. By applying a substrate bias we have a new way to control the sub-threshold SD tunnelling rates thru this buried donor.

Controlled MOS-SETs [2, 3]

By using self aligned spacers and a so-called underlap Source-Gate geometry it is possible to fabricate controlled MOS-SET [2]. We have extended this well controlled technique to fabricate two dots in series are created below two top gates overlapping a silicon nanowire (see figure 2, right panel). The coupling between dots is controlled by gate voltages.

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Figures

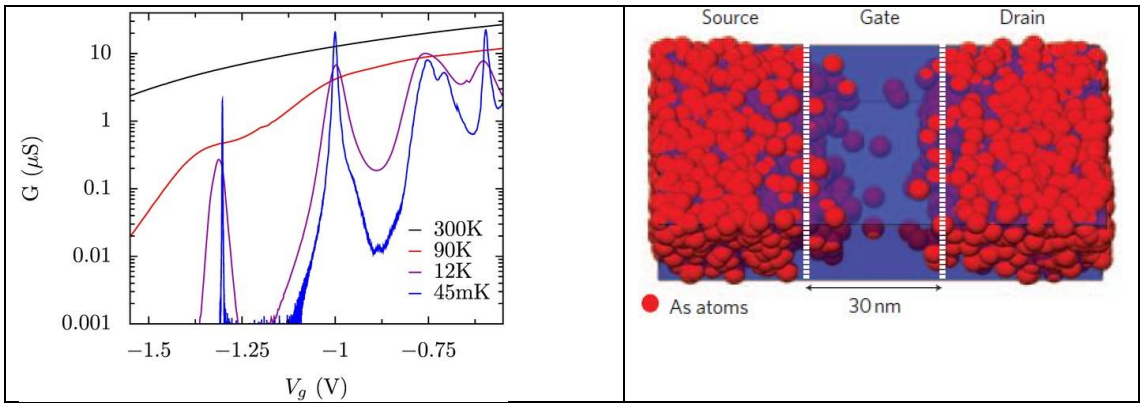

Figure 1
Left panel: Source –drain conductance versus gate voltage for a L*W*Ts_i = 10*50*20 nm^3 at different temperature. The first sharp resonance around Vg = -1.27 V is due to resonant tunnelling through the As+ ➔ As0 transition when the electronic ground state of the first As donor is aligned with the Fermi level in the source (and drain). The associated ionization energy is 108 meV. The resonating donor is centred in the channel but close to the BOX. The second resonance near Vg=-1.0 V is due to a second distinct As donor. The associated ionization energy is 50 meV. The donor is centred in the channel but closer to the gate. The third resonance is due to the double occupation of the second donor, as explained in ref. [1]. Resonance at larger gate voltage are close or above to the threshold voltage which is -0.5V.
Right panel: Process simulation of a typical random arrangement of the As donors in the studied device.

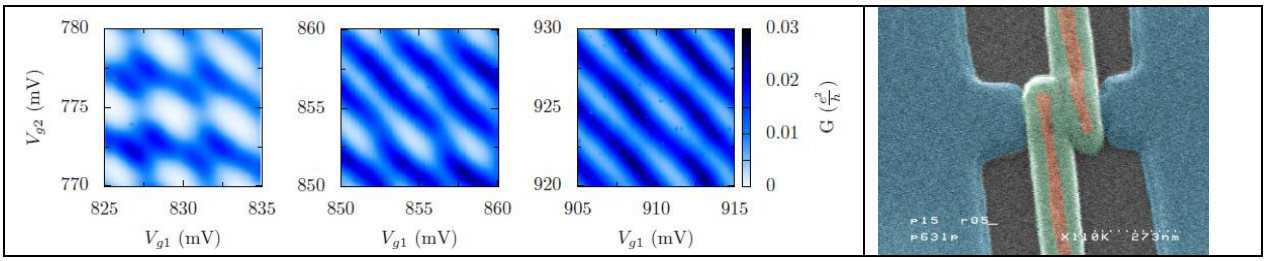

Figure 2
Left panel: The source-drain conductance in quantum units as function of the two gate voltages. The data are recorded at T=1K. For this sample the gate length is 60nm, the spacing between gates is 40nm and the nitride spacers are 40 nm thick. The SOI cross section is 20nm×60nm. At low gate voltage (left panel) the two MOS-SET below the gates are capacitively coupled. The pattern exhibits a typical honeycomb structure. At large gate voltage (right panel) the two MOS-SETs are tunnel coupled by the accumulation channel created in the central region: the two MOS-SETs merge as a single island and an anti diagonal pattern appears. The central panel describes an intermediate situation (from ref. [3]).
Right panel: coloured SEM view of the sample (SOI in blue, PolySiGate in red and SiN spacers in green).