Wafer scale fabrication of passivated carbon nanotube transistors for electrochemical sensing

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Since the operation of carbon nanotube transistors (CNT-FETs) was demonstrated [1], much progress has been achieved on the knowledge about electronic transport on SWCNTs and on their application for sensing [3]. However, there is still no standard high yield technology to fabricate single CNT-FETs.

In this contribution we present a technological process for the batch fabrication of CNT-FET based chips for electrochemical sensing applications (Figure 1) [2]. The fabrication of the CNT-FET structures is performed by using standard microelectronic steps at wafer level. Optical lithography is the only patterning technique to be used. The overall process can be divided in three main steps: the substrate preparation, the selective synthesis of the single-walled (SW) CNTs and the definition of the metallic contacts, stripes and pads. Recently, we have reported the fabrication of 10,000 functional CNT-FET devices on a 4 inch wafer by this technology [4].

An important requirement for the operation of the CNT-FETs in an electrochemical environment is the electrical contacts to be isolated from the electrochemical solution. With this purpose, we have developed a passivation procedure consisting in a PMMA coating of the CNT-FET and an electron beam lithography (EBL) process to locally remove the PMMA from the top of the CNTs and from the liquid polarization electrodes. The EBL process is programmed for the pattern to be automatically aligned on each device and it is performed at low electron beam energy to avoid any damage to the devices [5].

Figure 2(a-c) shows results on the fabrication of the CNT-FET based sensors. Figure 2(a) shows a 4 inch wafer after the fabrication of the CNT-FET structures. The wafer contains 5,616 CNT-FET structures. Almost 30% of the devices on this wafer were identified as operative and one third of those devices showed a semiconducting characteristic. Figure 2(b) shows an optical image of a sensor-platform into which the CNT-FET structures on the wafer are arranged. Each sensor-platform is composed of 24 CNT-FET structures that are located at the center of the chip for an electrochemical cell to be installed. The SEM image in Figure 2(c) shows a CNT-FET structure which channel length is 1.5 μm and where the width of the trench in the PMMA is 800 nm. Two SWCNTs had been contacted in this case by the metal contacts. The typical IV characteristics of a functional CNT-FET are shown in Figure 2(d). The transistors are p-type, their ON current is ~1 μA and the I_{ON}/I_{OFF} ratio is ~10^5.

The passivated CNT-FET devices are currently being tested in electrochemical environment.

Acknowledgements

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Figures

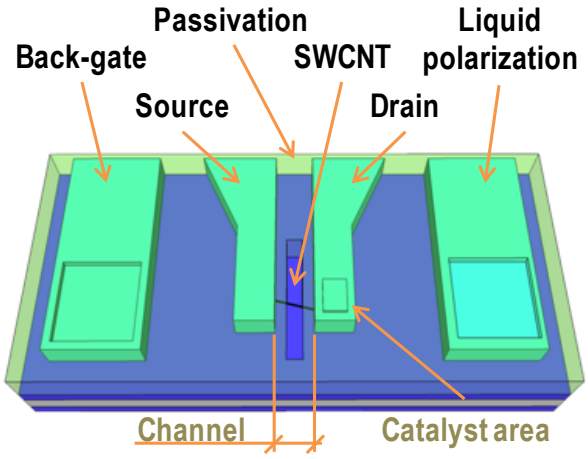

Figure 1: Schematic of the passivated, back-gated CNT-FET sensor. The sensor consists of one (or more than one) SWCNT that is contacted by two metal electrodes, a back-gate that is actuated through a top metal electrode and a top liquid polarization electrode. The sensor is completely passivated by PMMA except for the channel of the CNT-FET, for part of the liquid polarization electrode and for the contact pads.

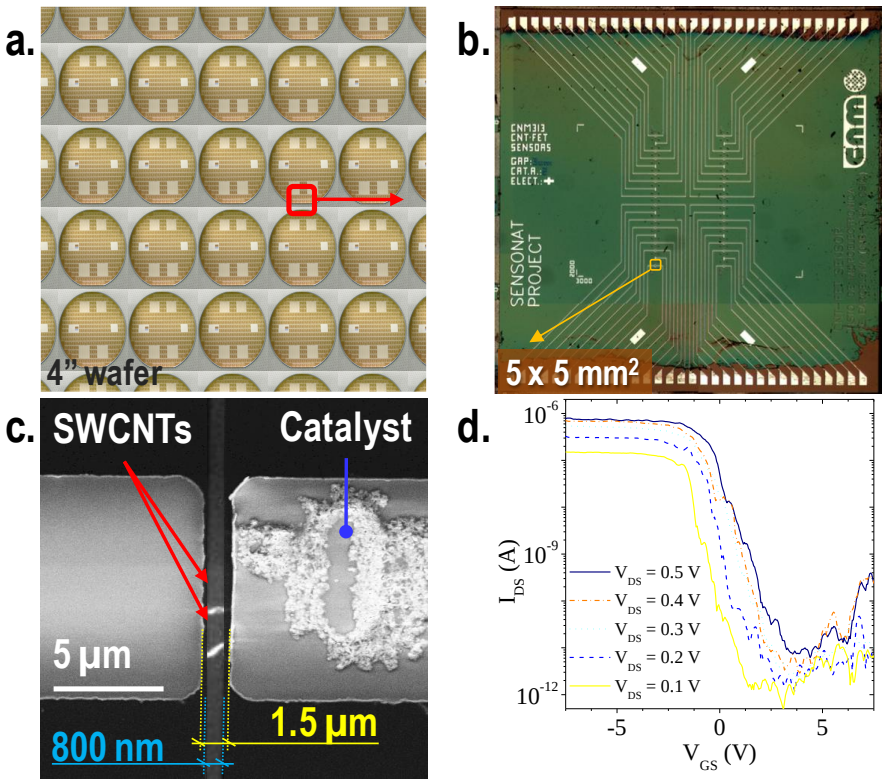

Figure 2: Images on the fabrication and IV characteristics of the CNT-FETs. (a) Photograph of a batch fabricated 4 inch wafer. (b) Optical image of a sensor chip after the passivation procedure. The sensor is 5 x 5 mm^2. (c) SEM image of a passivated CNT-FET device. (d) Typical I_{DS} vs. V_{GS} characteristics of a CNT-FET formed of a single semiconducting SWCNT.