Impact of the polycrystallization of high-k dielectrics on the nanoscale and device level electrical properties of MOS capacitors

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High-k dielectrics have been introduced in MOS devices to reduce gate leakage currents [1]. However, their crystallization [2] can affect the electrical properties and reliability of scaled devices [3]. In this work, a Conductive Atomic Force Microscope (CAFM) [4-5] has been combined with standard electrical characterization techniques at wafer level to investigate how the polycrystallization of a high-k layer affects its nanoscale morphological and electrical properties [6] and how such nanoscale properties affect the electrical characteristics of fully processed devices.

When CAFM works on bare (dielectric) surfaces, the conductive tip of the microscope plays the role of the metal gate of a MOS capacitor with an area that is the contact area between the tip and the sample (~100 nm^2), so that a nanometer resolution can be achieved. Using this technique, the impact of the polycrystallization after thermal annealing on the nanoscale properties of high-k dielectrics was studied, first, on 5nm thick polycrystalline HfO_2 films. Fig. 1 shows a (a) topographical and (b) current image obtained with the CAFM at 6.5V. Note that a granular structure can be distinguished in (a), which has been attributed to the polycrystallization of the high-k layer: grains in the image correspond to individual randomly oriented nanocrystals separated by grain boundaries (GBs, depressions in the image). The high-k polycrystallization effect on its electrical properties was investigated from the current image (Fig.1.b). In this image, brighter areas correspond to larger currents. A granular current pattern which overlaps with that of the topographical image is observed: leaky sites and breakdown spots are mainly located at GBs. Therefore, these results show that polycrystallization of the HfO_2 layer affects, not only the morphological, but also the electrical properties of the gate stack, increasing the leakage current and the inhomogeneity of its conductivity. Amorphous layers do not show any pattern, neither on topography nor on current, which suggests larger nanoscale homogeneity of the film.

The impact of the nanoscale device inhomogeneities on the global electrical characteristics of MOS devices has been analyzed from I-V characteristics measured on fully processed MOS devices (i.e., with metal gate electrode). Fig. 2 shows I-V curves obtained on MOS capacitors based on an amorphous (squares) and polycrystalline (triangles) 3nm thick HfO_2 layer as gate dielectric. The I-V curve in circles corresponds to a typical post-BD characteristic. Note that two clear different behaviours can be identified. In the amorphous structures (squares), before BD, the I-V curves follow a Fowler-Norheim behaviour with a very small dispersion between samples. However, in polycrystalline samples (triangles), at low fields, the gate conduction is larger than in amorphous gate dielectrics, with a very erratic and non-stable behaviour, suggesting different conduction modes, which can change from sample to sample. At high fields, current increases even more, showing the typical post-BD behaviour. The higher pre-BD currents observed in polycrystalline gate stacks could be related to the gate current that flows through the GBs, which have been shown to be more conductive (Fig. 1).

The impact of an electrical stress on the electrical conduction and charge trapping of amorphous and polycrystalline 10 nm Al_2O_3 layers has been also investigated from the measurement of sequences of current images on the same area. Figure 3 shows sequences of three images measured on the amorphous (a-c) and polycrystalline (d-f) Al_2O_3 layer. First a 500x500nm^2 area (a and d) was scanned by applying a large enough constant voltage to induce degradation. Afterwards two zooms out were done, and larger areas which include the previously scanned smaller regions where imaged. A quantitative analysis of Fig. 3 demonstrates that, although crystals (in polycrystalline structures) are more resistive and less weak (from an electrical point of view) than amorphous oxides, the GBs in the polycrystalline samples seem to be more sensitive to an electrical stress than non-crystallized structures: GBs would favor a faster generation of defects leading to charge trapping. These results suggest that the presence of GBs in polycrystalline structures strongly contributes to the inhomogeneity increase of the conduction and trapping properties of the stacks.

To conclude, the results show that polycrystallization of high-k dielectrics affects the homogeneity of their nanoscale properties (surface morphology and conductivity), which has a clear impact on the global electrical properties of MOS devices, since a larger sample-to-sample variability is measured.

Moreover, the presence of grain boundaries on polycrystalline dielectrics could also reduce significantly the reliability of MOS devices due to their lower robustness.

References

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Figures

Fig. 1

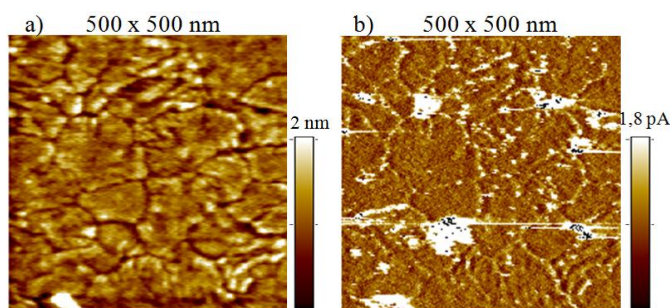

Fig. 2

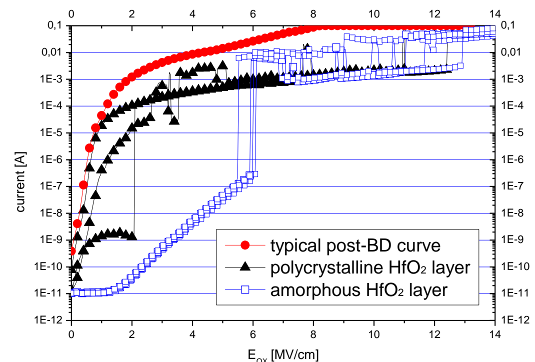

Fig. 3

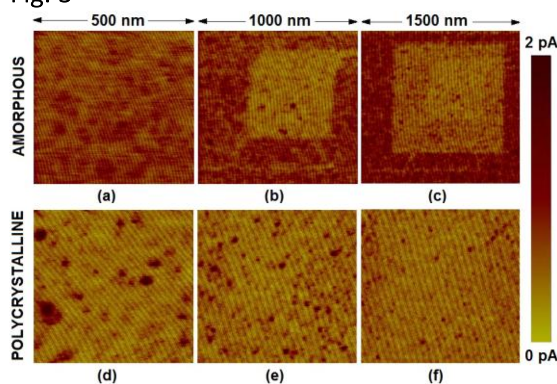

Figure caption

Fig.1. (a) Topographical and (b) current images obtained at 6.5V in a polycrystalline HfO_2 layer (5nm thick). In (a), depressions can be related to grain boundaries between nanocrystals. In (b), brighter areas are concentrated at grain boundaries.

Fig.2. Sets of IV curves obtained at device level on MOS capacitors (area 3µm x 3µm) based on HfO_2 as gate dielectric. Squares/triangles were obtained on fresh structures with an amorphous/polycrystalline HfO_2 layer. Circles correspond to a typical post-BD I-V curve, as reference.

Fig.3. First scans (a and d) and two consecutive zooms out (b/e and c/f) obtained on an amorphous (a, b and c) and polycrystalline (d, e and f) Al_2O_3 layer. Their sizes are (a and d) 500 nm x 500 nm, (b and e) 1µm x 1µm and (c and f) 1,5 µm x 1,5 µm. The applied voltage was 11.5 V in all cases.