ELECRTICAL COMPACT MODELLING OF GRAPHENE TRANSISTORS

Sébastien Frégonèse[1], Huu-Nha Nguyen[1], Cristell Maneux[1], Henri Happy[2], Nan Meng[2], Thomas Zimmer[1]

[1]CNRS, UMR 5218, Laboratoire IMS, Université de Bordeaux, France
[2]IEMN – CNRS 8520, Avenue Poincare, 59652 Villeneuve d'ASCQ Cedex, France
sebastien.fregonese@ims-bordeaux.fr

The discovery of single layer graphene has generated much theoretical and experimental interest because of its exceptional properties [1], [2]. The gapless bandstructure in graphene results in good transport properties of carriers such as high mobility and high Fermi velocity. These physical properties are of great interest for electronic application using graphene transistors (GFET and GNRFET). Also, the evaluation of such devices for circuit applications can be performed through appropriate electrical compact models. Moreover, during the graphene synthesis, defects may be created in the graphene sheet which induce trap charges in the channel [3, 7]. This effect must be taken into account for accurate compact modelling. Hence, in this paper we propose a modification of the drift-diffusion compact model for graphene FET devices from Meric et al. [5].

In order to model the drift-diffusive transport, we use the velocity saturation model [4], [5]. The models will be applied to the 2D system of graphene. In the channel, the carrier concentration is calculated using the model in [5, 6]: $n = \sqrt{n_0^2 + \left[C_{top}\left(V_{GS} - V_{DIRAC}^0\right)/e \right]^2}$, V^0_{DIRAC} is the top gate-source voltage at the Dirac point in these regions and n_0 is the minimum 2D carrier concentration which contains the effect of disorder and thermal excitation. The current in the channel is given by $I_d = \frac{W}{L}\int_0^L e.n(x).v_{drift}(x)dx$, where x is the distance along the channel, L and W are the length and the width of the channel. We approximate the carrier drift velocity v_{drift} by a velocity saturation model [6]: $v_{drift}(x) = \frac{\mu E}{1+\mu E / v_{sat}}$, where the saturated velocity depends on the carrier concentration as $v_{sat} = v_F\left(\hbar\Omega / E_F\right)$ where v_F and E_F is the Fermi velocity and Fermi energy, $\hbar\Omega$ is the surface phonon energy of the substrate.

The GNRFET has been fabricated and characterized by the IEMN laboratory [7, 8]. The transistor is composed of parallel graphene ribbons playing the role of the channel, with a gate length of 150 nm (fig 1). The width of the ribbons is about 50 nm, which is quite large so that the induced band gap may be negligible and the 2D model is applied to model the transistor transport. Its intrinsic cut-off frequency is about 10 GHz. The figure 2 shows I_{DS} versus V_{DS} characteristics for measurement and compact model simulation. A good agreement is observed in DC but doesn't match in AC regime. However, from the measurement, we can observe a strong difference between the transconductance g_M (calculated from measured DC $I_D(V_{GS})$ characteristic) and measured real part of Y_{21} (calculated from measured S-parameters)at medium frequency (10 MHz < f <10 GHz), (see Fig. 3, 4 and 5). We explain this effect by the presence of traps which are active during DC measurement and which are cancelled during the AC ones. To take into account the presence of trap charges in the channel, we modify the formula for the carrier concentration by replacing n_0 (AC regime) by $n_0+n_{traps}*H(f)$ (DC regime). H(f) is a low frequency band pass filter. Trapped charges are active only in DC regime and at low to moderate frequency. Trapped charges are cancelled in AC regime and modify the Dirac point position. Hence, we modify the V^0_{DIRAC} parameter in order to introduce charge dependence. The change in Dirac point voltage is

expressed as: $\Delta V_{DIRAC} = V_{DIRAC}^{traps} - V_{DIRAC}^{AC} = \sqrt{\left[e^2 \left({n_{0AC}}^2 - \left(n_{0AC} + n_{TRAPS} \right)^2 \right) / {C_{top}}^2 \right] + {V_{DIRAC}^{AC}}^2} - V_{DIRAC}^{AC}$.

This modification of the compact model improves strongly the accuracy of the model as shown on fig. 4 where the compact model is in agreement with both the transconductance and Y_{21} parameter.

References

[1] Novoselov, K.S., et al., Science, 306 (2004): p. 666-669.

[2] Geim, A.K. and K.S. Novoselov, Nat Mater, 6 (2007): p. 183-191.

[3] Zhu, J., R. Jhaveri, and J.C.S. Woo, Applied Physics Letters, 96 (2010): p. 193503-3

[4] Canali, C.M., G. Minder, R. Ottaviani, G., IEEE Transactions on Electron Devices 22 (1997): p. 1045-1047.

[5] Meric, I., et al., Nat Nano 3 (2008): p. 654-659.

[6] J. L. Xia et al. Applied Physics Letters 96, 162101, 2010.

[7] N. Meng et al, Device Research Conference (DRC), 2010

[8] Meng, N. et al., EuMIC 2010 - Conference Proceedings , art. no. 5613734, pp. 294-297

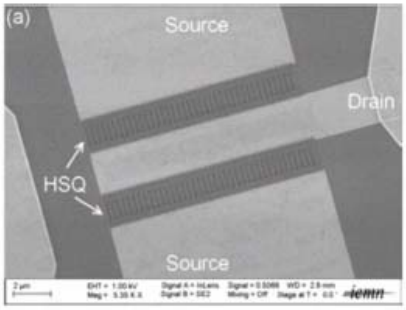

Figure 1. Top gated graphene FET for measurement by the IEMN group.

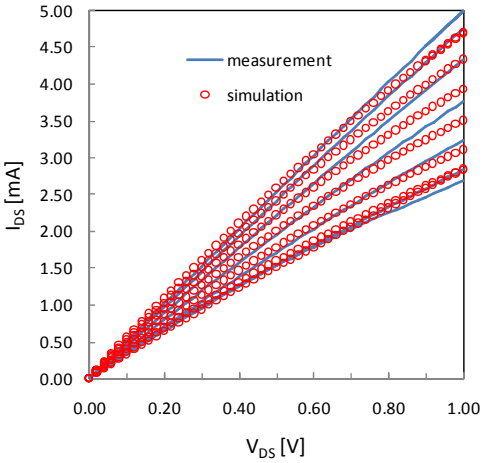

Figure 2. I_{DS}-V_{DS} characteristics for V_{GS} = -2 to 1 V (upwards) with the step = 0.5 V. The simulated results are blue lines, the measured ones are red circles

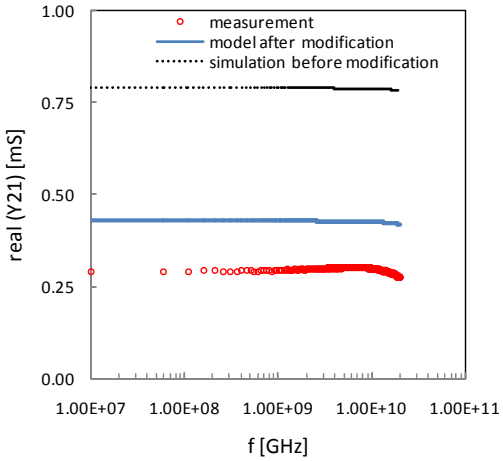

Figure 3. real part of Y_{21} parameter versus frequency for V_{GS} =-0.8V for V_{DS} =1 V.

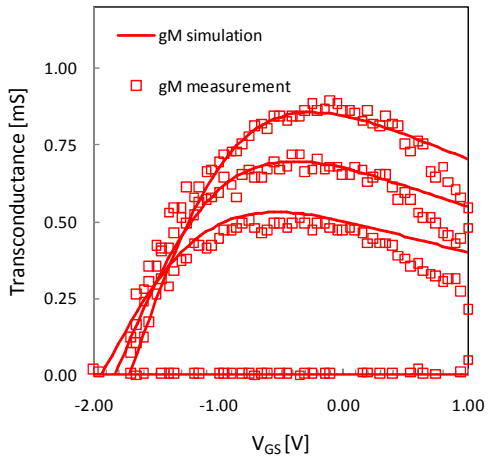

Figure 4. Transconductance g_M as a function of V_{GS} for V_{DS} = 0.6, 0.8, and 1 V.

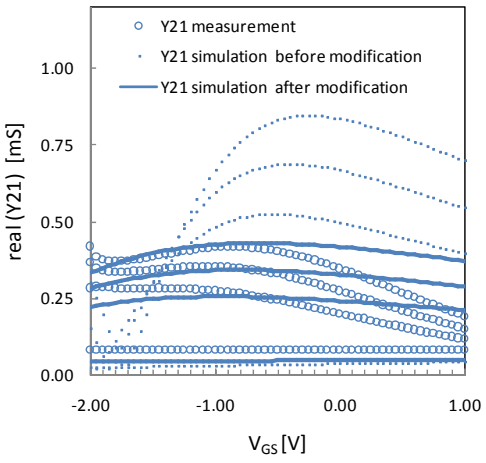

Figure 5. real part of Y_{21} parameter at 3GHz as a function of V_{GS} for V_{DS} = 0.6, 0.8, and 1 V.