Large Scale CVD Graphene Nanoribbon Transistors with High-κ Dielectrics and Top Gates

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Graphene nanoribbon field-effect transistors (GNRFETs) are promising candidates for nanoelectronic applications. Researchers have demonstrated that one-of-a-kind GNRFETs can have mobility values >1,000 $cm^2V^{-1}s^{-1}$ [1] and I_{on}/I_{off} ratios ~10^6 [2]. However, such one-of-a-kind GNRFETs use chemically derived or mechanically exfoliated graphene, neither of which are practical for large scale fabrication. On the other hand, synthesis of graphene by chemical vapor deposition (CVD) is a promising method [3] for creating wafer-scale transistors and circuits.

In this study we use a novel fabrication technique to demonstrate the first large scale arrays of top-gated GNRFETs using CVD graphene. This approach can be used to fabricate thousands of GNRFETs on a single test chip, enabling systematic and statistical characterization of device performance as a function of device dimension, material, and temperature. This method also paves the way toward realistic GNRFET-based circuits.

Our CVD graphene growth and transfer process is illustrated in Fig. 1. CVD growth on copper foil results in monolayer growth (Fig. 2) on both sides of the Cu foil [3]. After growth, one side of the foil is protected with poly-methyl methacrylate (PMMA), while the other side is exposed to an O_2 RIE plasma etch to remove the additional graphene film. The Cu foil is removed using $FeCl_3$ and the PMMA/graphene film is transferred to a deionized (DI) water bath. After rinsing, the film is transferred to SiO_2 (90 nm) on highly doped Si wafers. When the sample is dry, PMMA is removed using a 1:1 methylene chloride to methanol solution.

Figure 3 depicts our top-gated GNRFET fabrication process. Electron-beam evaporation is used to deposit source and drain Ti/Au (1 nm/50 nm) contacts. We introduce a novel technique for defining the nanoribbon while simultaneously providing a sticking layer for the high-κ dielectric. The narrow GNR channel is first patterned between the source and drain, and then 2 nm of Al is deposited. The sample is removed from vacuum, immediately oxidizing the thin layer of Al [4]. After PMMA liftoff, the 2 nm AlO_x film covering the GNR channel is used as an O_2 RIE plasma etch mask. Etching removes all exposed graphene, defining a nanoribbon between source and drain while electrically isolating all devices on the chip. The nanoribbon is completely covered with AlO_x, enabling the high-quality atomic layer deposition (ALD) of either Al_2O_3 or HfO_2 [4,5]. In this work we deposited 12 nm of Al_2O_3 over the surface of the sample after the O_2 etch. The top gate is patterned and Ti/Au (1 nm/50 nm) is evaporated onto the high-κ dielectric. We anneal the samples in vacuum at 200 ºC overnight, reducing contact resistance up to 25%.

We used relatively conservative dimensions in our initial proof-of-concept experiments. Nanoribbons were W = 50 nm wide, with channel lengths from L = 350-500 nm (Fig. 4). The top gate was kept narrow (L_G = 100 nm) to prevent overlap with source or drain from misalignment. Measurements were taken in vacuum (Fig. 5) and ambient (Fig. 6) at room temperature. Device yield was a respectable 63%, even for the initial fabrication runs, highlighting the large-scale utility of the novel GNR patterning approach. Extracted mobility values were μ_{GNR} ~ 100-200 $cm^2V^{-1}s^{-1}$ across all samples, typical of narrow GNRs where edge scattering dominates [2]. It is important to point out that CVD-grown GNRs had not been evaluated before, but the mobilities estimated here are similar to GNRs obtained from exfoliated graphene. This may indicate that our GNRs are smaller than the CVD graphene grain size, and thus edge scattering dominates. Future work must better characterize such issues, improve the parasitics of these devices, and decrease their dimensions.

In summary, we have demonstrated (to our knowledge) the first large-scale CVD-graphene nanoribbon transistors with top gates and high-k dielectrics. We have also introduced a novel technique for defining the nanoribbon while simultaneously seeding the high-k dielectric. Combined, these approaches pave the way toward systematic and statistical characterization of GNRFETs, and toward the implementation of realistic GNRFET-based circuits.

References

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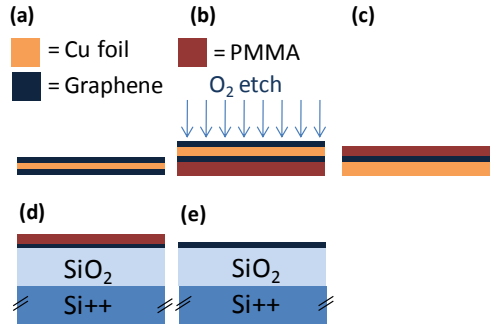


Fig. 1. *(A) Monolayer CVD grown graphene on both sides of a Cu foil. (B) PMMA is used to protect graphene on one side of the foil while the other is removed by O_2 etching. (C) PMMA and graphene on Cu foil before $FeCl_3$ etching. (D) PMMA/graphene film transferred to 90 nm SiO_2 on heavily doped Si. The substrate is used as the back gate in electrical measurements. (E) PMMA liftoff completes the CVD growth and transfer process.*

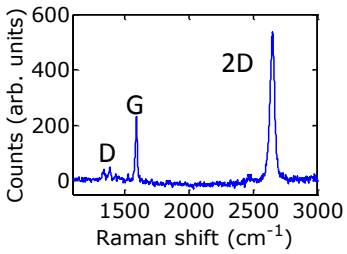


Fig 2. *Raman spectra of the monolayer graphene used in this experiment. The graphene has a 2D:G ratio of ~2.*

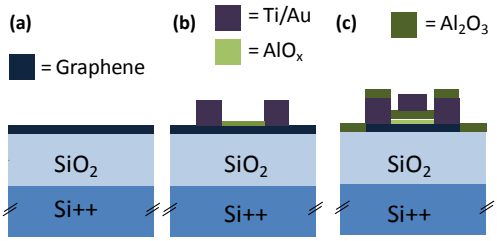


Fig. 3. *(A) Large scale GNRFET fabrication commences with CVD graphene transferred to an SiO_2/Si++ substrate. (B) E-beam evaporation is used to deposit Ti/Au (1 nm/50 nm) contacts. Al (2 nm) is deposited between source and drain to serve as an etch mask for defining the GNR and as a nucleation layer for high-κ oxide deposition. The Al instantly oxides into AlO_x upon removal from vacuum. (C) An O_2 plasma etch defines the GNR and electrically isolates GNRFETs from each other. Al_2O_3 (12 nm) is grown by ALD. A Ti/Au (1 nm/50 nm) top gate completes the large scale CVD GNRFET fabrication process.*

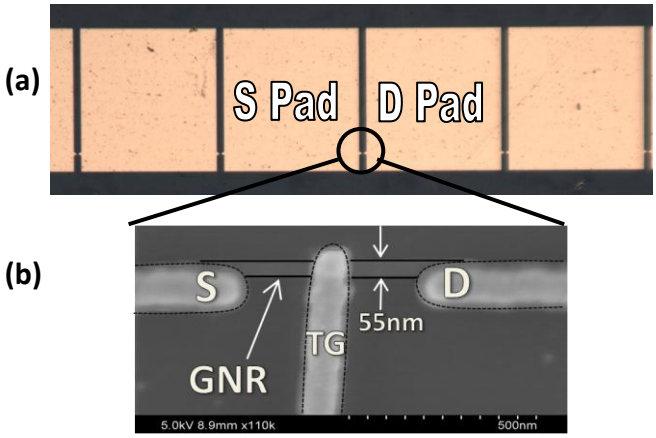
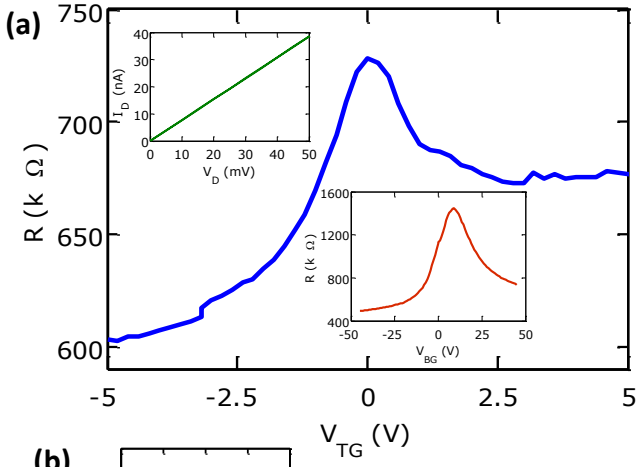


Fig. 4. *(A) A row of GNRFETs (B) An SEM image of a top-gated high-κ GNRFET on CVD graphene with channel W=55 nm L=450 nm and top gate W=100 nm.*



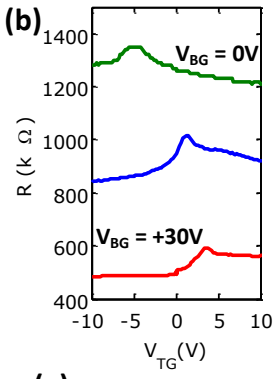


Fig. 5. *(A) Room temperature measurements for a GNRFET in vacuum with W = 50 nm, L = 500 nm. (B) TG modulation for the same device with V_{BG} = 0 V (top) to V_{BG} = +30 V (bottom).*

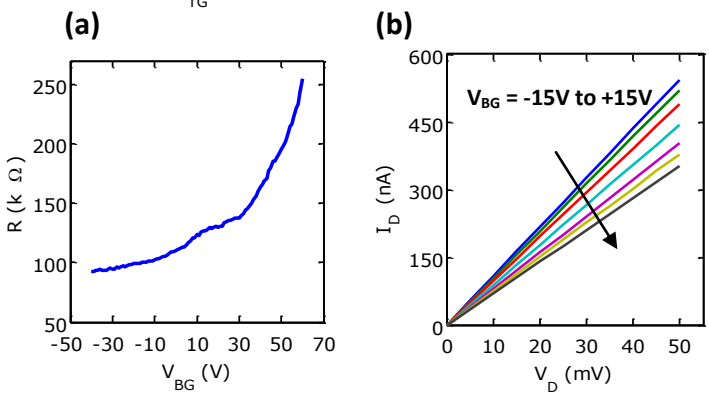


Fig. 6. *(A) Room temperature, ambient R-V_{BG} of a W = 50 nm, L = 400 nm device. (B) Id-Vd for the same device.*