Analytic drain-current model of Graphene Field-Effect Transistors targeting analog/radiofrequency applications

David Jiménez, Oana Moldovan

Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona, Spain

david.jimenez@uab.es

Graphene has emerged as a candidate material for future nanoelectronic devices. Aside the impressive mechanical properties, graphene exhibits very high mobility (~10⁵ cm²/V-s) and saturation velocity (~10⁸ cm/s), together with a promising ability to scale to short gate lengths and high speeds by virtue of its thinness. The main problem is the absence of a gap, therefore limiting the usefulness of graphene in digital applications. Several approaches have appeared in the last years to open a gap. For instance, graphene nanoribbons providing quantum confinement, bilayer graphene, or strained graphene have been suggested. However, zero gap graphene could still be very useful in analog and radiofrequency (RF) applications where high ON/OFF current ratios are not required [1]. For instance, for small signal amplifiers, the transistor is operated in the ON-state and small RF signals that are to be amplified are superimposed onto the DC gate-source voltage. Instead, what is needed to push the limits of analog/RF performance is an operation region where high transconductance together with a small output conductance is accomplished. This situation is realized for state-of-the-art graphene field-effect transistors (GFETs). Specifically, for large-area GFETs, the output characteristic shows a weak saturation that could be exploited for analog/RF applications. Recently, cutoff frequencies in the range of hundreds GHz [2] have been demonstrated and operation in the THz range is envisioned.

At this stage of development of GFET technology, modeling is a key aspect for device design optimization, projection of performance, and exploration of circuit designs providing new functionalities. We have done this modeling effort in the framework of the drift-difussion theory. This theory has proved to be successful in explaining the electrical behavior of GFETS [3,4]. In this work we present a fully analytic physics-based electrical model of the useful for analog/RF research community. Explicit close-form expressions for the drain current have been derived and benchmarked with experimental results [5].

References

- [1] F. Schwierz, Nature Nanotechnology, 5 (2010) 487.
- [2] Y.-M. Lin et al., Science, **327** (2010) 662.
- [3] I. Meric et al., Nature Nanotechnology, 3 (2008) 654.
- [4] S. Thiele et al., Journal of Applied Physics, 107 (2010) 094505
- [5] Kedzierski et al., IEEE Electron Device Lett., **30** 745 (2009).

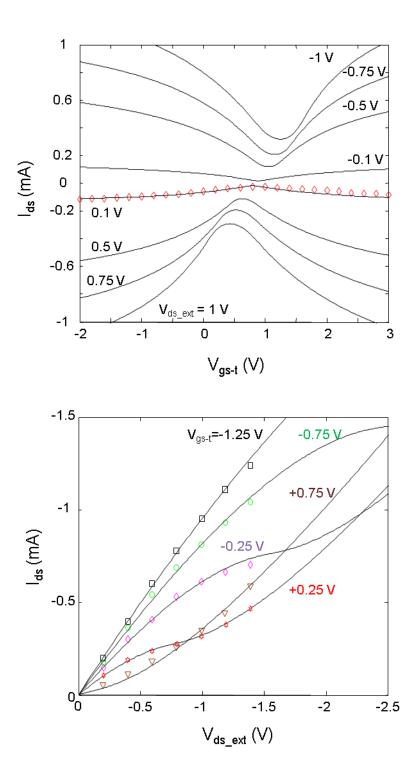


Figure 1. Transfer and output characteristics of a prototype GFET as computed with the analytical model benchmarked with experimental results reported by Kedzierski et al., IEEE Electron Device Lett. 30, 745 (2009). The device under test is a top-gate GFET with channel length of 10 μ m, gate width of 5 μ m, top dielectric is hafnium oxide with thickness of 40 nm and permittivity ~ 16. The flat-band voltage was tuned to 0.85 V according to the location of Dirac point from the transfer characteristics. A low-field mobility of 7500 cm²/V-s for both electrons and holes, source/drain resistances of 300 Ω , and phonon effective energy ~ 100 meV was considered. These values are consistent with the extracted values from measurements. As input parameter a sheet carrier density =3.10¹¹ cm⁻² was used for the final fine tuning. Symbols: experimental results. Solid line: model results.