NANOMAGNETIC STRUCTURES FOR METALLIC SPINTRONICS

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As CMOS matures, there is growing interest in exploring alternative paradigms for digital information storage and processing. This is particularly true of new technologies which are capable of being integrated onto CMOS platforms to form a System on Chip hybrid.

The emerging field of spintronics, in which the spin of the electron is used in addition to its charge, provides a number of potential candidates. Spintronics has been considered from two different perspectives. In the first ('semiconductor spintronics'), spin polarized electrons are injected into a semiconductor and manipulated using transistor-like structures. In the second ('metallic spintronics'), ferromagnetic metals are integrated onto a CMOS platform using a Back-End-Of-Line process and magnetization is probed using one of the magneto-resistive effects.

To date, most of the work in metallic spintronics has concerned non-volatile magnetic random access memory (MRAM), in which the ferromagnetic magnetization direction is used to represent the Boolean states 0 and 1 for the memory. Electronics, however, is a combination of memory and logic. The work described in this talk attempts to address the question: can ferromagnetic nanostructures be used to perform Boolean logic operations as well as simply to store information?

In this talk I describe domain wall logic, in which information is carried and processed on a network of interconnected ferromagnetic nanowires. Nanowire junctions which perform the logical NOT [1], AND / OR functions [2] as well as signal routing functions such as domain wall diodes [3] have all been demonstrated experimentally, as have structures which allow signals to cross-over in the same plane and to fan out into multiple identical copies. In this talk, I show a number of working nanocircuits comprising interconnected magnetic nanowires fabricated by focused ion beam milling from a thin permalloy ($Ni_{80}Fe_{20}$) film (Fig. 1). The advantages of domain wall logic are numerous and include: non-volatility and radiation hardness; the potential for low fabrication cost; the potential for fabrication on mechanically flexible substrates; the potential for fabrication in 3-dimensions to form a high density neural-like device; very low delay-power products; good scalability to smaller design rules; a large amount of implicit distributed memory, allowing novel architectures to be realized. The disadvantages of domain wall logic are essentially a limited operation speed determined by the speed of propagation of domain walls and the need to generate a rotating magnetic field in order to power the devices.

References:

[1] D.A.Allwood et al., Science **296**, 2003 (2002)
[2] Faulkner et al. IEEE Trans. Mag. **39**, 2860 (2003)
[3] D.A. Allwood et al., Appl. Phys. Lett. **85**, 2848 (2004)

Figures:

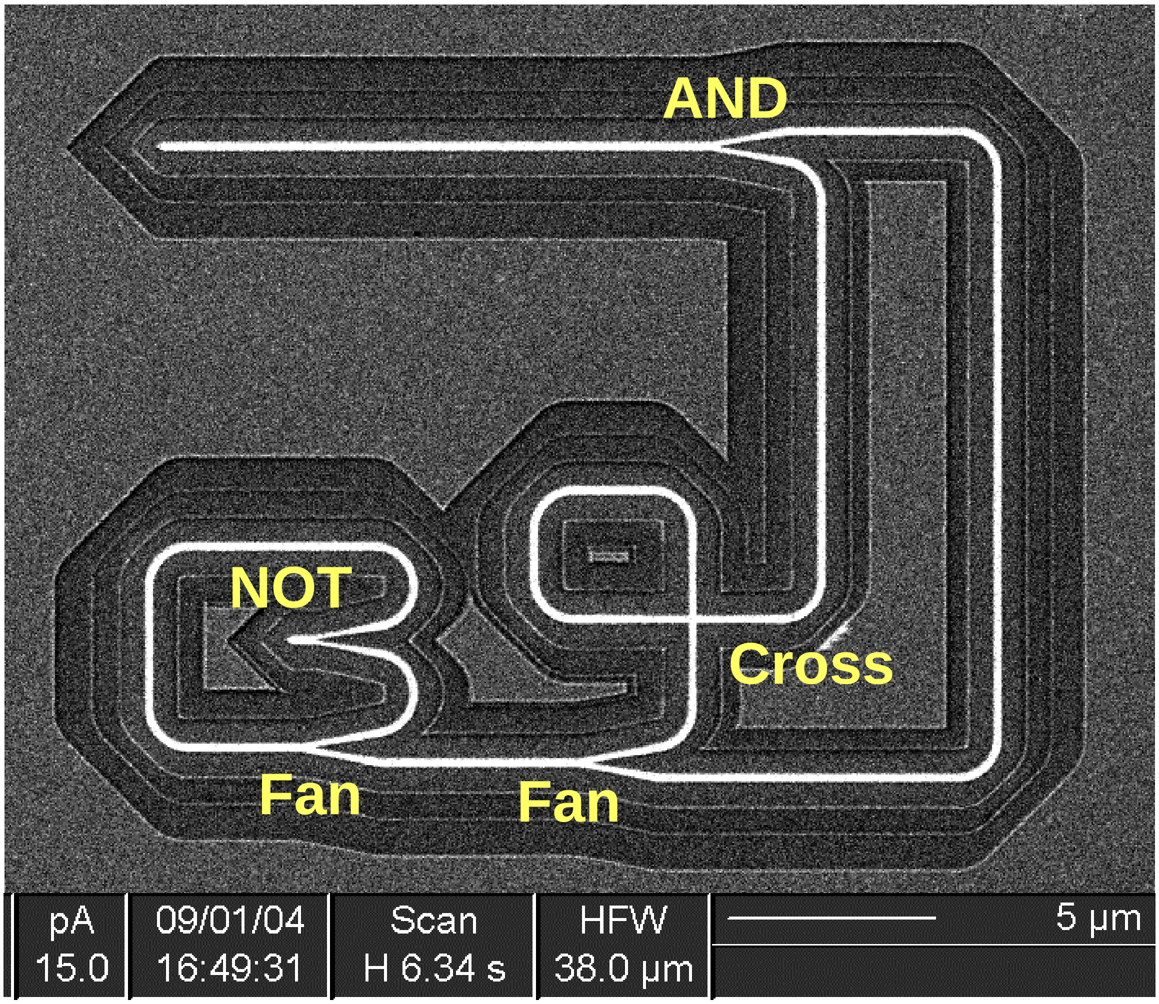

Figure 1: A working domain wall logic circuit comprising a NOT gate, two fan-out structures, a cross-over structure and an AND gate. Information is represented by the magnetisation direction in the Permalloy nanowires.